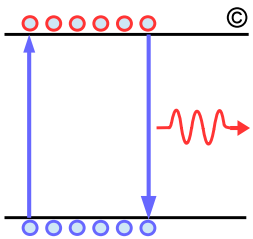

Considerations for CRU BW 400 GbE PMDs in Support of Comments

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Ghiasi Quantum LLC

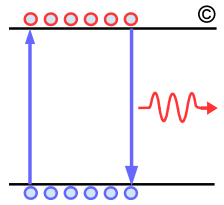
802.3bs Plenary Meeting
Macau

March 14, 2016

List of Supporters

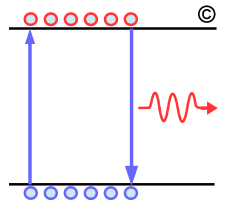
- **Gary Nicholl – Cisco Systems**
- **Vipul Bhatt – Inphi Inc**
- **Fernando De Bernardinis - Marvel**

Comments addressed



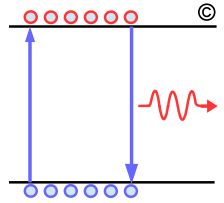
- Comment 102 CRU BW for 400Gbase-DR4
- Comment 103 stress receiver sensitivity for 400Gbase-DR4
- Comment 104 CRU BW for CDAUI-8 C2C
- Comment 105 stress receiver sensitivity for CDAUI-8 C2C
- Comment 109 CRU BW for CDAUI-8 C2M
- Comment 110/114 module output CRU for CDAUI-8 C2M
- Comment 111 host output CRU BW for CDAUI-8 C2M
- Comment 112 host SerDes stress sensitivity CDAUI-8 C2M
- Comment 113 Host output CRU CDAUI-8 C2M
- Comment 114 Host stress sensitivity CDAUI-8 C2M
- Comment 116 CRU BW for 400Gbase-FR8/LR8
- Comment 117 stress receiver sensitivity for 400Gbase-FR8/LR8.

Overview



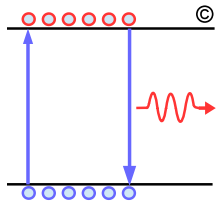
- **Previously considerations for CRU and CDR BW have been presented in details**
  - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
  - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
  - http://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf
  - http://www.ieee802.org/3/bs/public/16_01/ghiasi_3bs_01a_0116.pdf
- **802.3bs has no specific objective for a ports to be backward compatible with legacy 10 GbE, 40 GbE, or 100 GbE**
  - Since 802.3ae in Ethernet we have been using CRU BW of Fbaud/2578
  - CRU BW for standards at 10.3125 GBd/lane is 4 MHz
  - CRU BW for standards at 25.78 GBd/lane is 10 MHz
  - The market however requires at least the host provide a level of backward compatibility
  - CDAUI-16 based on 4 instance of CAUI-4 carries forward 10 MHz CRU
- **During Atlanta meeting there where more support for 2 MHz CRU but majority wanted more supporting material**
  - The group understand well that more sophisticated PAM4 receiver have inherent latency and to support 4 or 10 MHz require burning more power
  - Using 6 representative paper from ISSCC 2016 next will explore impact of reducing CRU BW on OSC/VCO phase noise and its impact on the transmitter jitter
- **It is important for the P802.3bs make decision regarding CRU BW with a value between 2 and 4 MHz!**

Consideration for CRU and CDR BW

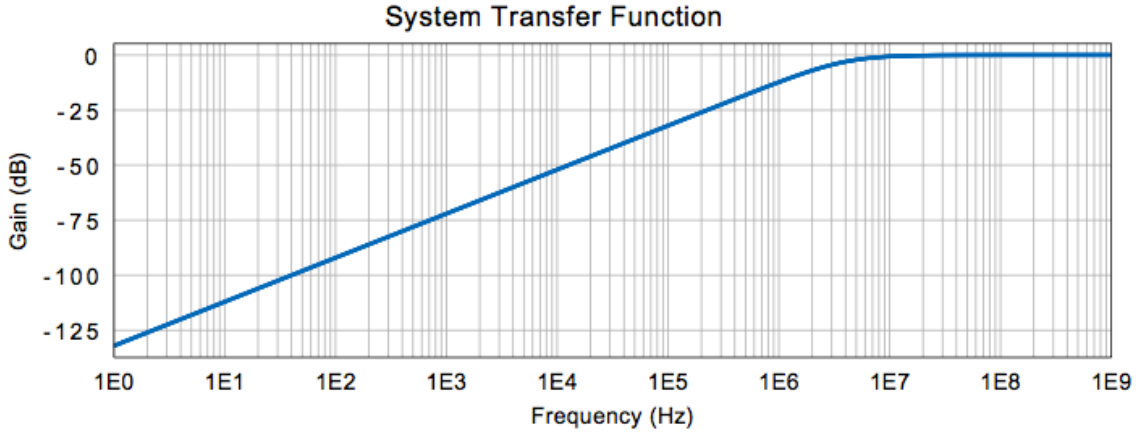


- **Consideration for the golden PLL CRU BW**
  - Oscillator phase noise
    - Typical oscillator have flat phase noise> 1 MHz
  - Crosstalk
    - High frequency effects >> CRU BW
  - VCO phase noise
    - No benefit when CRU BW > 4MHz
- **Consideration for CDR BW**
  - Pattern dependent effect
    - Does not apply to 64B/66B/scrambled data with spectrum in the ~ 100 KHz
  - Power
    - Higher loop BW results in higher CDR power
  - DSP receiver
    - Timing recovery introduces latency making it challenging to meet traditional Fbaud/2578 CDR loop BW
  - Backward compatibility
    - Does an HOM port only operate at single speed with another HOM port or the port need to interoperate at lower bit rate with CAUI-4, CR4, SFI, etc?
    - An implementation requiring backward compatibility through a common data path would need 10 MHz CDR BW.

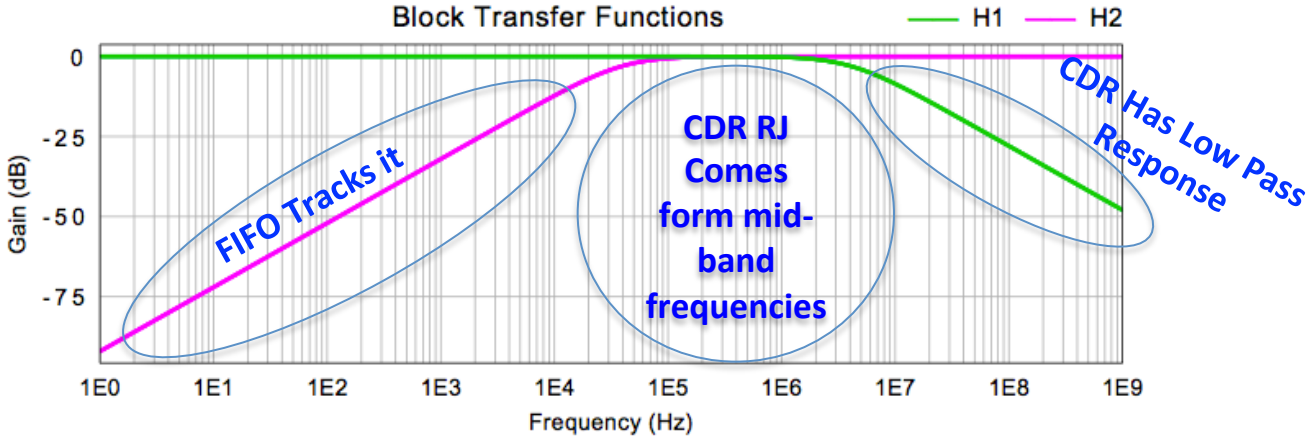
Filter for Phase Noise Analysis of 5 ISSCC 2016 Papers



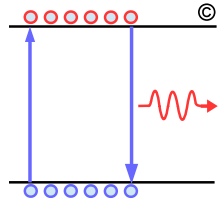
- **Transmitter jitter calculated with high pass filter "Golden PLL"**
  - Graph shown is for 4 MHz Golden PLL



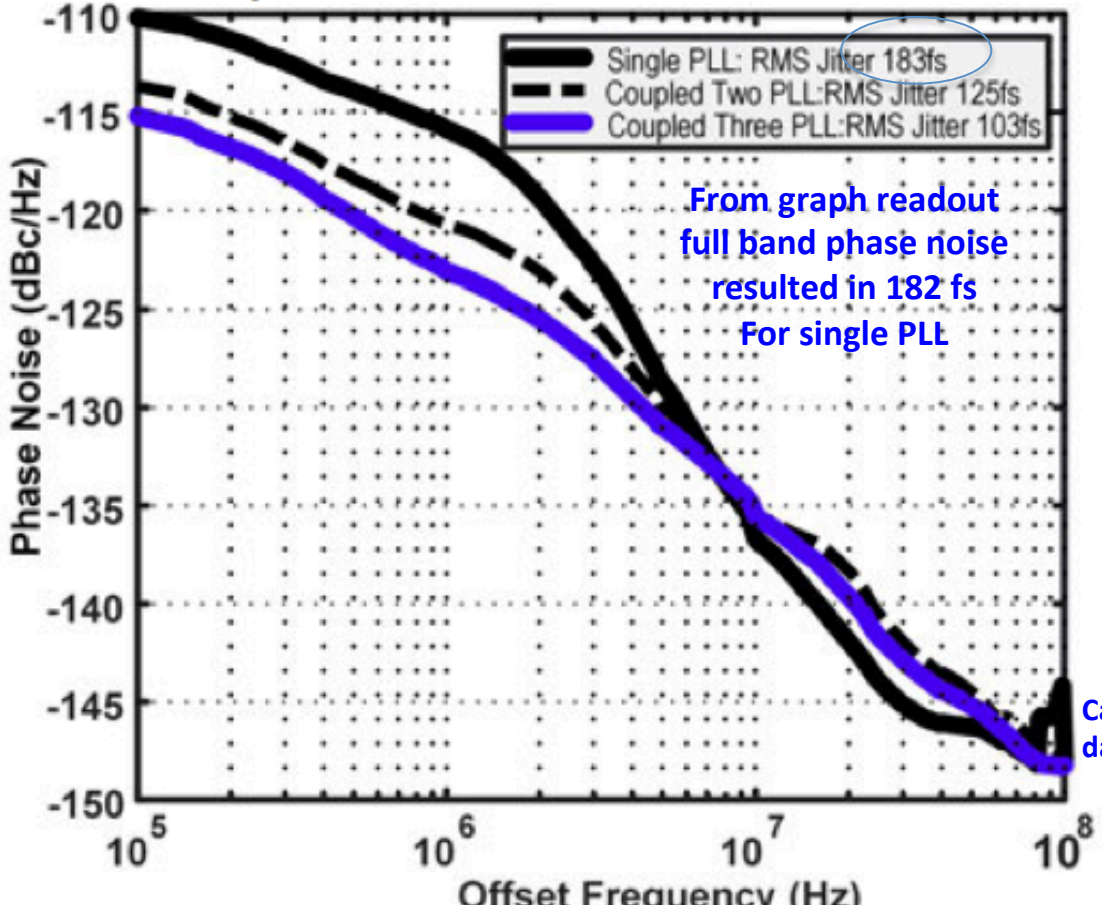
- **Receiver jitter analyzed by sliding band-pass filter**
  - Graph shown is for 4 MHz Golden PLL



I. VCO Phase Noise from ISSCC 2016



ISSCC 2016- 2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large- Scale 5G mm-Wave Arrays



From graph readout full band phase noise resulted in 182 fs For single PLL

Calculation Based on Single Stage PLL

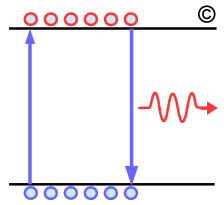
Observed by Golden PLL
10 MHz = 42 fs
4 MHz = 69 fs
2 MHz = 95 fs

Observed by RX CDR
10 MHz = 45 fs
4 MHz = 21 fs
2 MHz = 10 fs

Can be artificially low since no phase data below 100 kHz provided

Phase noise output for ÷8=3.5 GHz

II. VCO Phase Noise from ISSCC 2016



ISSCC 2016 2.4 A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications

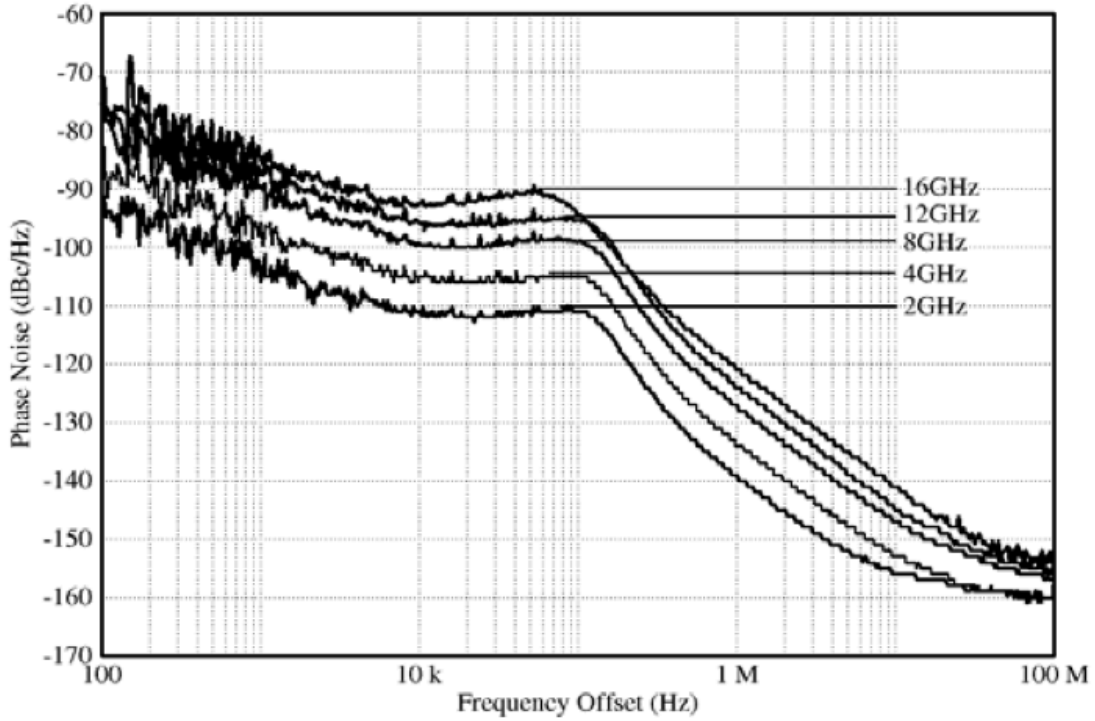


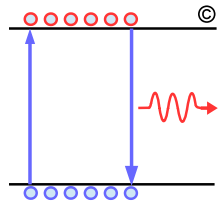
Figure 2.4.5: LO phase noise measurement results at different output frequencies.

Calculation for 16 GHz Output

Observed by RX CDR
10 MHz = 6 fs
4 MHz = 10 fs
2 MHz = 14 fs

Observed by Golden PLL
10 MHz = 127 fs
4 MHz = 104 fs
2 MHz = 87 fs

III. VCO Phase Noise from ISSCC 2016



9.6 A 2.7-to-4.3GHz, 0.16psrms-Jitter, -246.8dB-FOM, Digital Fractional-N Sampling PLL in 28nm CMOS

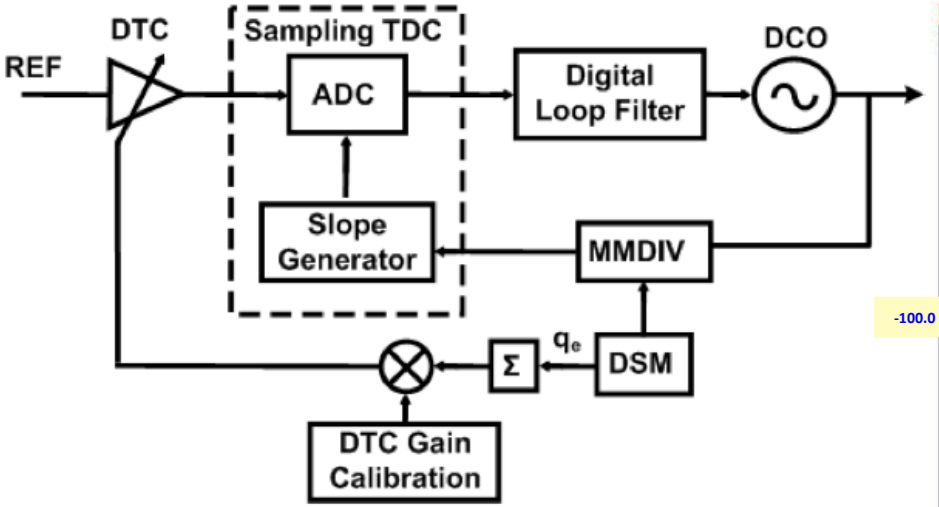
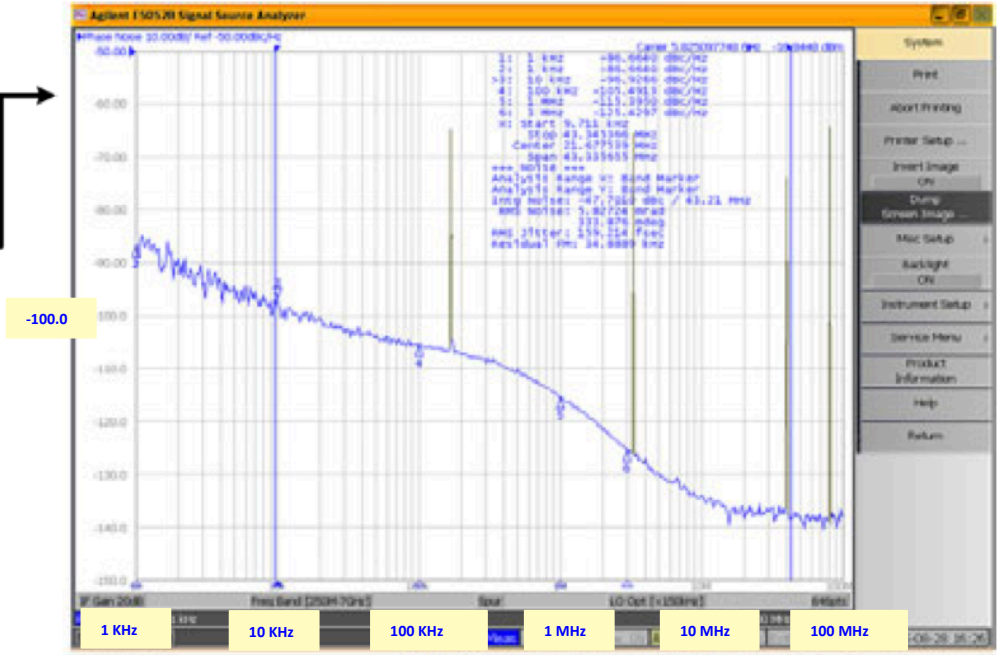


Figure 9.6.1: Proposed digital frac-N sampling PLL architecture.

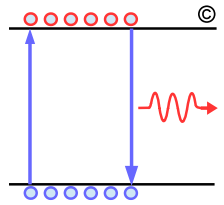
Phase Noise Output for 5825 MHz



Observed by Golden PLL
10 MHz = 49 fs
4 MHz = 59 fs
2 MHz = 71 fs

Observed by RX CDR
10 MHz = 127 fs
4 MHz = 111 fs
2 MHz = 100 fs

IV. VCO Phase Noise from ISSCC 2016



ISSCC 2016 10.8 A 12-to-26GHz Fractional-N PLL with Dual Continuous Tuning LC-D/VCOs

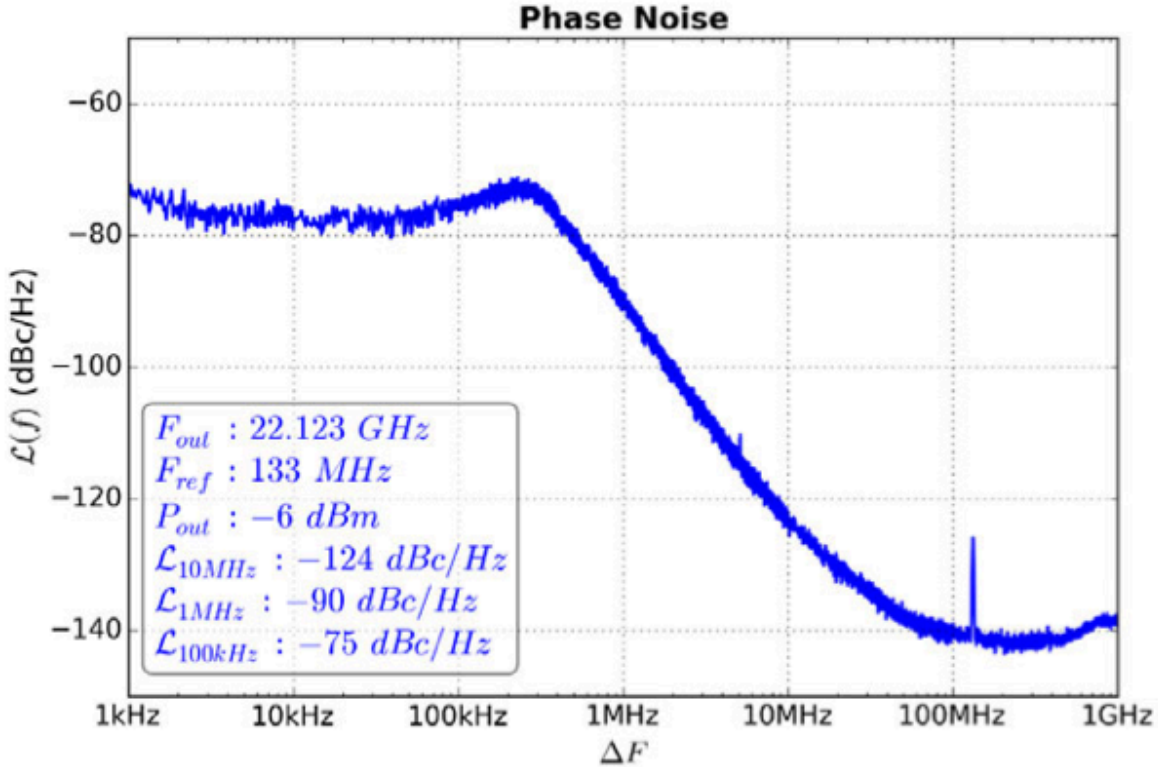


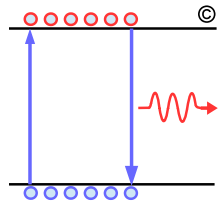
Figure 10.8.5: Hybrid PLL measured phase noise, fractional-N mode. Measured noise @10MHz offset from the carrier is better than -120dBc/Hz across the PLL tuning range.

Calculation Based on Single Stage PLL

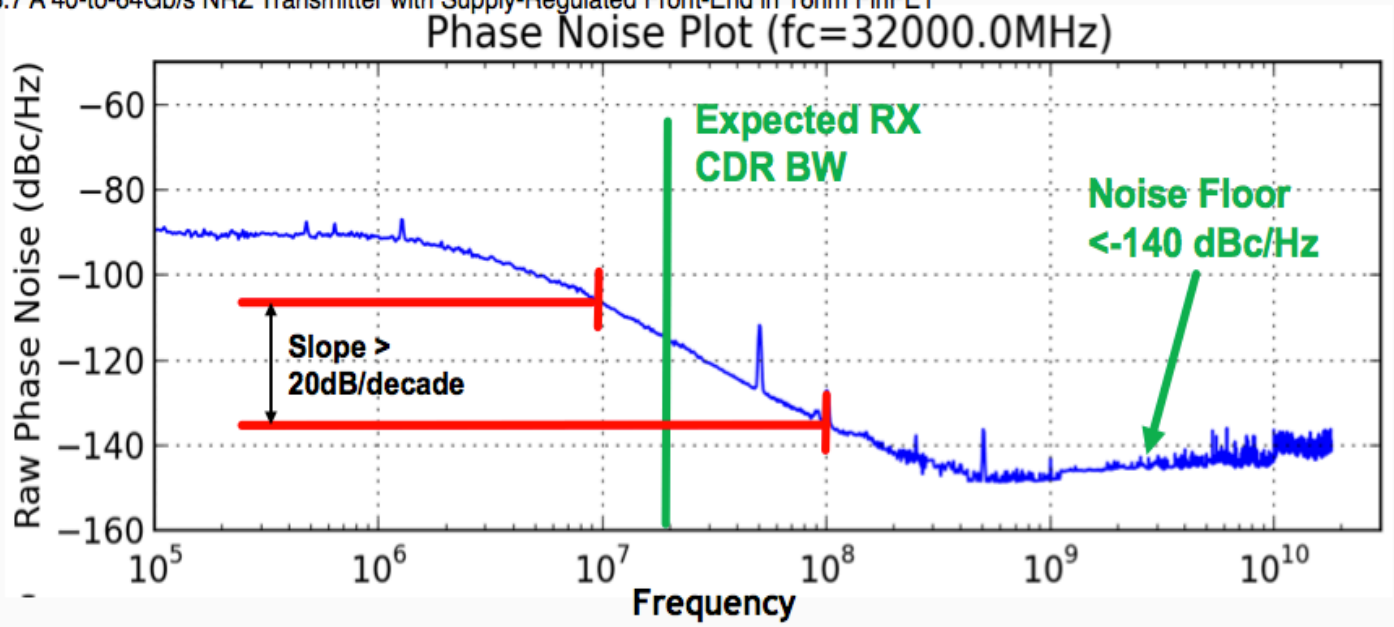
Observed by Golden PLL
10 MHz = 74 fs
4 MHz = 176 fs
2 MHz = 330 fs

Observed by RX CDR
10 MHz = 668 fs
4 MHz = 399 fs
2 MHz = 267 fs

V. VCO Phase Noise from ISSCC 2016



3.7 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET



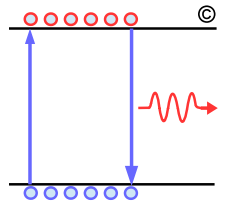
- Low phase noise floor from the use of CMOS clock buffers
- No significant spurs from supply noise
- Flicker noise corner > 10MHz, but phase noise level is low
  - Expect CDR filter to suppress it further

Observed by Golden PLL
10 MHz = 116 fs
4 MHz = 179 fs
2 MHz = 228 fs

Observed by RX CDR
10 MHz = 57 fs
4 MHz = 25 fs
2 MHz = 13 fs

Can be artificially low since no phase data below 100 kHz provided

Summary



- **Reliable link operation requires that the receiver tests jitter masked by the Golden PLL**
- **HOM receivers are more complex with timing recovery potentially having higher latency could make it difficult to support Fbaud/2578 CRU**
- **During Atlanta meeting there were general consensus that should consider reducing CRU BW but concern were also raised that reducing CRU BW to 2 MHz may burden the transmitter**
- **To better understand how much a burden will result in reducing the CRU BW to 2 or 4 MHz 5 representative ISSCC-2016 PLL papers jitter contribution from phase noise studied**
  - PLL I, II, and III perform very well with as low as 2 MHz
  - PLL IV phase noise is high for any BW either transmitter or receiver may fail
  - PLL V designed high BW is marginal with 2 MHz CRU
- **Reducing CRU BW on CDAUI-16 from 10 MHz to 2 MHz may result some implementations not meeting the transmit jitter unless one uses an OSC with improved phase noise**
- **Three viable options explored are:**
  - Option I: stay with 10 MHz CRU for all 400 GbE PMDs – Not Viable
  - Option II: go with 4 MHz CRU for all 400 GbE PMDs – 2 MHz would be better for HOM receiver but advantage is that all 400 GbE PMDs including could operate with 4 MHz
  - Option III: go with 2 MHz for all 8 and 4 lanes PMDs but CDAUI-16 based based CAUI-4 cores may have difficulty meeting transmit jitter with 2 MHz CRU
- **What ever we choose for CRU BW the receiver must operate with identical stress and be able to tolerate jitter components masked by the transmit CRU high pass response**
- **We know how to deal and manage any interoperability issue choosing 4 or 2 MHz CRU and we are overdue to make a decision!**