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Comment #41: Effects of the change from Np=13 to Np=200

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IEEE P802.3bs 200GbE and 400GbE Task Force
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Background

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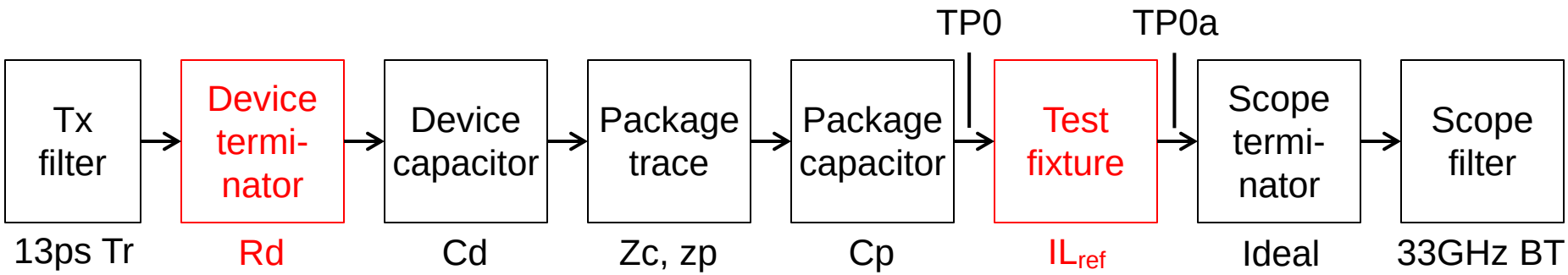
- Np was changed from 13 to 200 in Draft D2.1.
- A larger Np value increases the steady-state voltage v_f, because a longer fillted pulse will capture more long-term ISI.
  - On the other hand, peak of the fillted pulse does not change.
- As a result, the ratio of the linear fit pulse peak to v_f is reduced.
- In order to keep the requirement for Tx same, we should adjust v_f and the ratio of the linear fit pulse peak to v_f consistently with the change to Np.

This presentation is an updated version of hidaka_01_102416_elect.pdf which was presented at electric ad hoc on October 24, 2016

Simulated Model

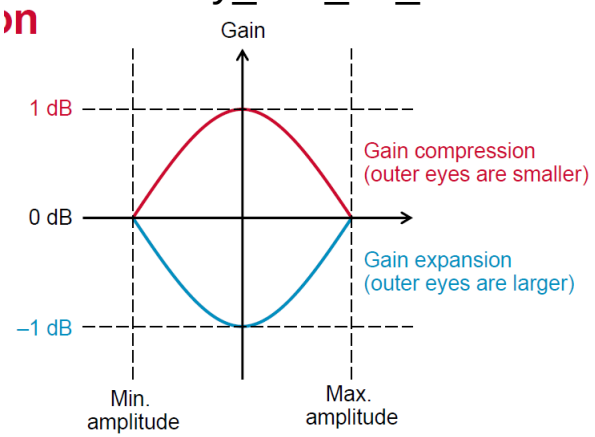


- Tx filter: $S_{21} = (\mathrm{EQ93A{-}46} | T_r = 13\mathrm{ps}, \beta = 2)$ (i.e. 13ps 20-80% Tr)
- Device terminator: $S_{21} = \frac{100\Omega}{Rd+50\Omega}, S_{22} = \frac{Rd-50\Omega}{Rd+50\Omega}$
  - S_{21} was updated from 1 that was used for hidaka_01_102416_elect.pdf
- Device capacitor: $S = (\mathrm{EQ93A{-}8} | C = C_d)$
- Package trace: $S = \left(\mathrm{EQ93A{-}13,14} \middle| \mathrm{Table93A{-}3\ except}\ Z_c, z_p\right)$
- Package capacitor: $S = \left(\mathrm{EQ93A{-}8} \middle| C = C_p\right)$
- Test fixture:
  - A: $|S_{21}| = 10^{-(\mathrm{EQ93-1})/20}, \angle S_{21} = \mathrm{minimum\ phase}(|S_{21}|)$
  - B: 38mm Host PCB trace using EQ93A-13,14 with Table 92-12
- Scope terminator: $S_{21} = 1, S_{11} = 0$ (i.e. ideal)
- Scope filter: 4-th order Bessel-Thomson LPF with 33GHz 3dB BW
  - $\omega_0 = 98.28967142447435\ \mathrm{G\ rad/s}$

Simulation Methodology

1. Get S_{21} of the entire model from 1MHz to f_{max} with 1MHz step
   - $f_{max} = 26.5625\text{GHz} \times M \div 2$, where $M = 32$
2. Get a single-bit pulse response
3. Get a linear cycle response of PRBS13Q with ideal levels
4. Cancel the DC offset of the linear cycle response of PRBS13Q
5. Get a non-linear cycle response of PRBS13Q by gain expansion / compression (similar to a methodology in healey_3bs_02_0916)
   - Simulated from -1.0dB to +1.0dB with 0.2dB step
6. Get V0, V1, V2, and V3 per 120D.3.1.2.1
7. Get Vmid, ES1, and ES2 per 120D.3.1.2
8. Get ES=(ES1+ES2)/2 per 120D.3.1.3
9. Get linear fit pulse p(k) and error e(k) per 120D.3.1.3, 94.3.12.5.2, 85.8.3.3.5
   - Dp=2 and Np=13 or 200
10. Get steady-state voltage v_f and linear fit pulse peak p_{max} per 120D.3.1.4
11. Get σ_e from e(k), then get SNDR per 120D.3.1.6
    - σ_n is always set to $p_{max} \times 10^{(-50/20)}$ (i.e. -50dB) to have noise floor

From healey_3bs_02_0916



Simulated Package Parameters

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- The following 10 combinations of parameters were simulated

Case	zp Package trace length	Rd Termination resistance	Zc Package trace impedance
#1	12 mm	45 Ω	85 Ω
#2			115 Ω
#3		55 Ω	85 Ω
#4			115 Ω
#5	30 mm	45 Ω	85 Ω
#6			115 Ω
#7		55 Ω	85 Ω
#8			115 Ω
#9	12 mm	50 Ω	100 Ω
#10	30 mm		

- Device capacitor: Cd = 280 fF
- Package capacitor: Cp = 110 fF

Values in red were updated from hidaka_01_102416_elect.pdf with correct parameters

TDR of Entire Path from Scope (zp=12mm)

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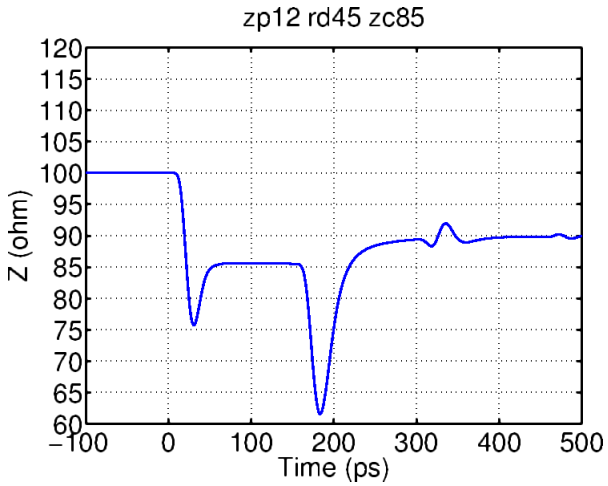
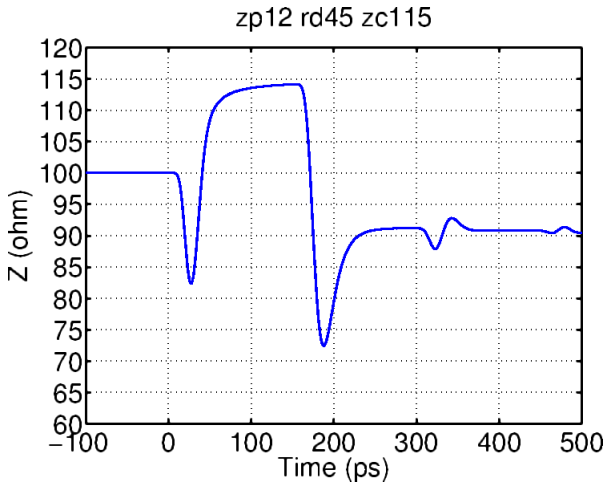
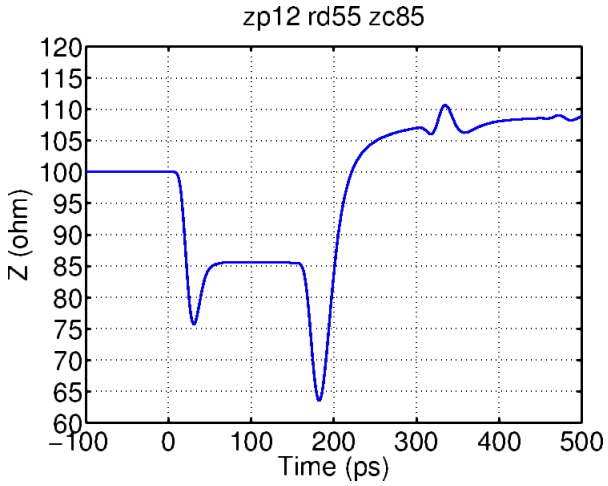
#1: Rd=45, Zc=85



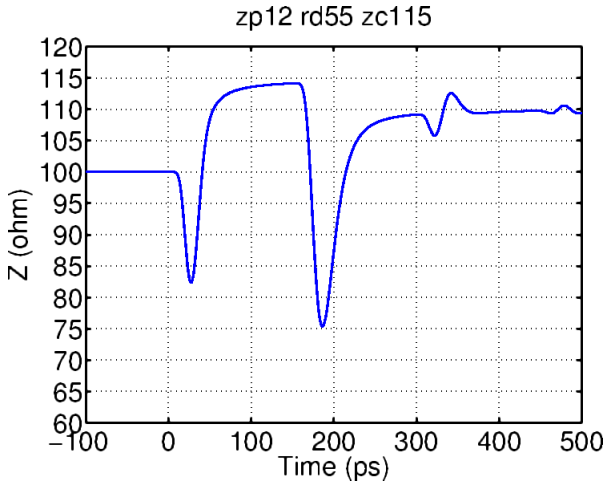
#2: Rd=45, Zc=115



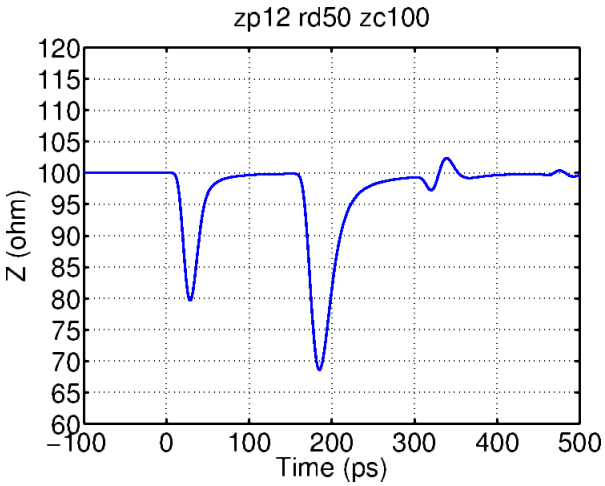
#3: Rd=55, Zc=85



#4: Rd=55, Zc=115

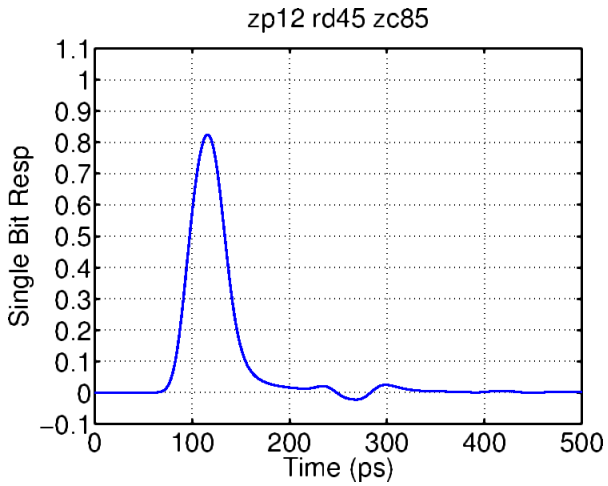


#9: Rd=50, Zc=100

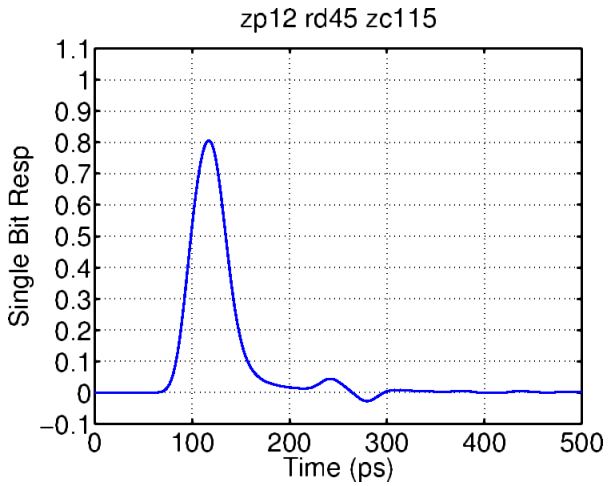


SBR of Entire Path (zp=12mm)

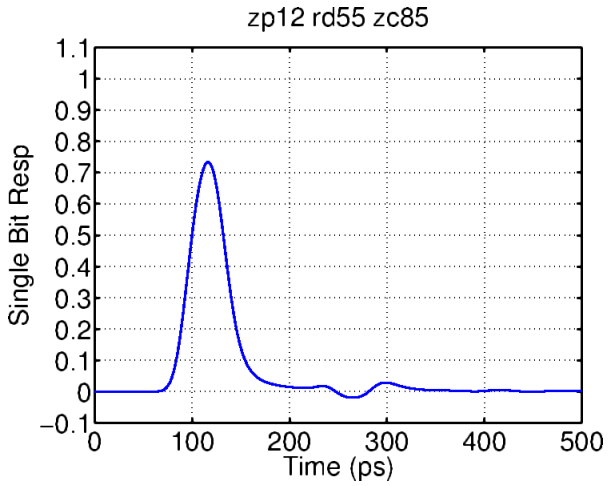
#1: Rd=45, Zc=85



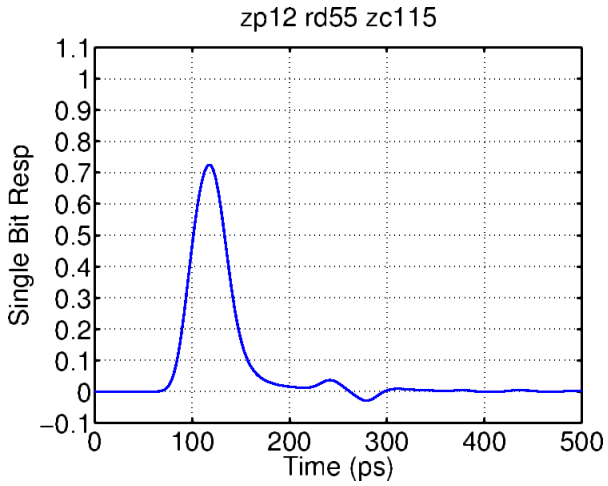
#2: Rd=45, Zc=115



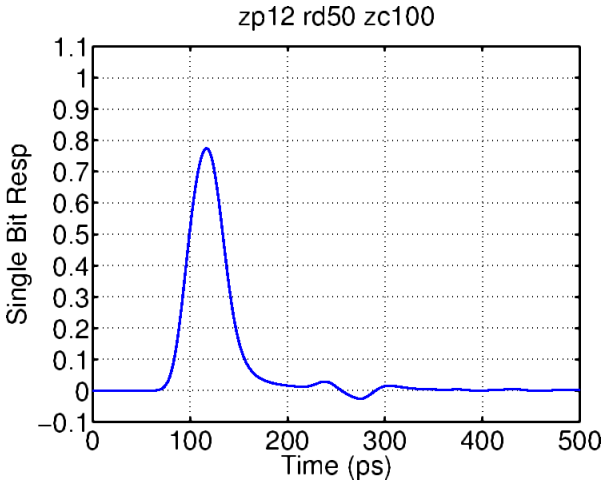
#3: Rd=55, Zc=85



#4: Rd=55, Zc=115



#9: Rd=50, Zc=100



TDR of Entire Path from Scope (zp=30mm)

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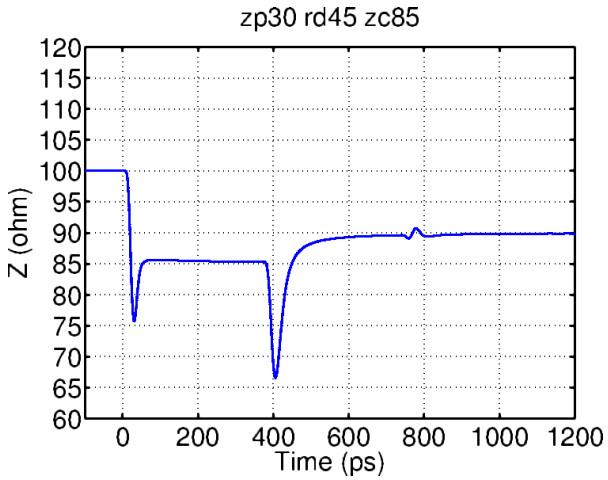
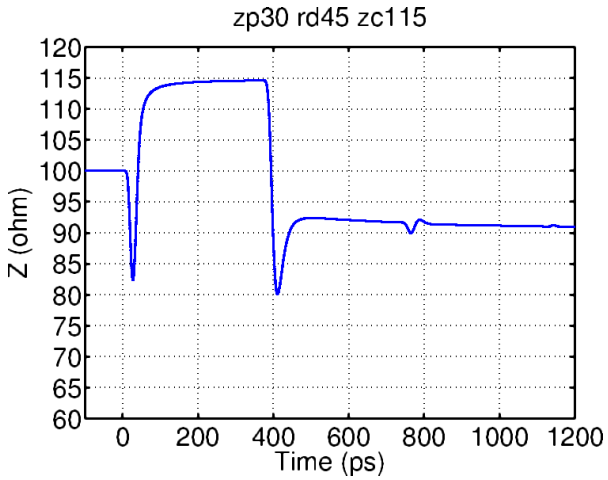
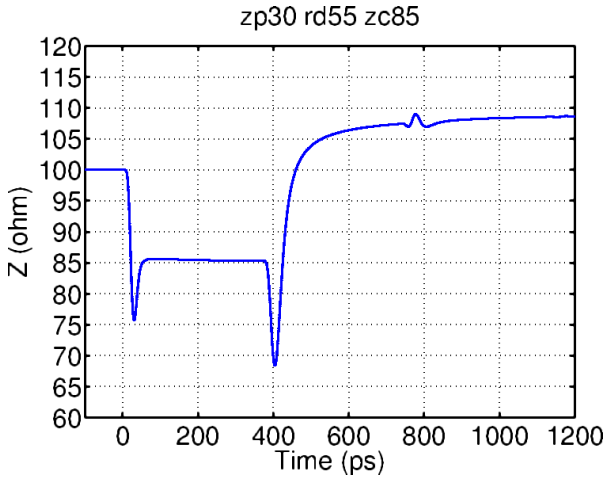
#5: Rd=45, Zc=85



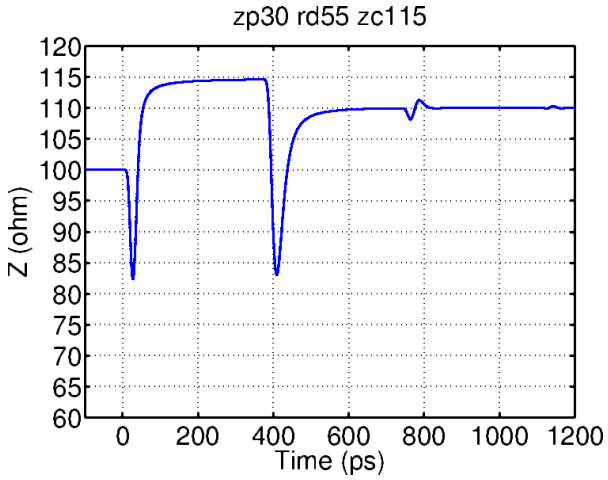
#6: Rd=45, Zc=115



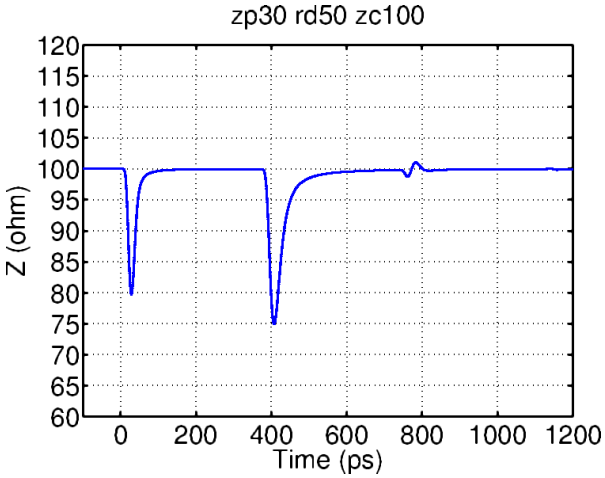
#7: Rd=55, Zc=85



#8: Rd=55, Zc=115



#10: Rd=50, Zc=100



SBR of Entire Path (zp=30mm)

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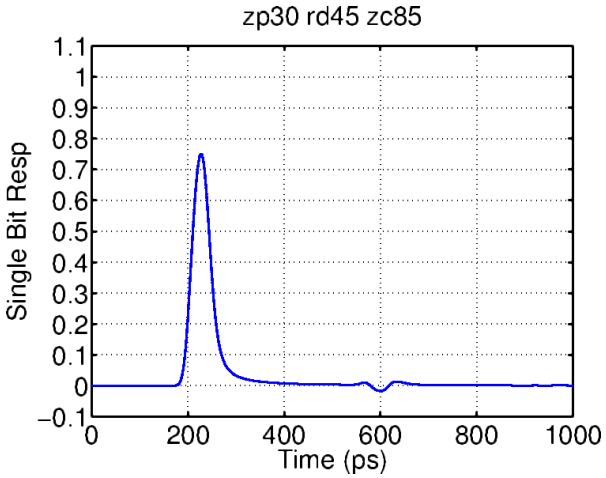
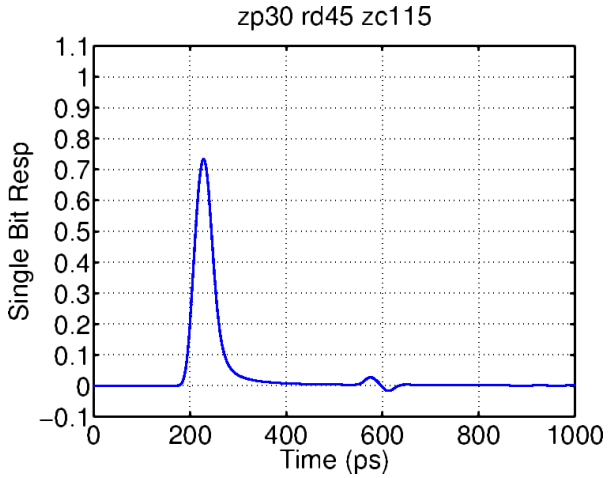
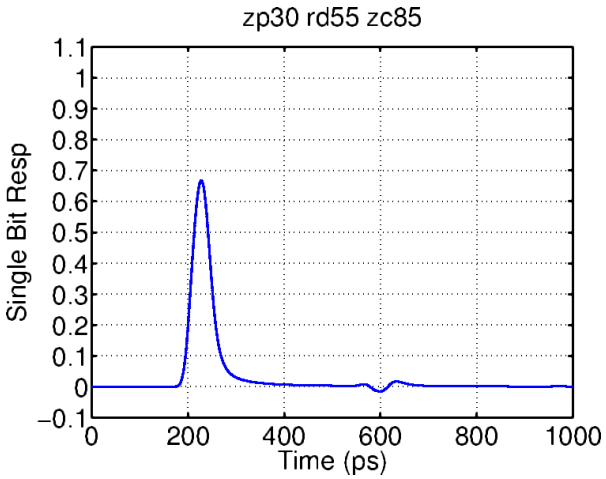
#5: Rd=45, Zc=85



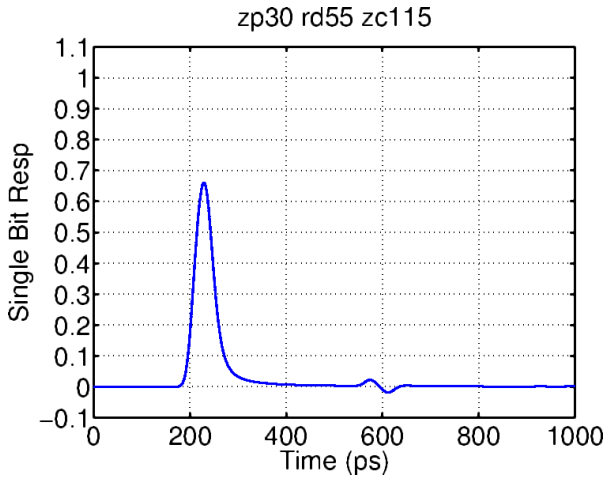
#6: Rd=45, Zc=115



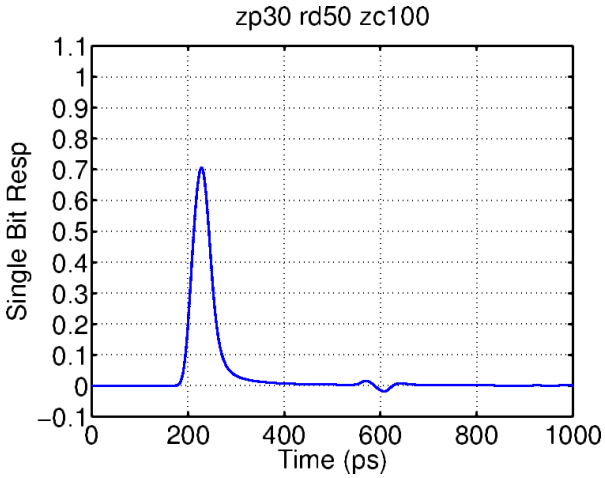
#7: Rd=55, Zc=85



#8: Rd=55, Zc=115



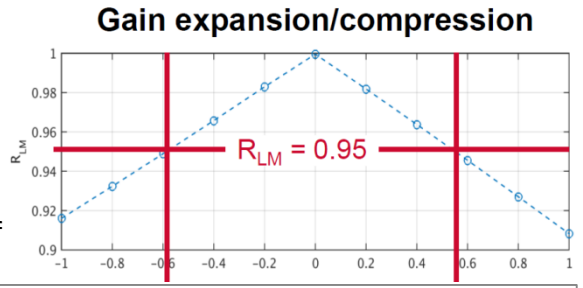
#10: Rd=50, Zc=100

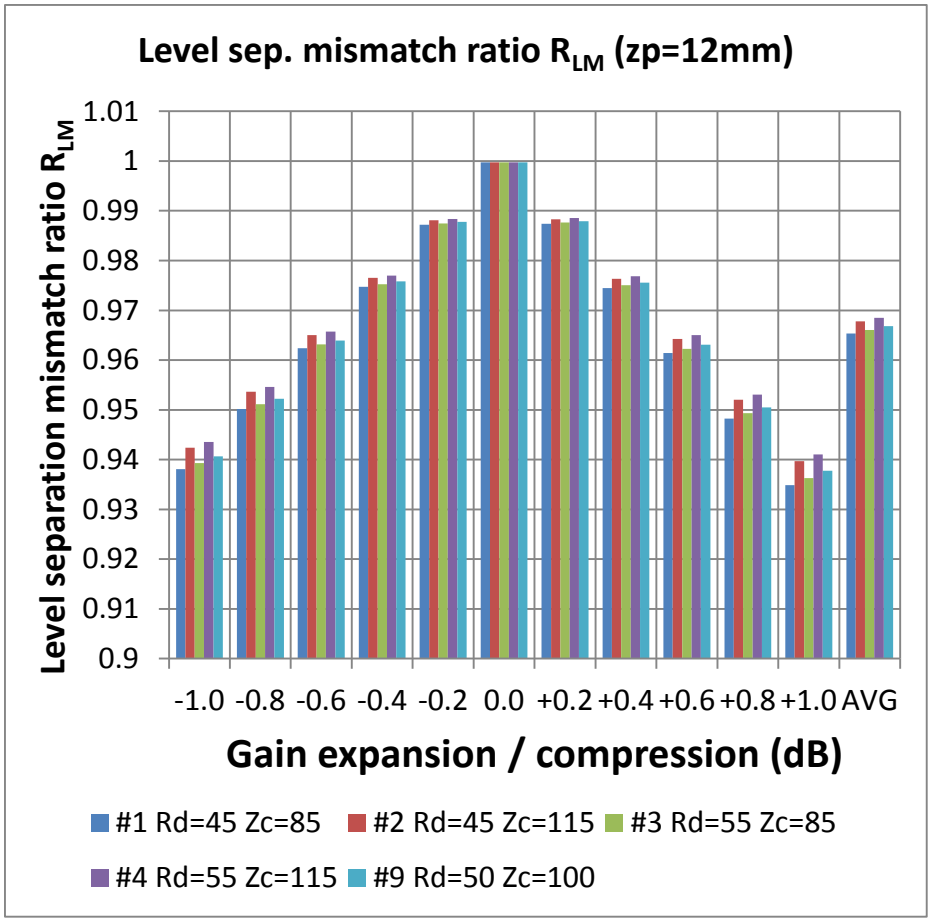


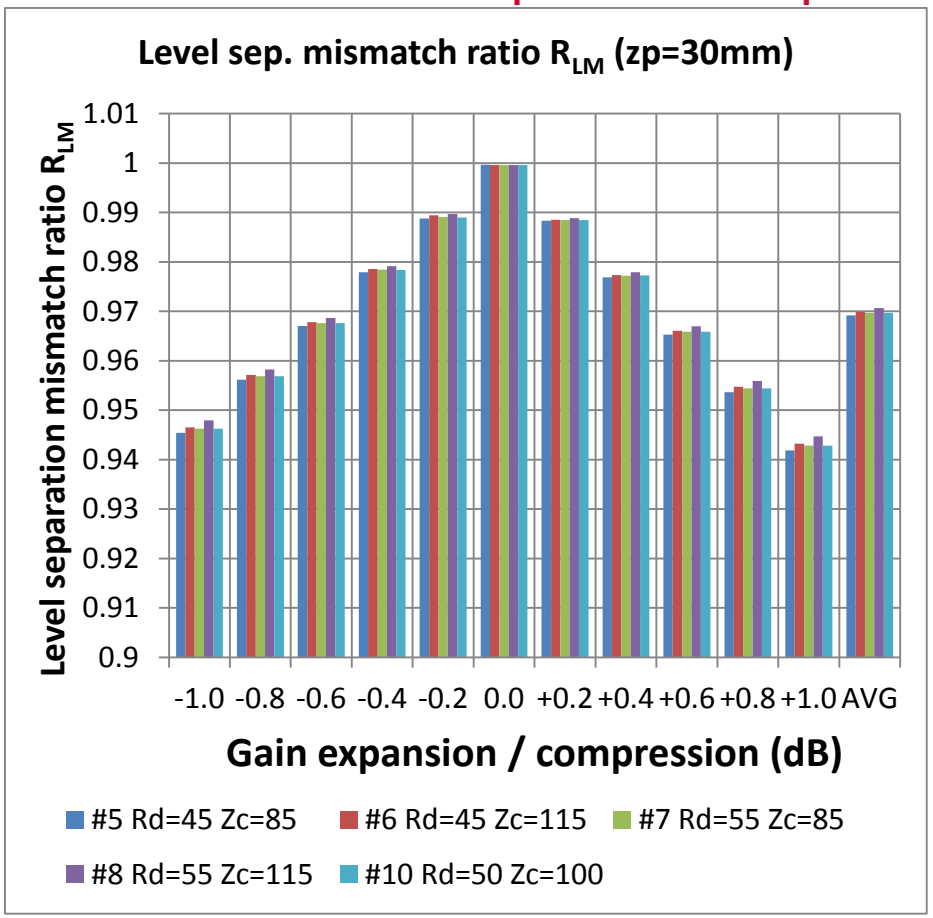
Level separation mismatch ratio R_{LM}

- Better than healey_3bs_02_0916.pdf
  - Maybe some model difference

healey_3bs_02_0916.pdf

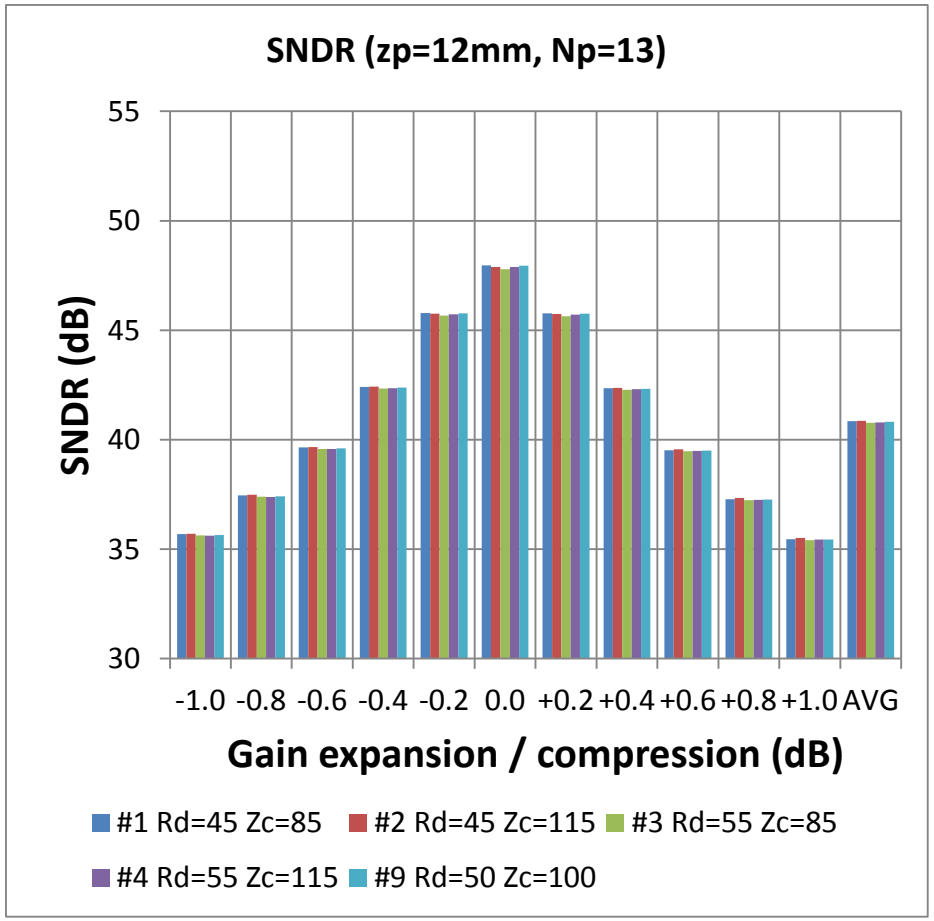


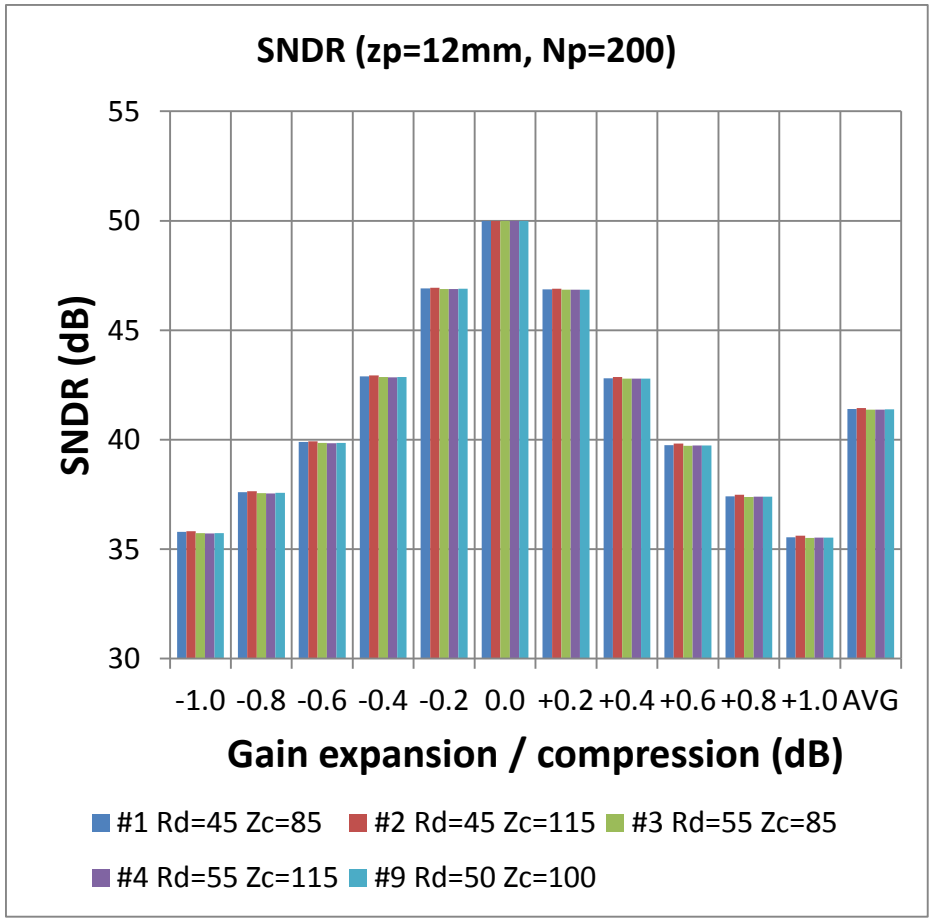




SNDR (zp=12mm)

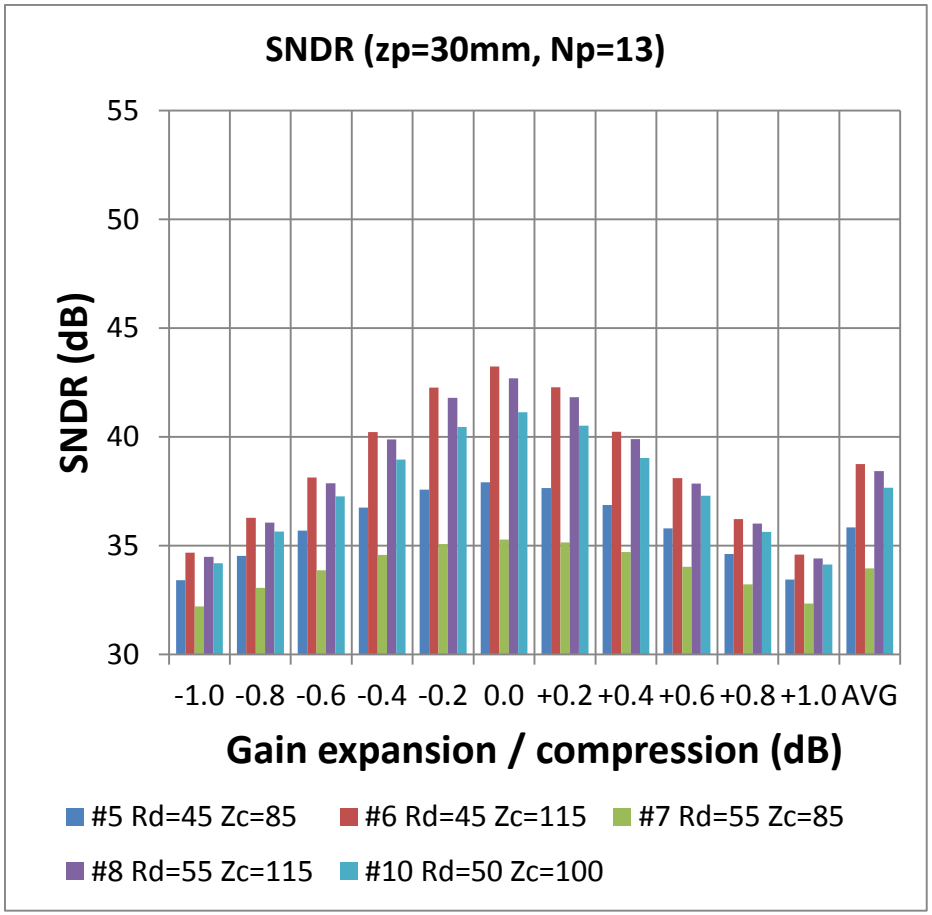
- Improved as expected
  - For the linear case, we can see the noise floor (50dB in this simulation)

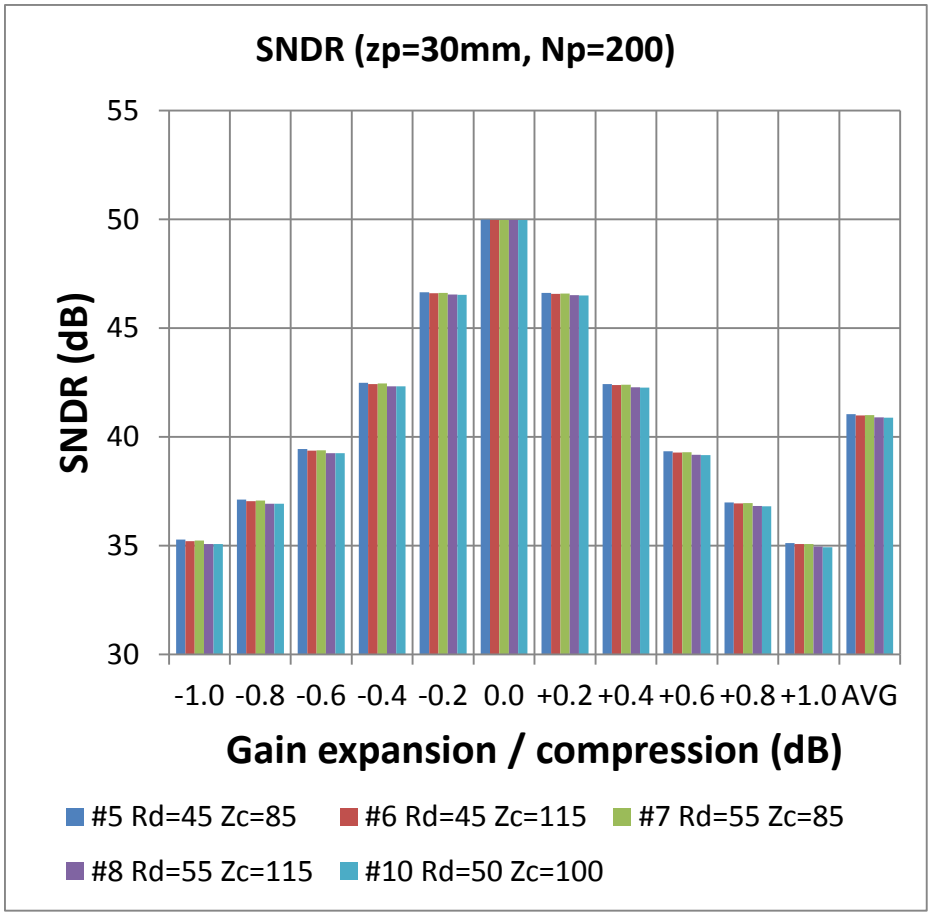




SNDR (zp=30mm)

- Less dependent on package parameters as expected
  - For the linear case, we can see the noise floor (50dB in this simulation)





Linear Fit Pulse Peak p_{max} (zp=12mm)

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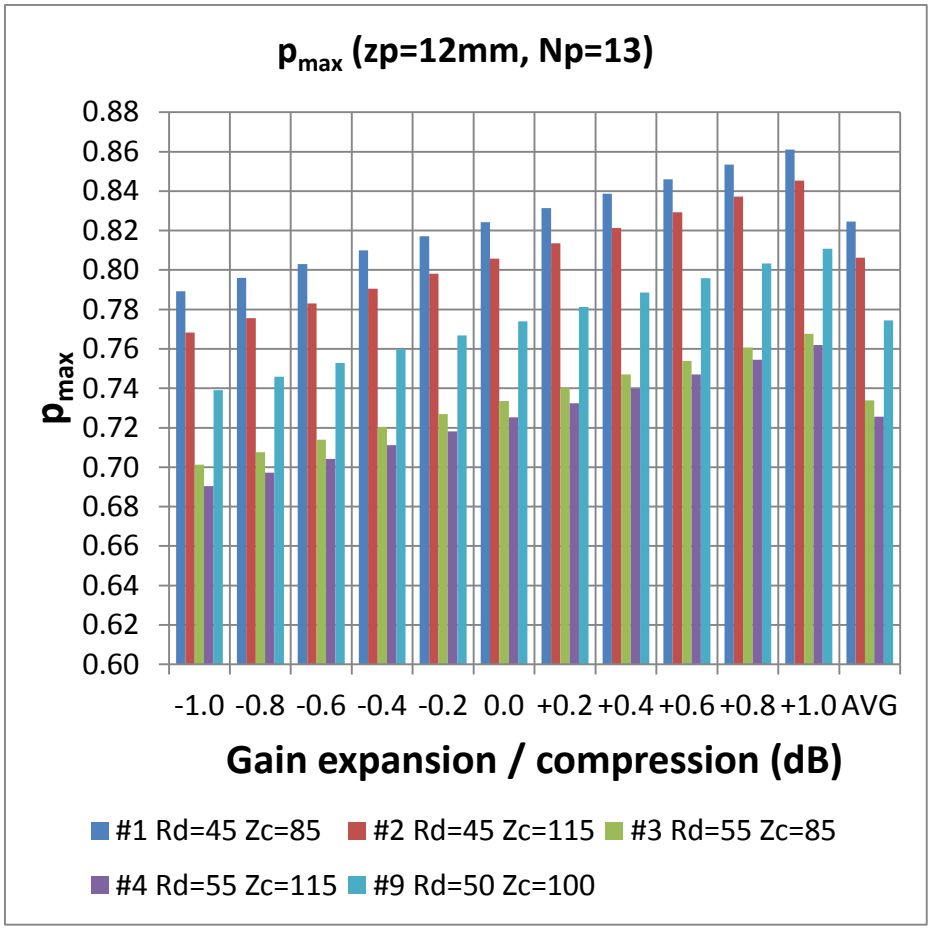
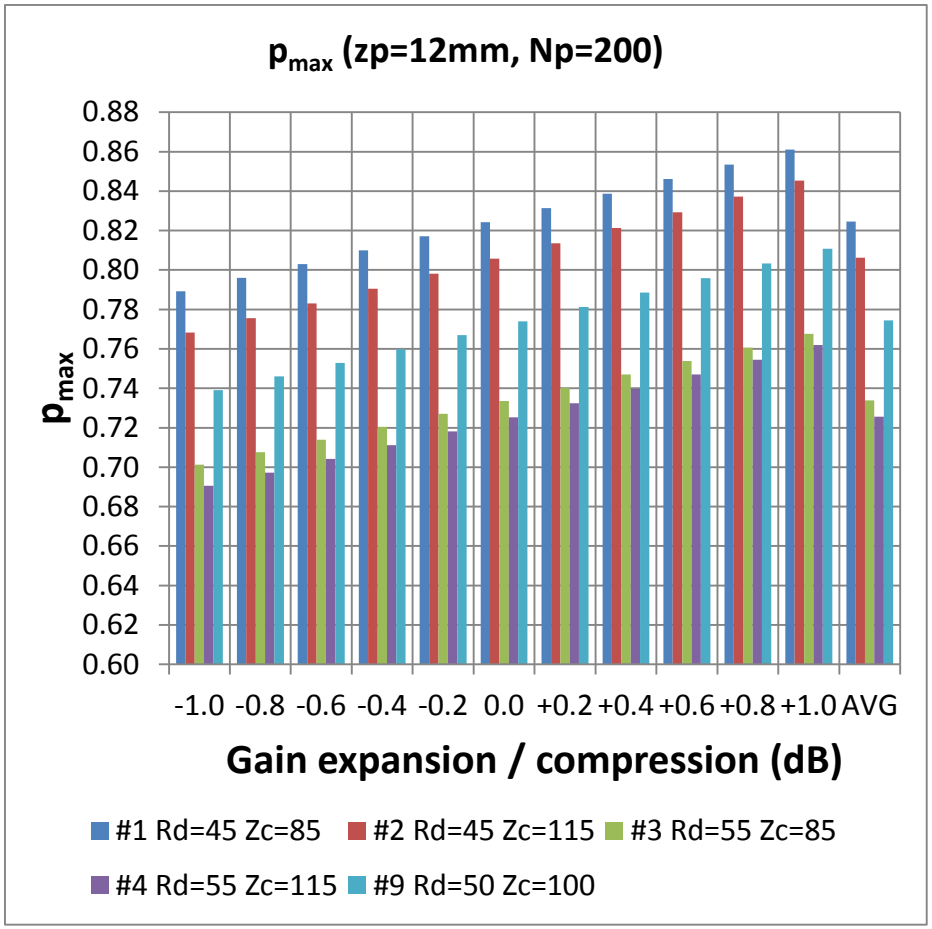
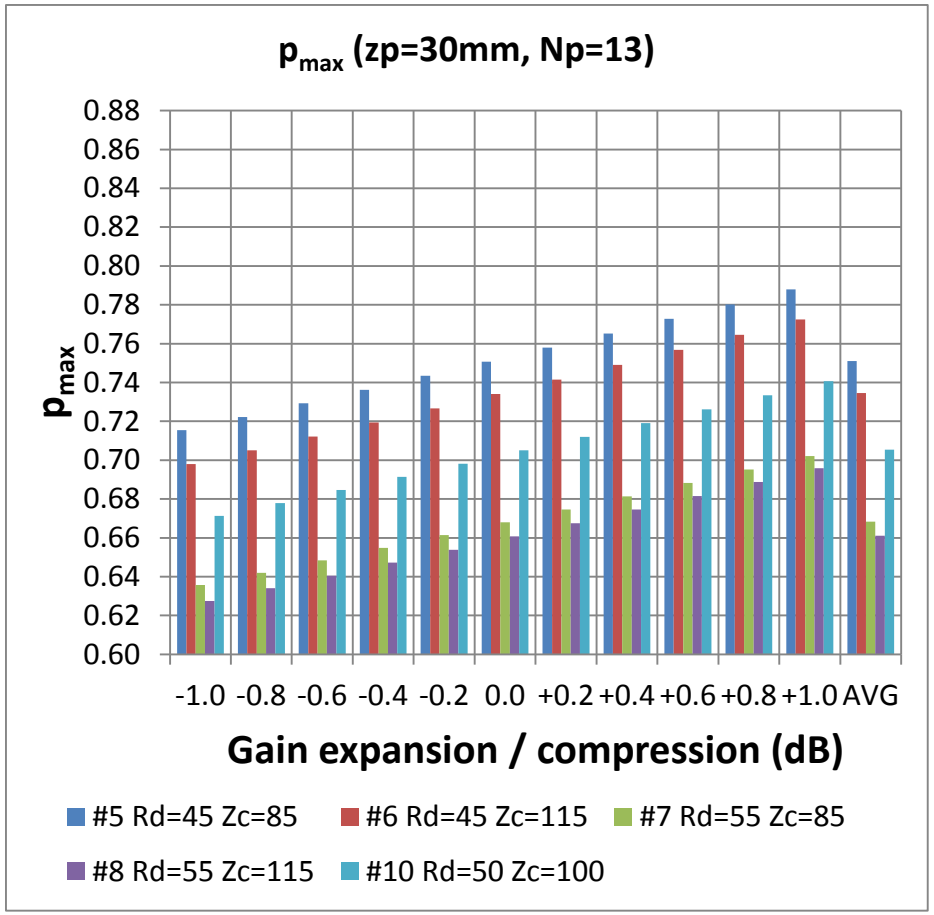
- Almost no effect
  - The average effect was 0.00049%

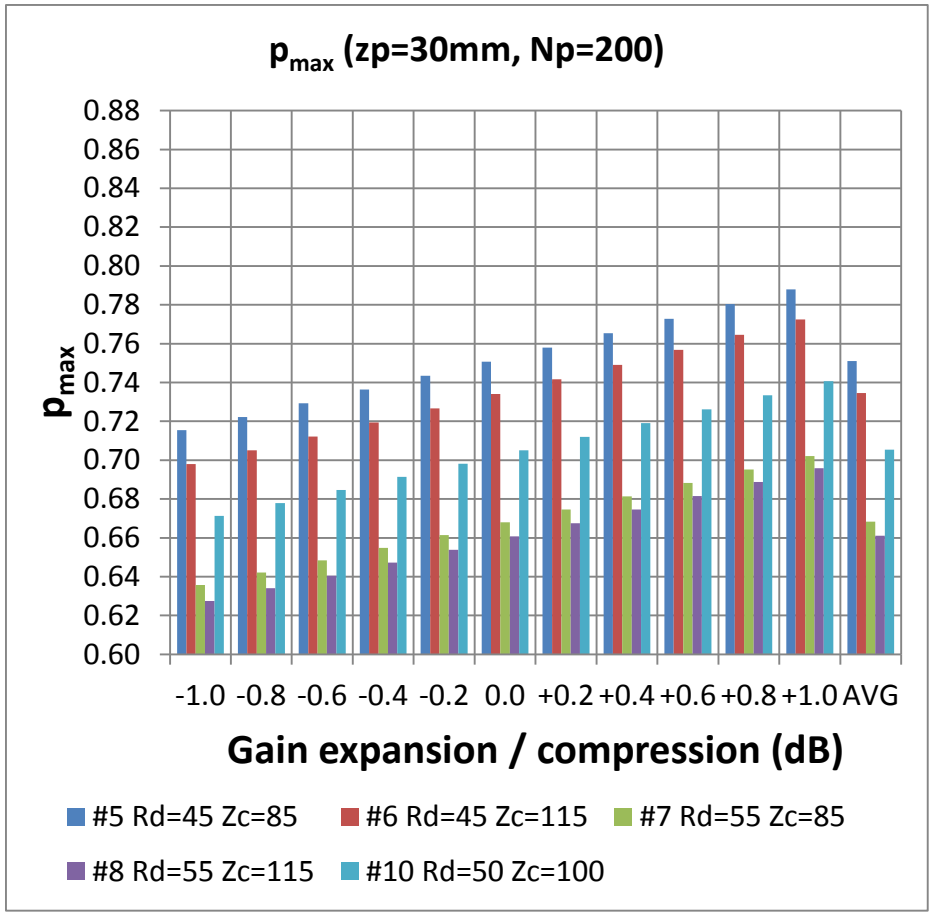




Linear Fit Pulse Peak p_{max} (zp=30mm)

- Almost no effect
  - The average effect was 0.0012%





Steady-State Voltage v_f (zp=12mm)

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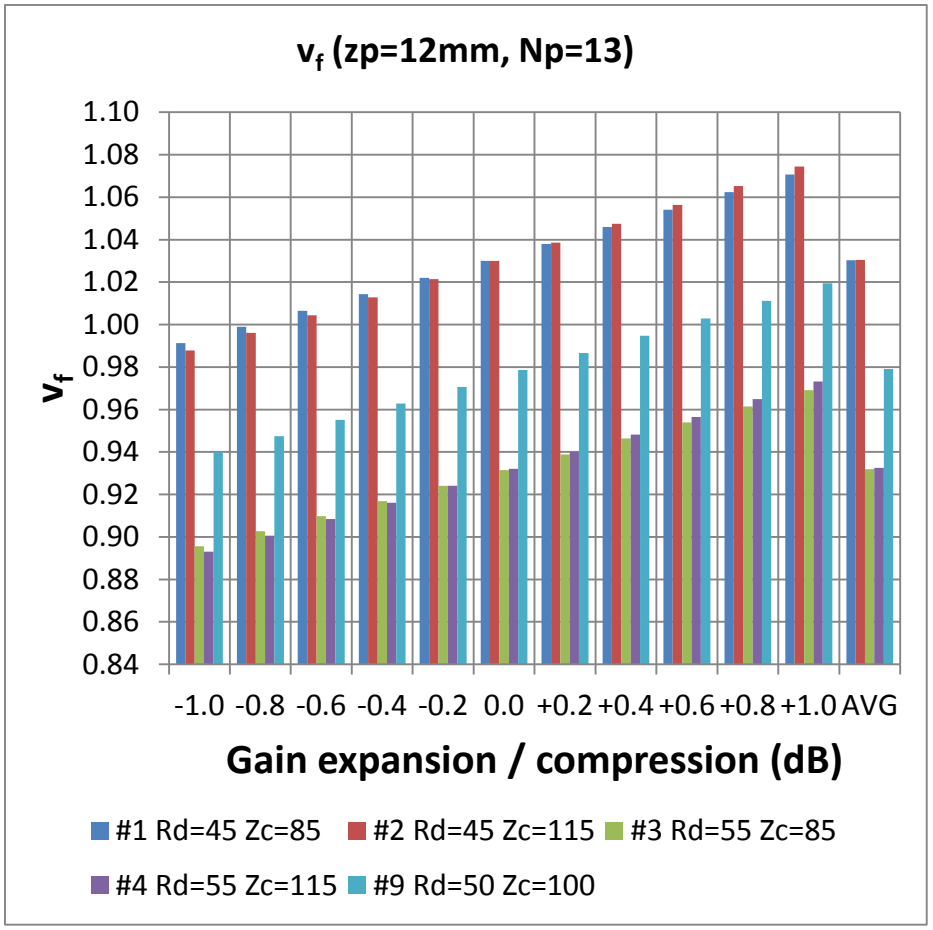
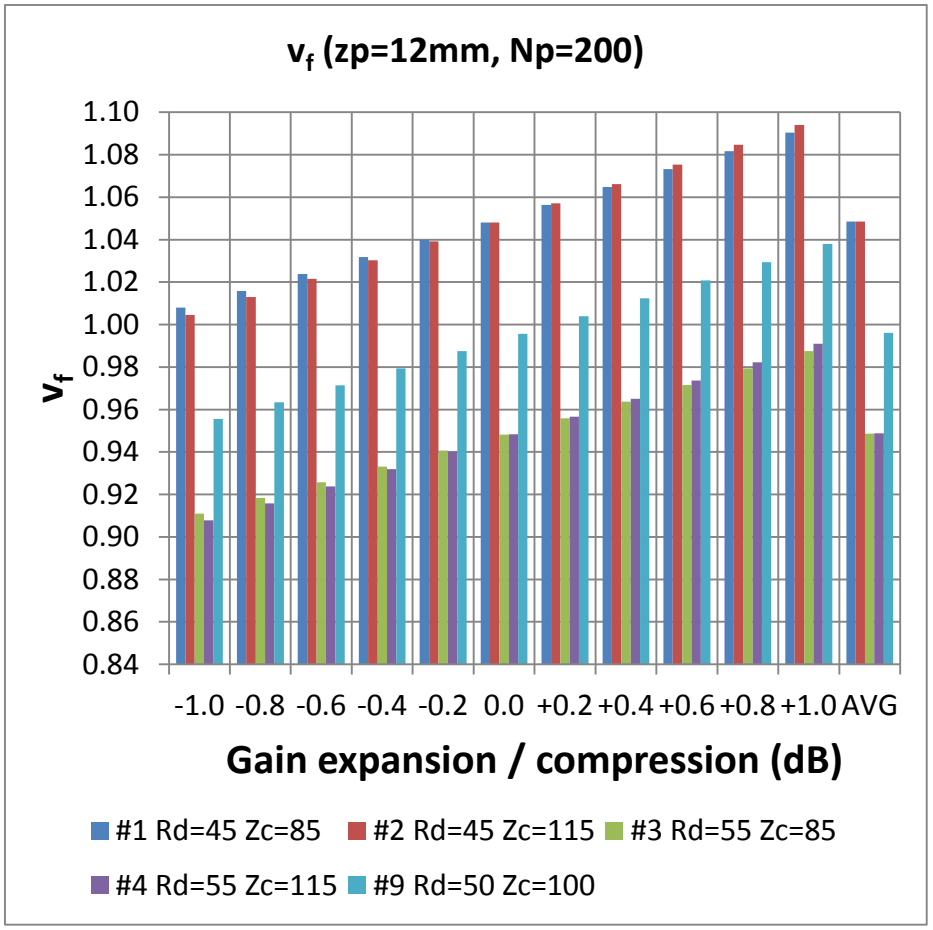
- Non-negligible increase
  - Becaise a longer fitted pulse captures more long-term ISI

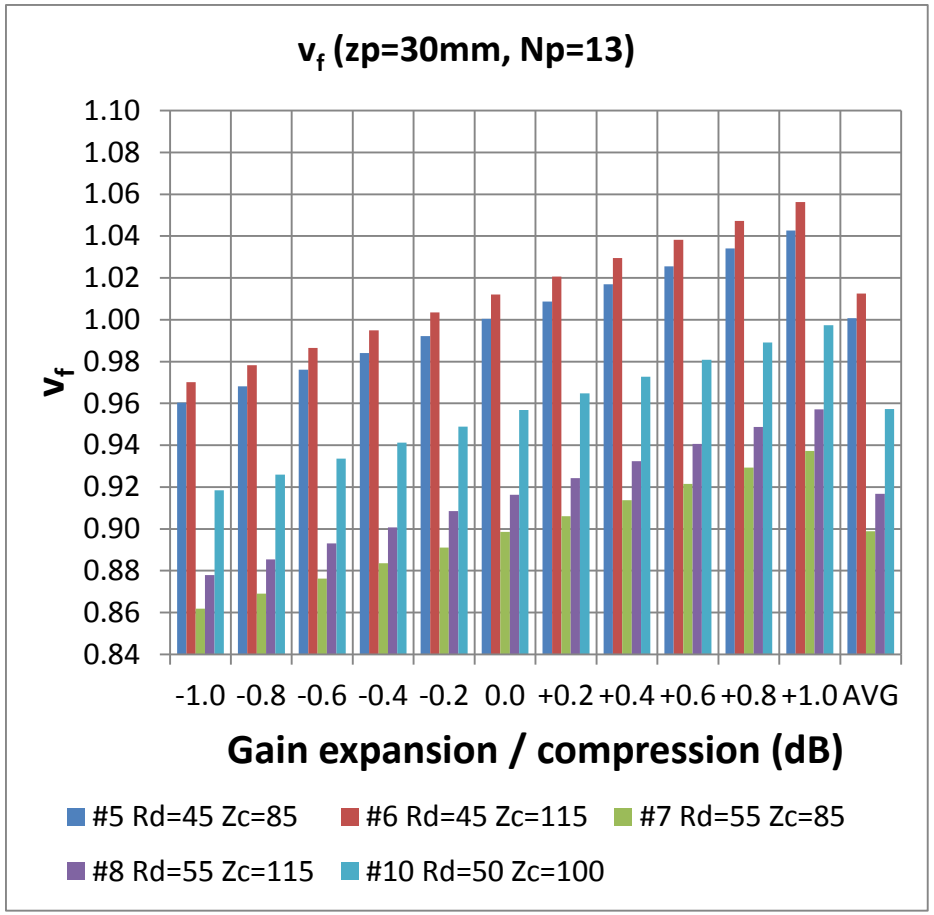


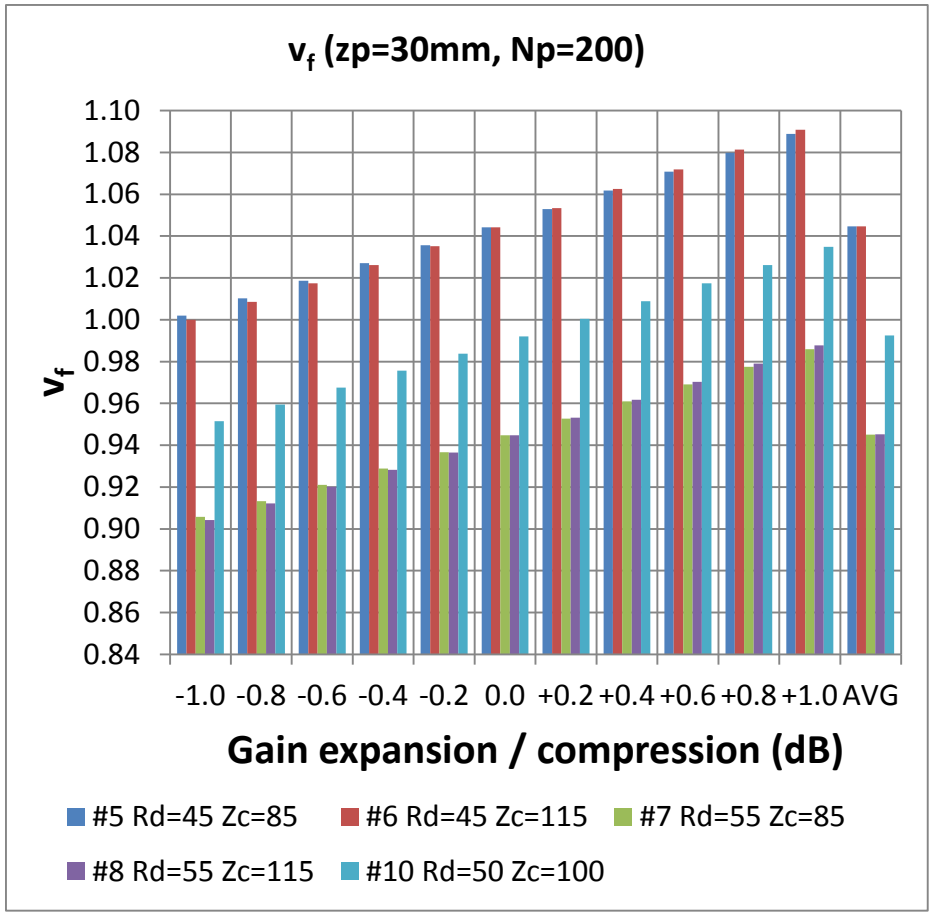


Steady-State Voltage v_f (zp=30mm)

FUJITSU

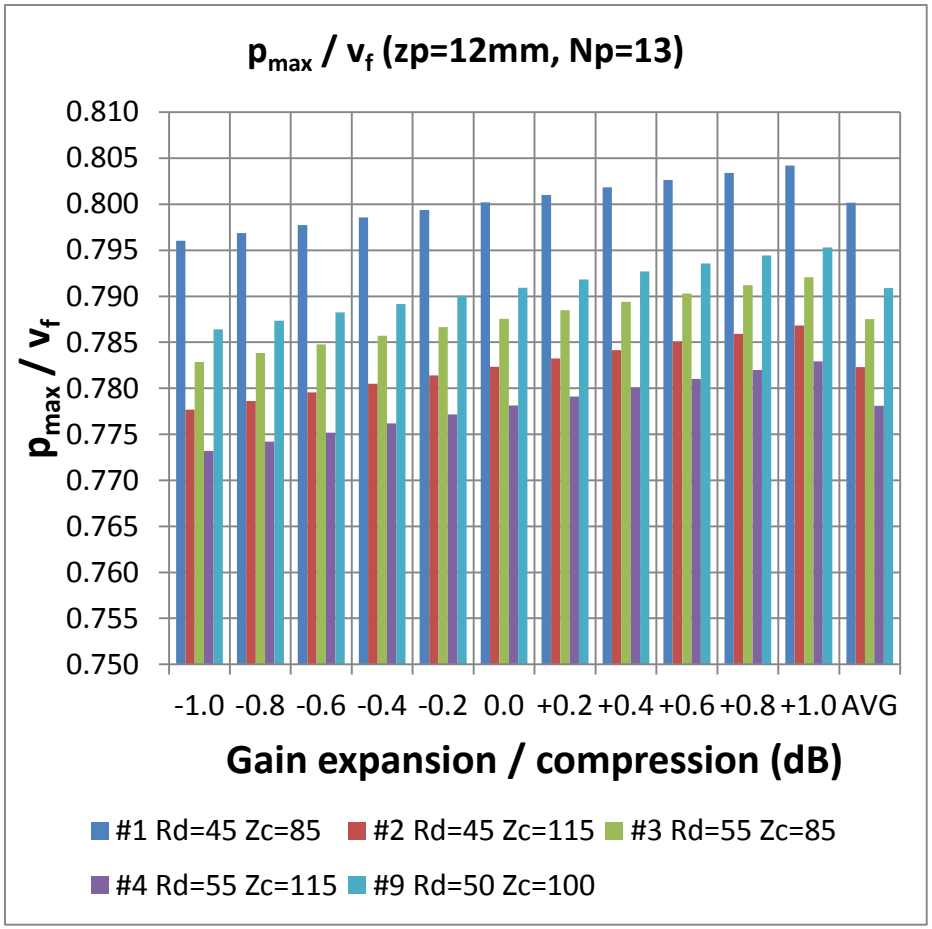
- Non-negligible increase
  - Becaise a longer fitted pulse captures more long-term ISI

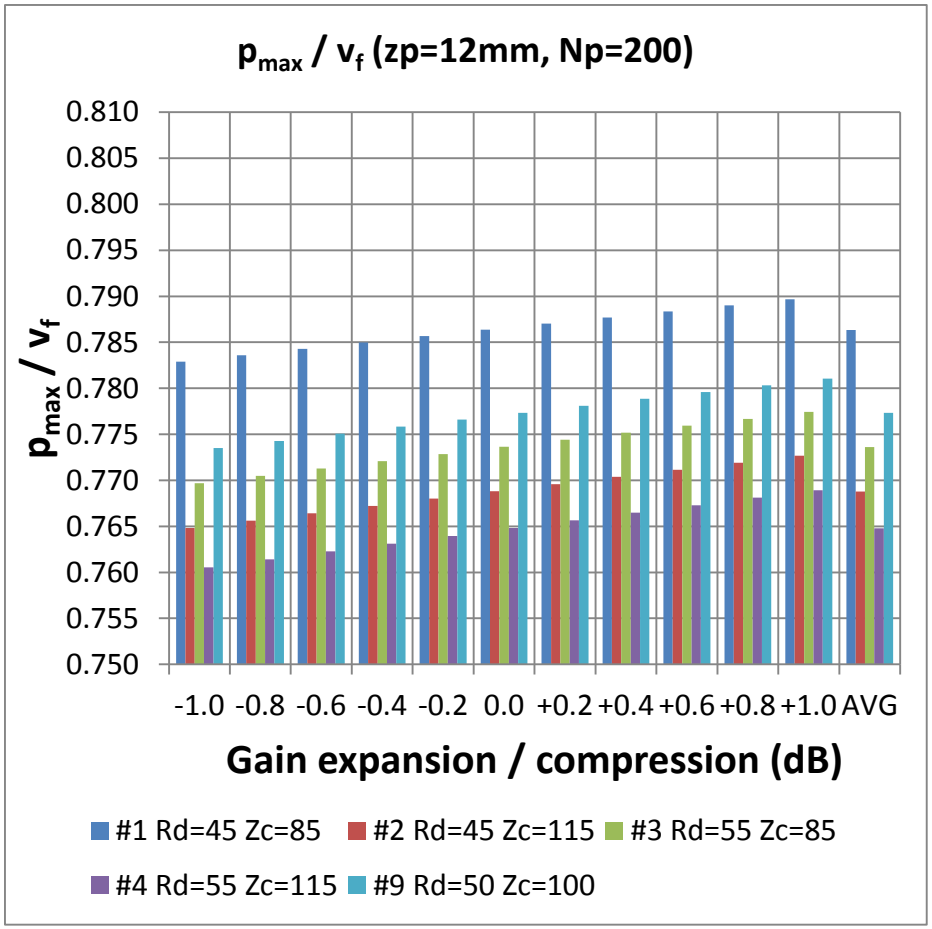




Ratio of p_{max} to v_f (zp=12mm)

- Reduced a lot
  - Because v_f increases while p_{max} does not change





Ratio of p_{max} to v_f (zp=30mm)

- Reduced a lot
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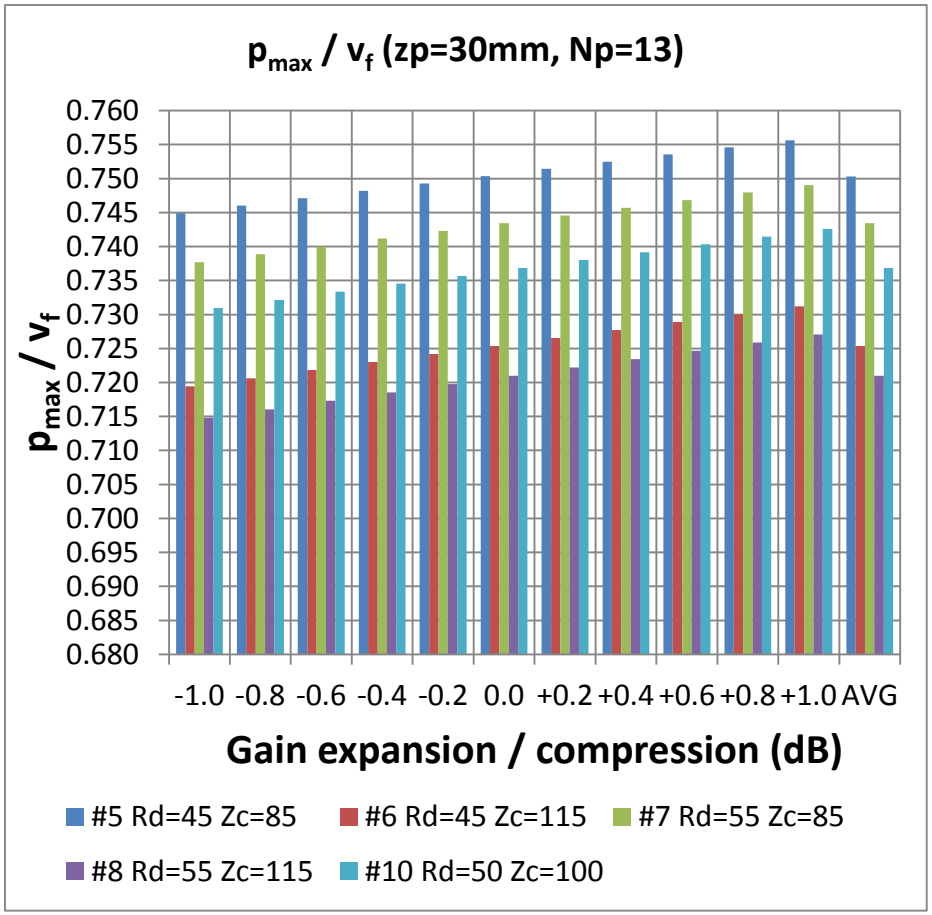
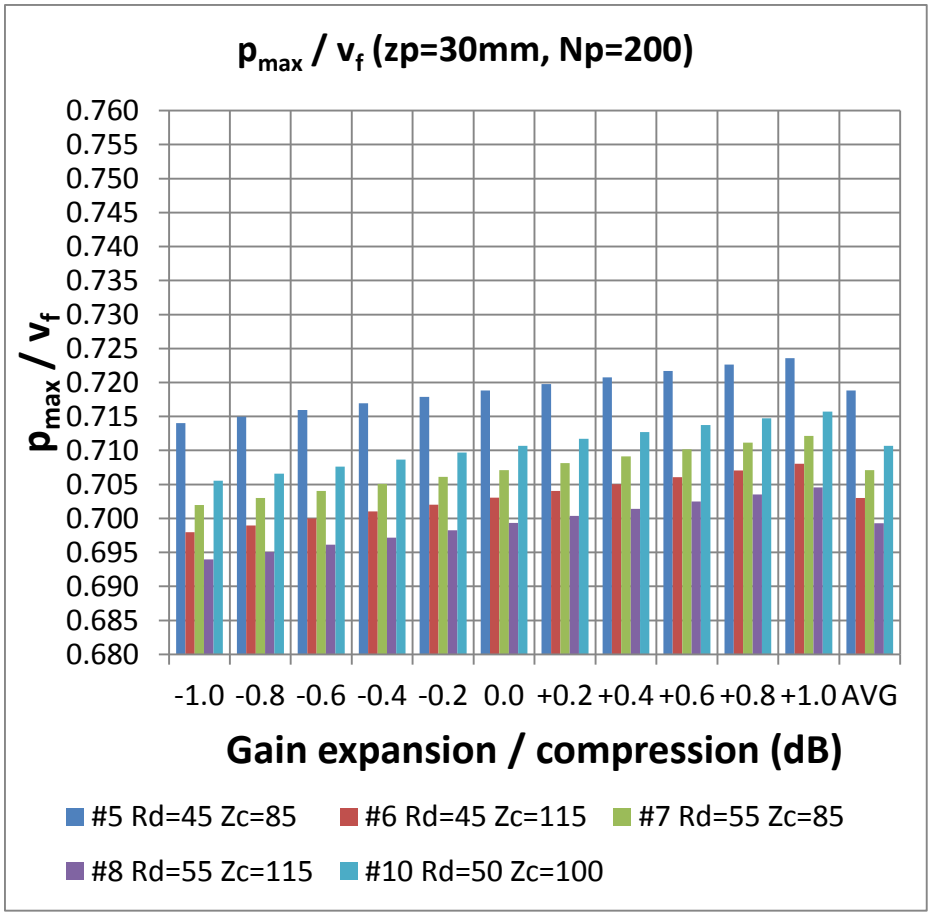
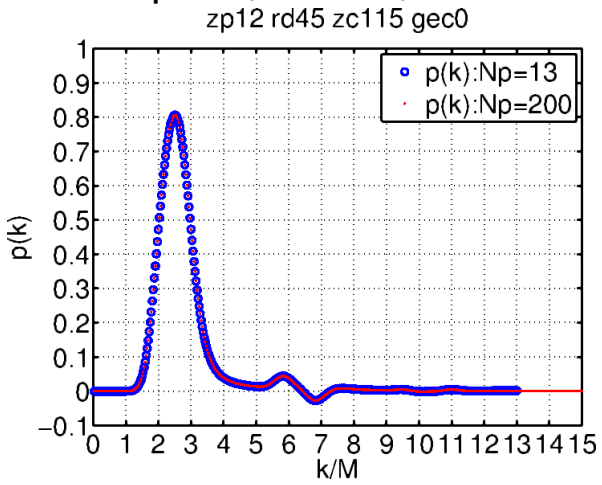




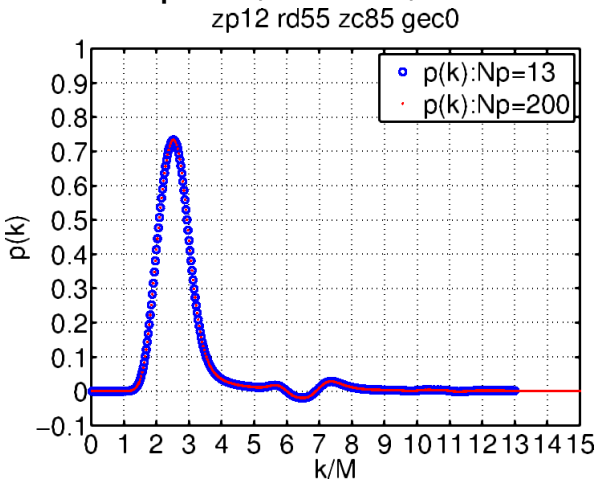
Linear Fit Pulse p(k)

- p(k) does not change for k ≤13*M between Np=13 and Np=200

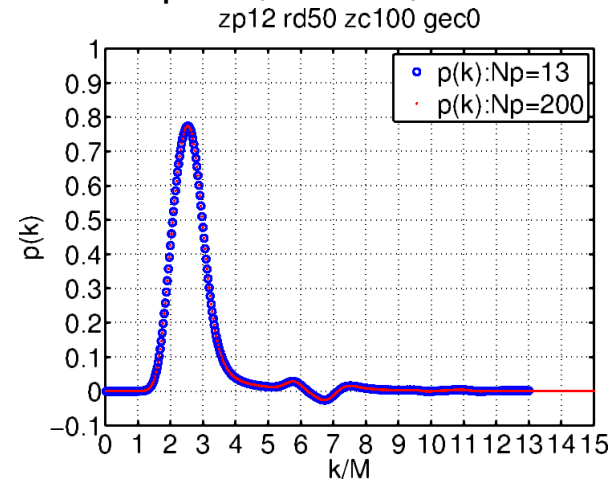
#2: Zp=12, Rd=45, Zc=115



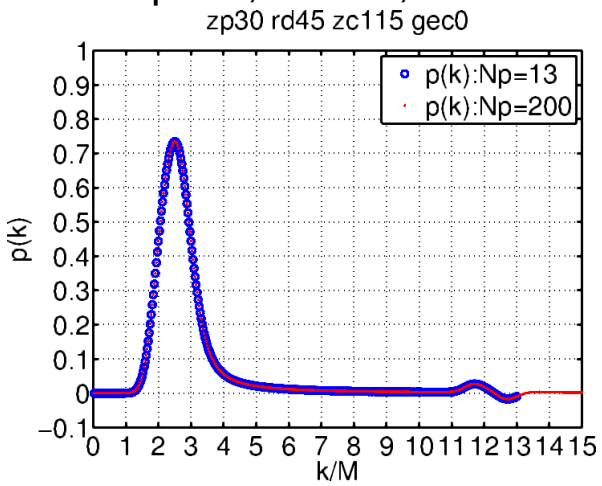
#3: Zp=12, Rd=55, Zc=85



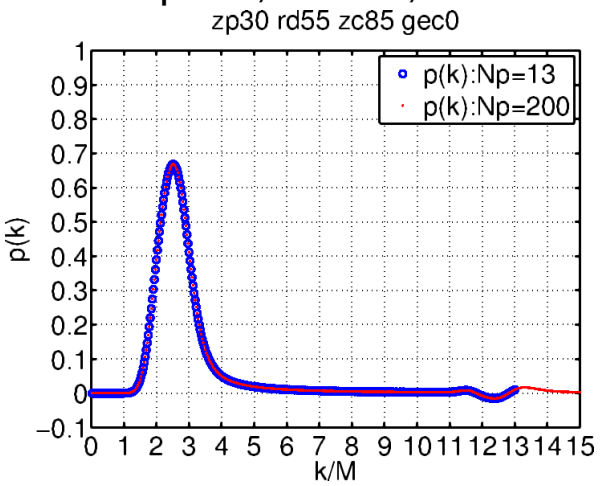
#9: Zp=12, Rd=50, Zc=100



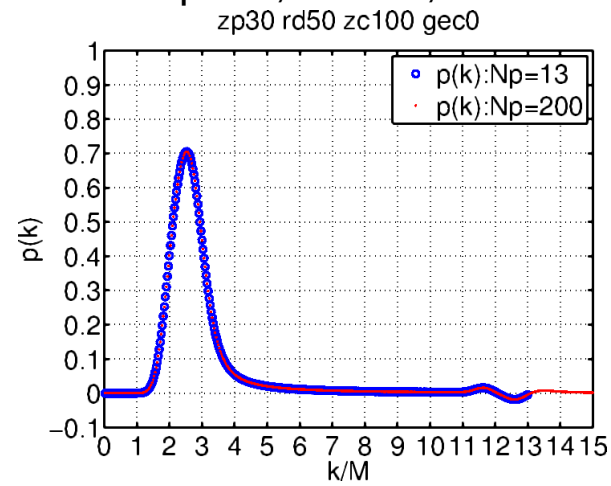
#6: Zp=30, Rd=45, Zc=115



#7: Zp=30, Rd=55, Zc=85



#10: Zp=30, Rd=50, Zc=100



Linear Fit Pulse p(k) (zoomed)

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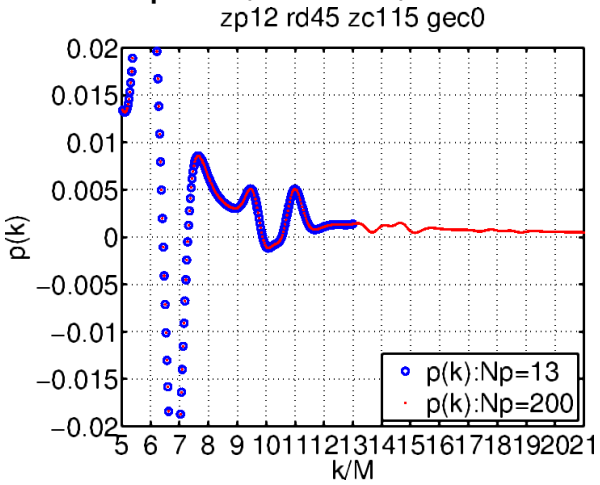
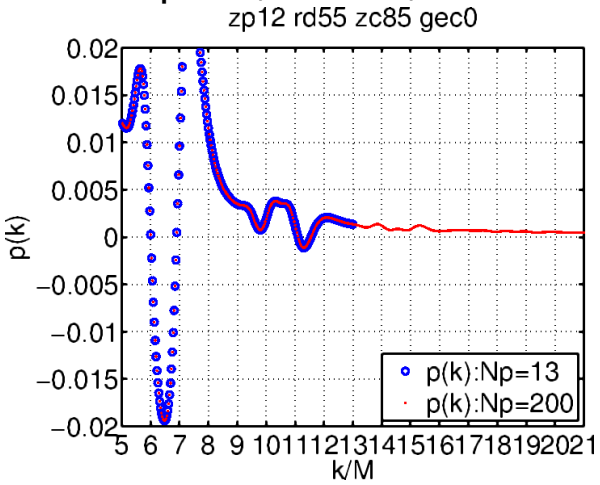
- p(k) does not change for k ≤13*M between Np=13 and Np=200

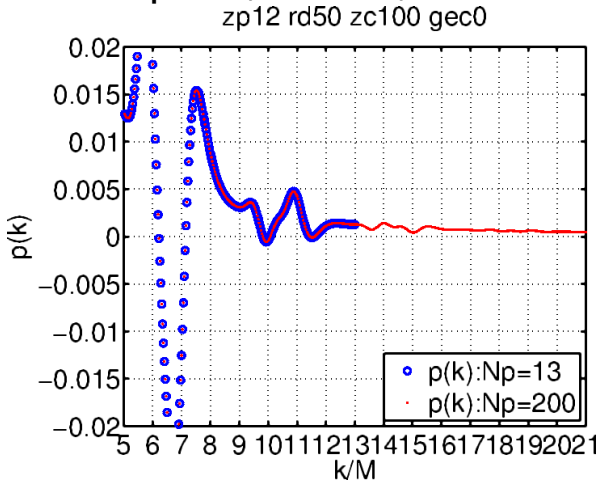
#2: Zp=12, Rd=45, Zc=115



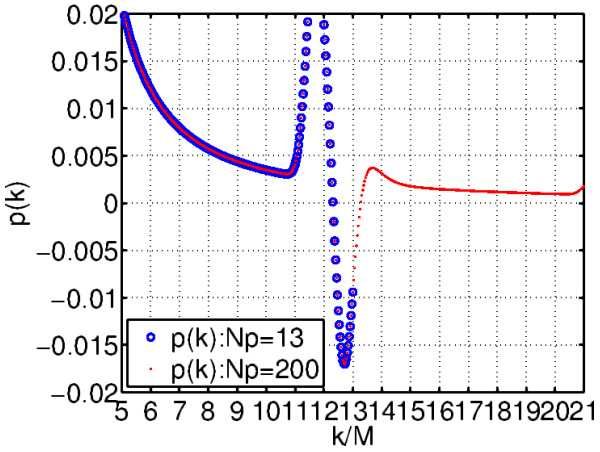
#3: Zp=12, Rd=55, Zc=85



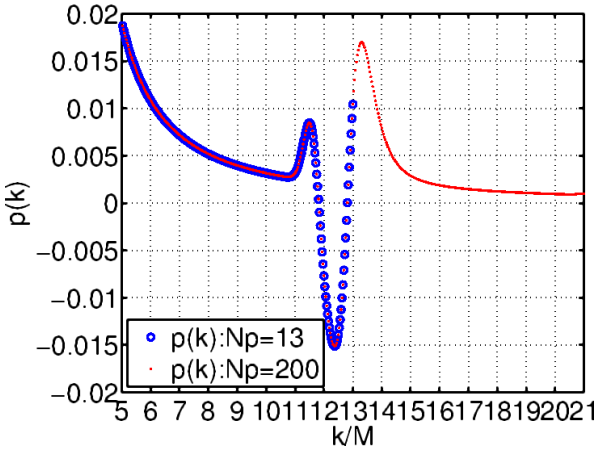
#9: Zp=12, Rd=50, Zc=100



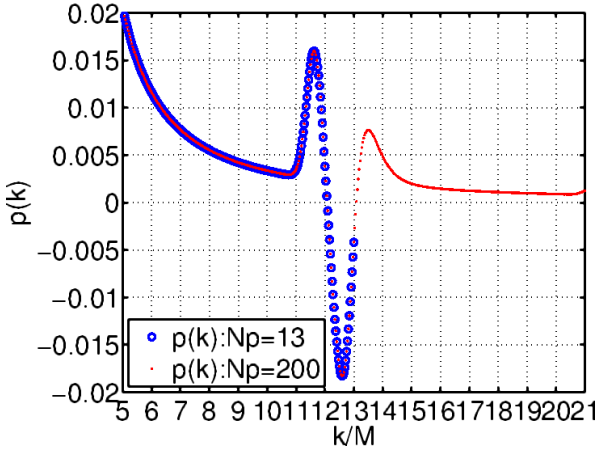
#6: Zp=30, Rd=45, Zc=115



#7: Zp=30, Rd=55, Zc=85



#10: Zp=30, Rd=50, Zc=100



Revised Simulation Results

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#	Description	TF	TF IL @ 12.89GHz	Np	vf	pmax (min)	Av, Afe, Ane	zp	Rd	Zc
1	Old spec (min)		1.2~1.6dB	13	0.4V (min)	0.736 * vf	0.45V	30mm		
2	Old spec (max)		1.2~1.6dB	13	0.6V (max)		0.63V	12mm		
3	Check old spec	B	1.5770dB	13	0.4V (min)	0.738102 * vf	0.44914V	30mm	55Ω	85Ω
4			1.5770dB	13	0.6V (max)		0.64446V	12mm	55Ω	85Ω
5	Check old spec	A	1.4049dB	13	0.4V (min)	0.743455 * vf	0.44519V	30mm	55Ω	85Ω
6			1.4049dB	13	0.6V (max)		0.64415V	12mm	55Ω	85Ω
7	Revised spec with anchored Av	A	1.4049dB	200	0.4206V (min)	0.707112 * vf	0.44519V	30mm	55Ω	85Ω
8			1.4049dB	200	0.6108V (max)		0.64415V	12mm	55Ω	85Ω
9	Revised spec with anchored vf	A	1.4049dB	200	0.4V (min)	0.707112 * vf	0.42342V	30mm	55Ω	85Ω
10			1.4049dB	200	0.6V (max)		0.63275V	12mm	55Ω	85Ω

- Test Fixture
  - A: Reference Insertion Loss EQ93-1 with minimum phase and Zdiff=100Ω
  - B: 38mm Host PCB trace (Zdiff=109.8Ω) using EQ93A-13,14 with Table 92-12
- #3~#10 are simulated with Cd=280fF, Cp=110fF, Gaussian Filter (Tr=13ps) and 4-th order Bessel-Thomson LPF with 33GHz 3dB bandwidth

Conclusion

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- Suggested remedy of comment #41 updated w/ correct parameters (changes based on simulation results #7 and #8)
  - Change the Steady state voltage v_f (max) from 0.6 V to 0.611 V
  - Change the Steady state voltage v_f (min) from 0.4 V to 0.421 V
  - Change the Linear fit pulse peak (min) from 0.736 x v_f to 0.707 x v_f
  - Update the following COM parameters
    - Av and Afe from 0.45V to 0.445V
    - Ane from 0.63V to 0.644V

- Or, another remedy based on simulation results #9 and #10
  - Change the Linear fit pulse peak (min) from 0.736 x v_f to 0.707 x v_f
  - Change Av and Afe from 0.45V to 0.423V
  - Change Ane from 0.63V to 0.633V
    - Keep v_f (max) as 0.6V and v_f (min) as 0.4V

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Thank you