Four lane interleaving and SSPRQ

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Introduction

ghiasi_3bs_01_0317 proposes to rely on the SSPRQ test pattern to verify that CDRs can cope with the clock content issue outlined in anslow_01_121916_elect.

The plots in ghiasi_3bs_01_0317 to compare SSPRQ with the offset clock curves were formed by showing two charts from different presentations on the same page, which makes it difficult to compare the distributions.

This contribution adds the SSPRQ characteristic to the four plots with shifted clock from anslow_01_121916_elect.

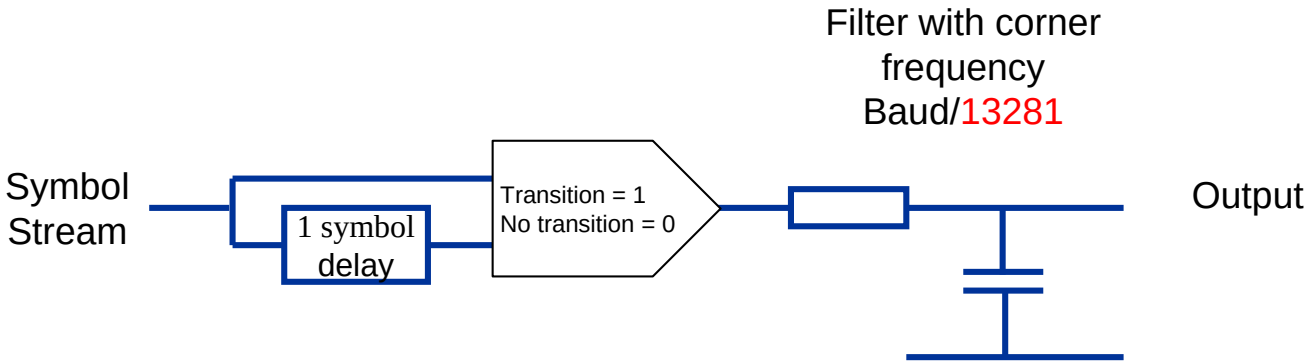
Clock content

The “clock content” parameter is defined here as:

Create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/13281.

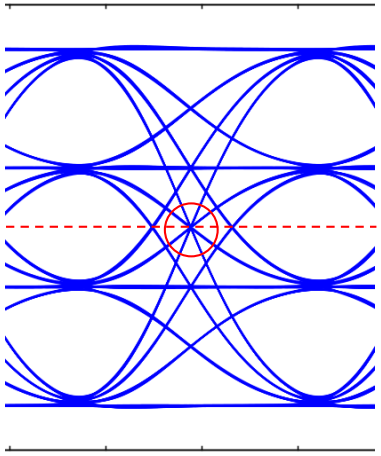
This analysis defines a transition as one of three possibilities (as per healey_3bs_01_1115):

- Symmetrical transitions through the signal average
- Transitions through the signal average
- All transitions

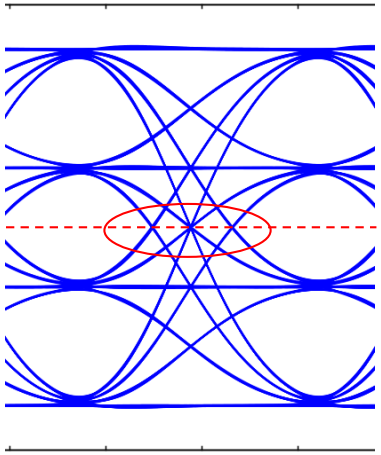


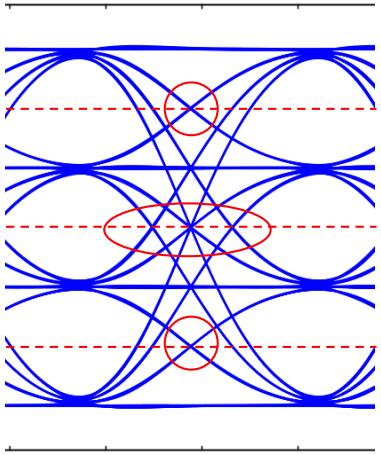
Clock content illustration

Symmetrical transitions through the signal average



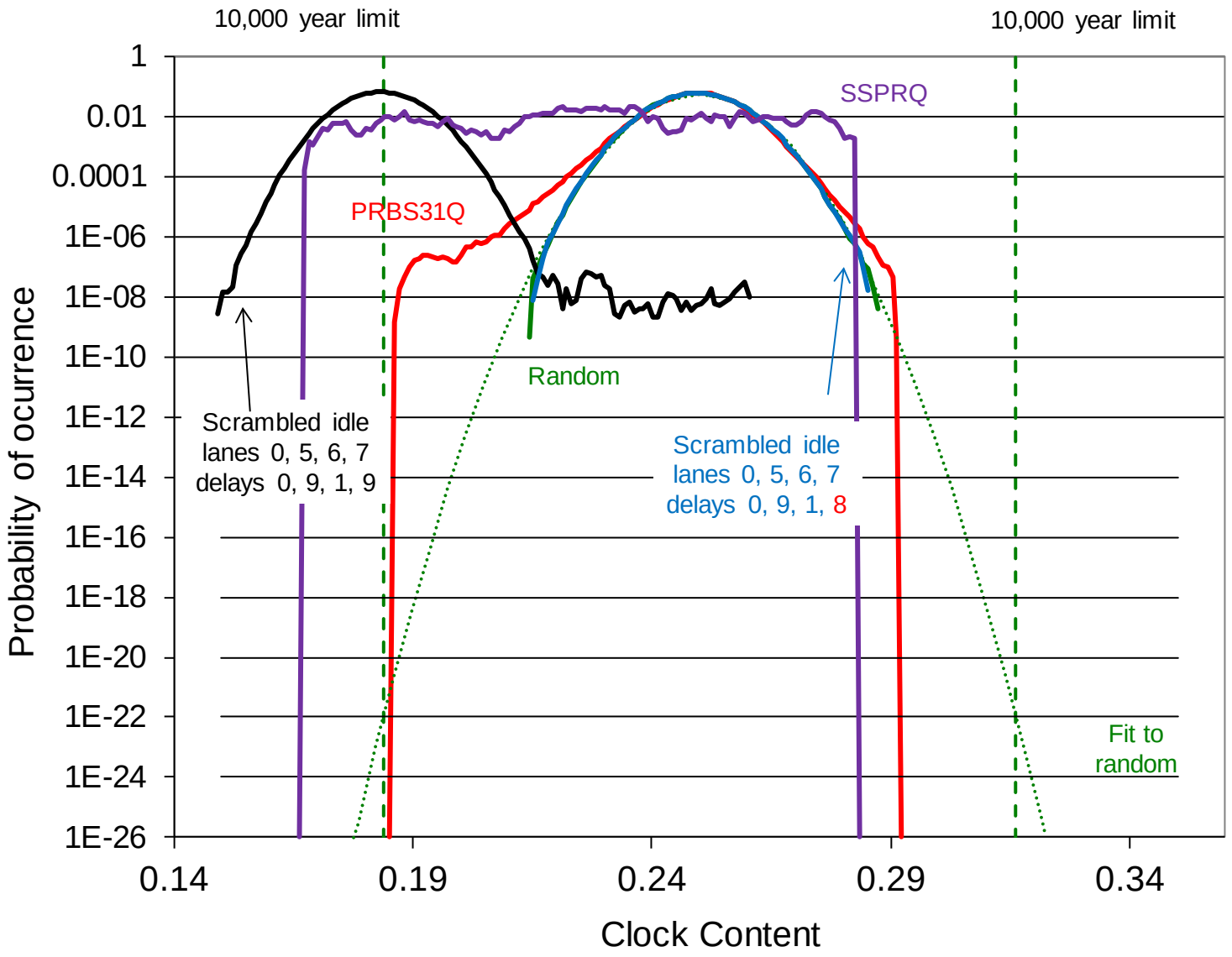
Transitions through the signal average



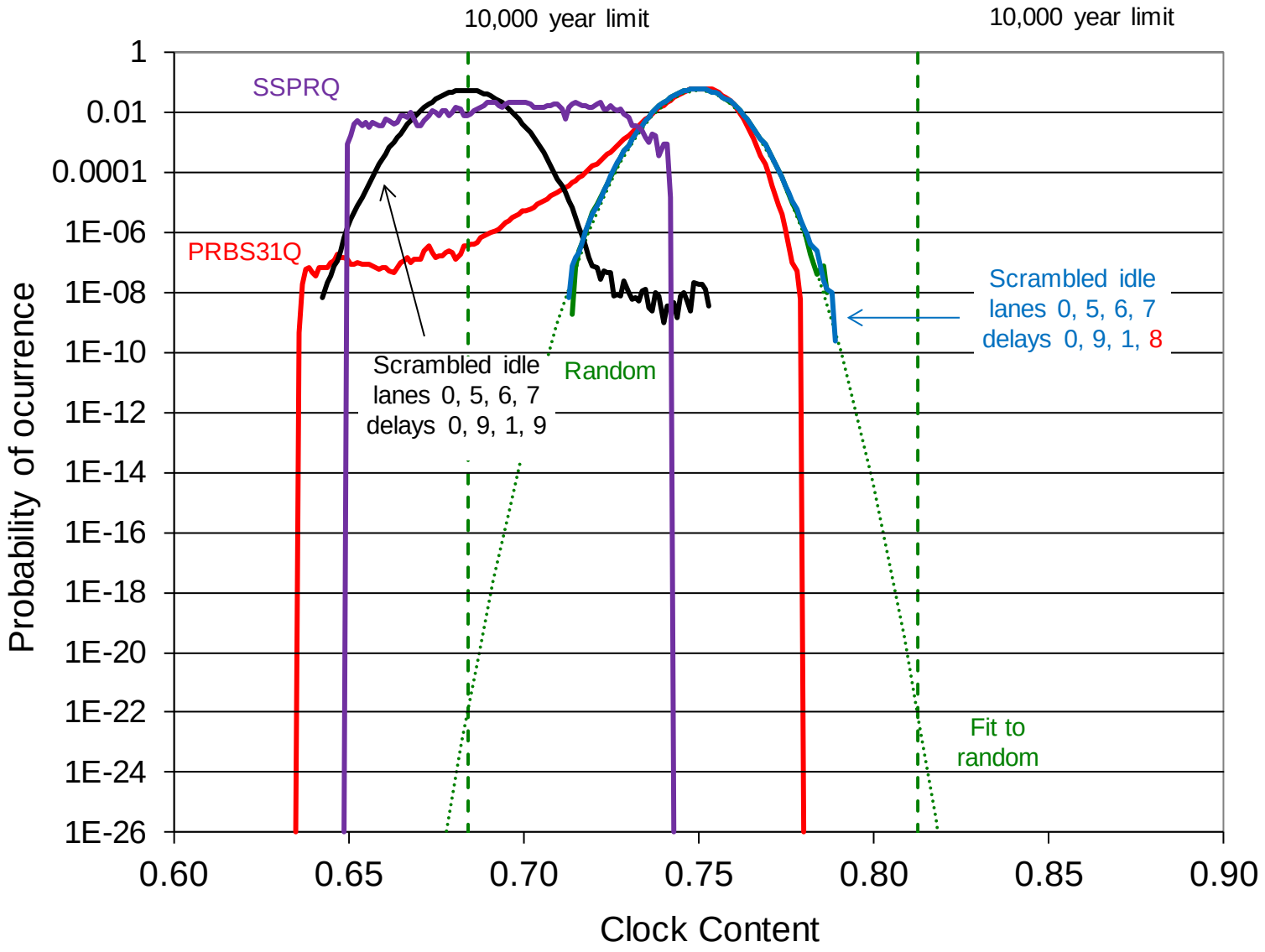


All transitions

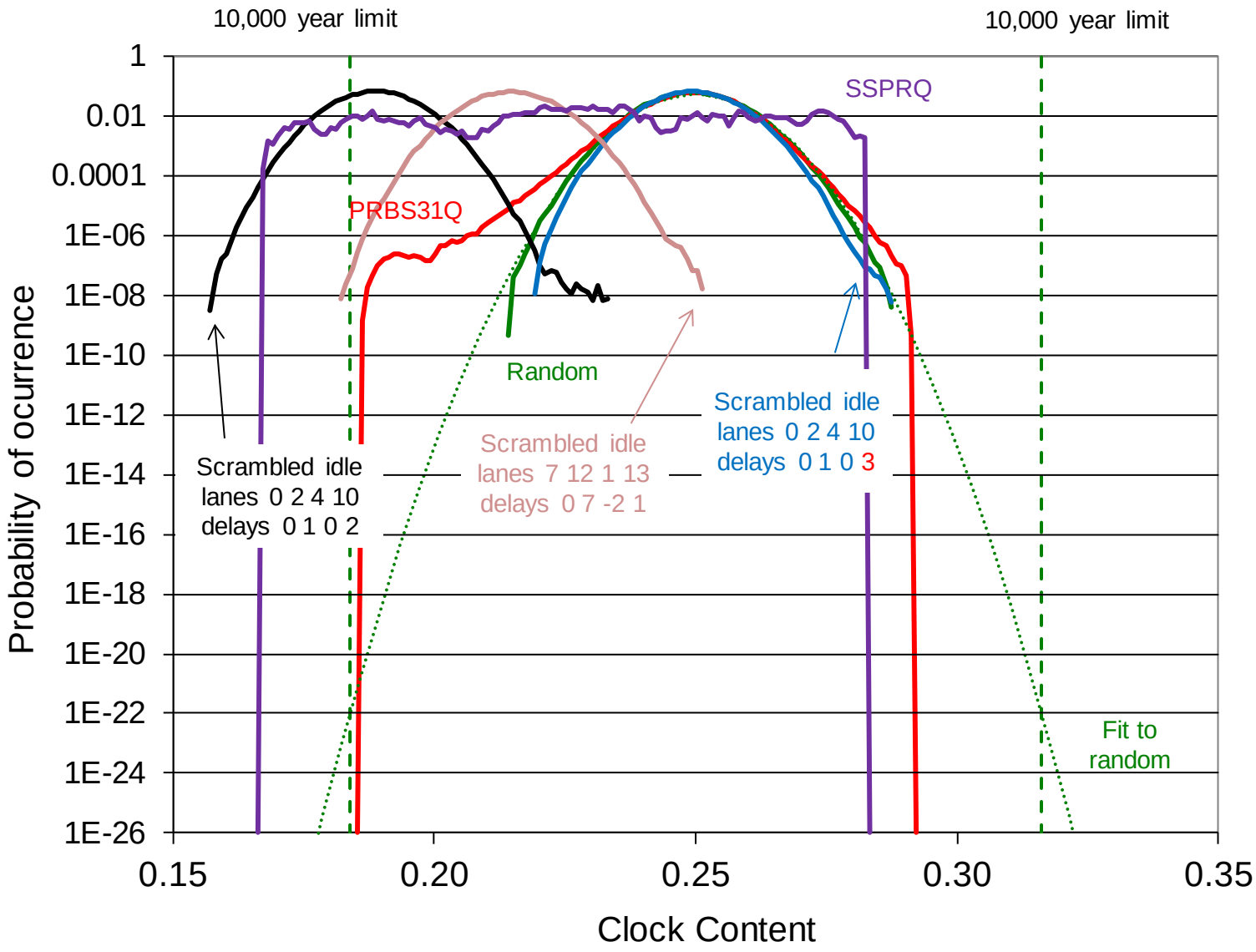
200GbE clock, sym trans through ave, 0, 5, 6, 7



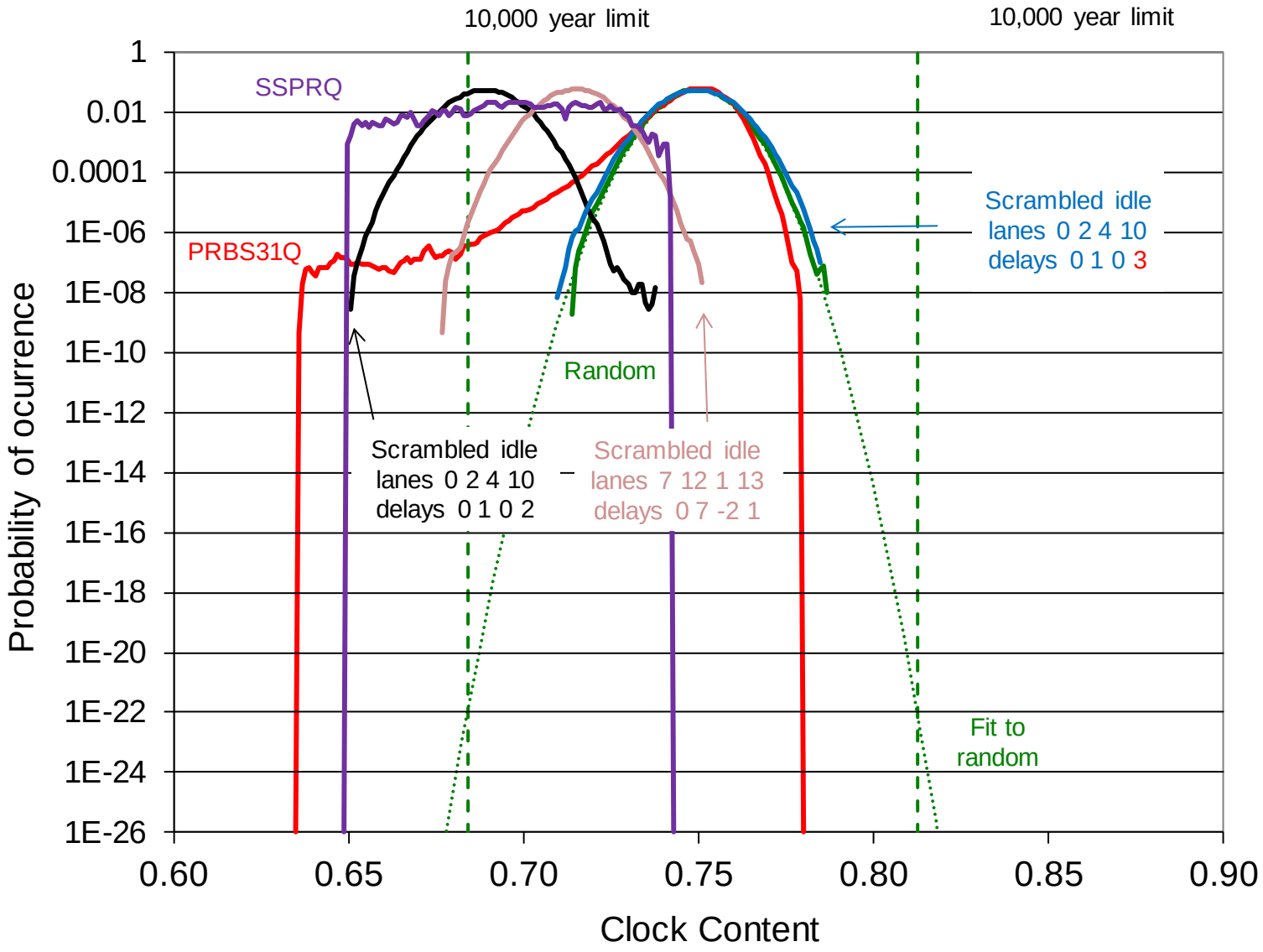
200GbE clock, all transitions, 0, 5, 6, 7



400GbE clock, sym trans through ave, 0, 2, 4, 10



400GbE clock, all transitions, 0, 2, 4, 10



Thanks!