Chip to Module simulations and the effect of crosstalk.

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Introduction

- This presentation explores the difference between ADS simulation and COM on a chip to module link with and without crosstalk and other impairments.
- The loss of the long package and host PCB traces used in COM are concatenated with a measured mated test fixture file which includes crosstalk. Initial results are presented with no other degradations in the Tx and package and PCB traces.
- Further results are presented showing the effect of various impairments including Tx noise, package model capacitances and package and board impedance variations.
- This is a follow on to two presentations at the March 6th 2017 Electrical Ad-Hoc. This presentation includes some corrections and clarifications. Significant differences are that it was realized that 5ps risetime (not 8ps) had been used for the ADS simulations so COM simulations were changed to 5ps to match. Also the FIR in COM was changed to a 3-tap FIR as had been used in ADS (except for the COM optimized setting comparisons.)

Methodology and details.

- **Characterize ADS PAM4 driver to ensure the Tx used in COM is the same**
  - 0.8V voltage swing
  - 5ps 20-80% risetime
- **In ADS, sweep TX FIR and CTLE to find optimal eye at BER 1E-5 at scope**

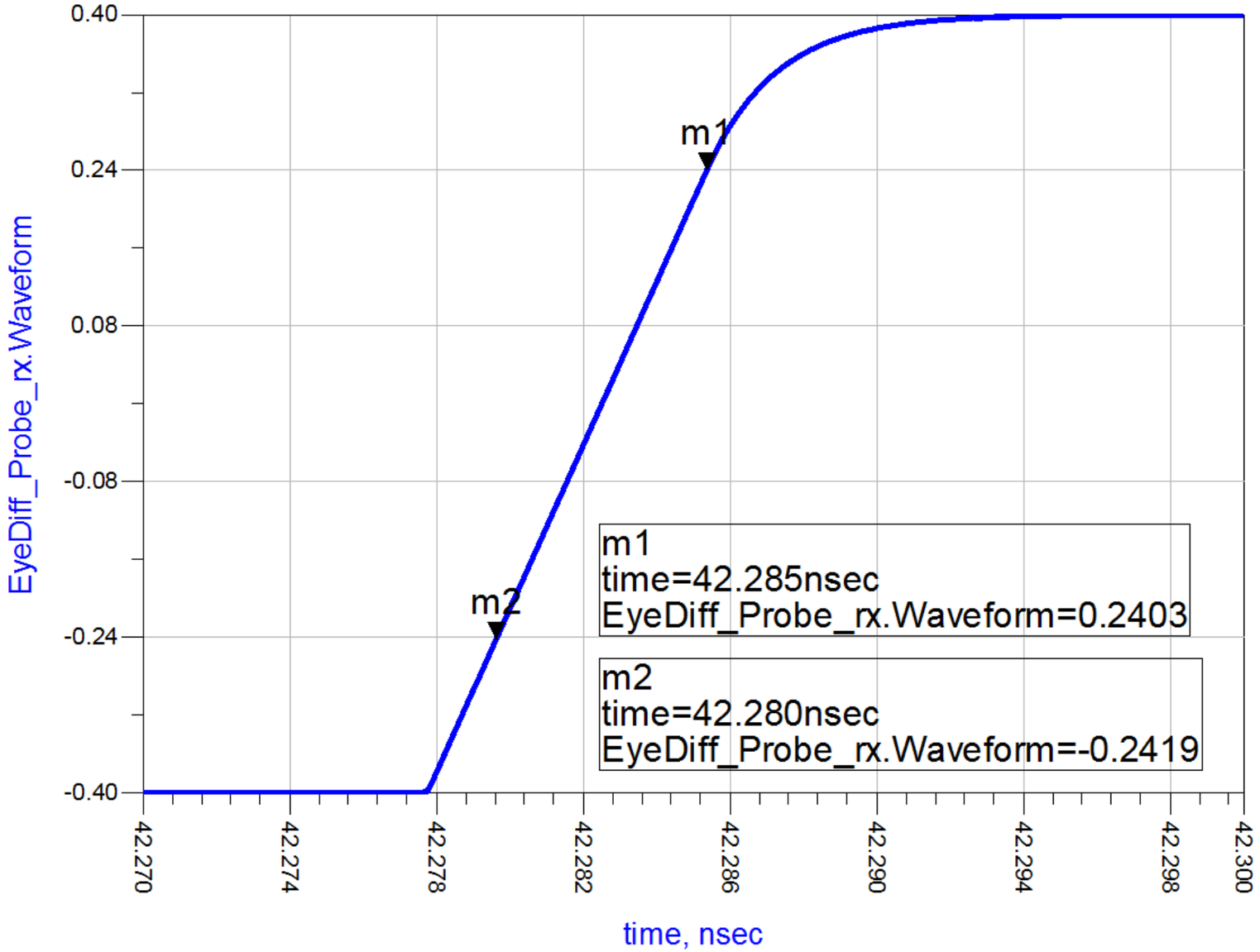
  pre1: -0.15 to 0 with step 0.05

  post1: -0.25 to 0 with step 0.05

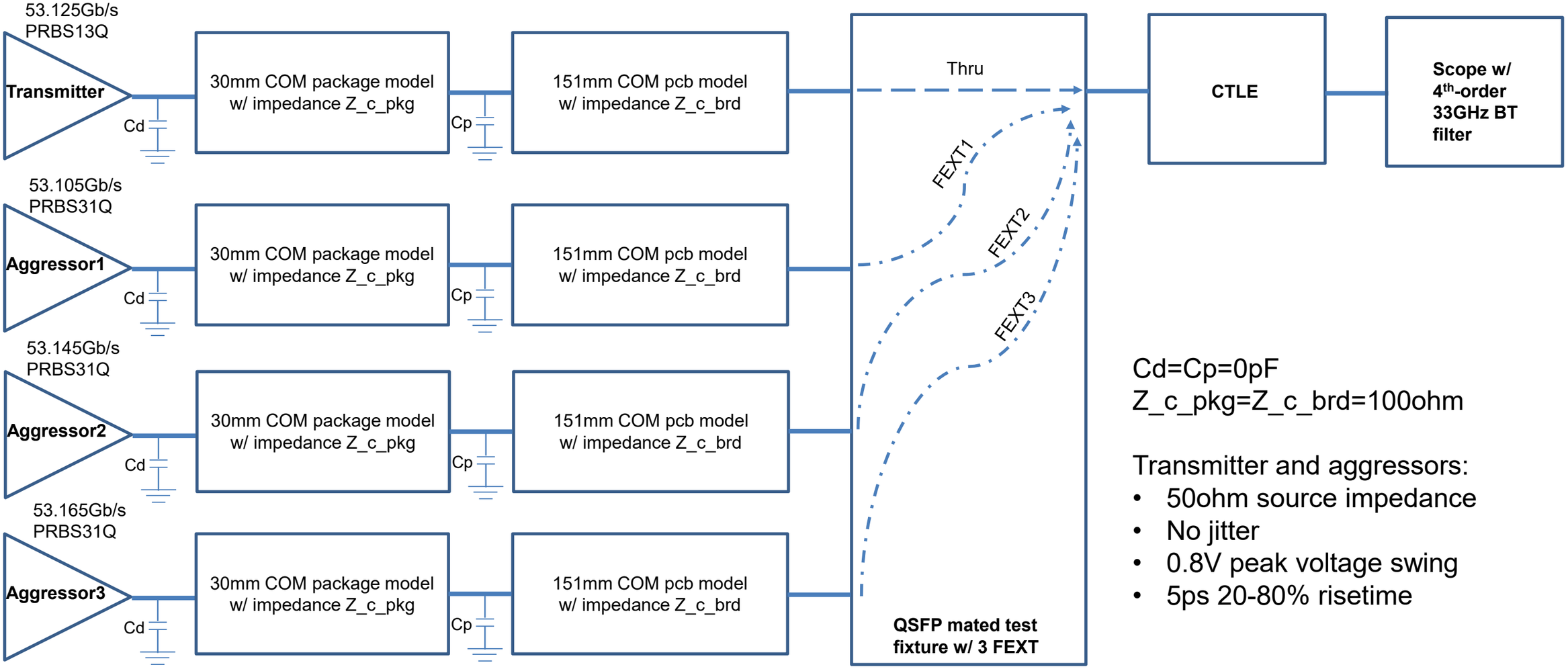
  Optimal in this work is the largest eye amplitude. If eye amplitude*eye width had been chosen as the optimal setting slightly different results would have been obtained.

  CTLE is as defined in 120E.3.1.7 draft 3.0.
- **ADS simulations used bit by bit and simulations used 10^5 bits when not otherwise noted. A comparison for some of the results with 10^7 bits is included showing only minor differences.**
- **All ADS simulation eye height and eye width measurements are from the ADS measurement methodology not the method adopted in the 802.3bs draft.**
- **In ADS eye 0 is the lowest eye, eye 1 is the middle eye and eye 2 is the upper eye.**
- **Simulations were also performed in COM to get eye height (VEO) at BER 1E-5**

AMI driver risetime: 5pS 20-80%



Chip to module block diagram with initial simulation parameters

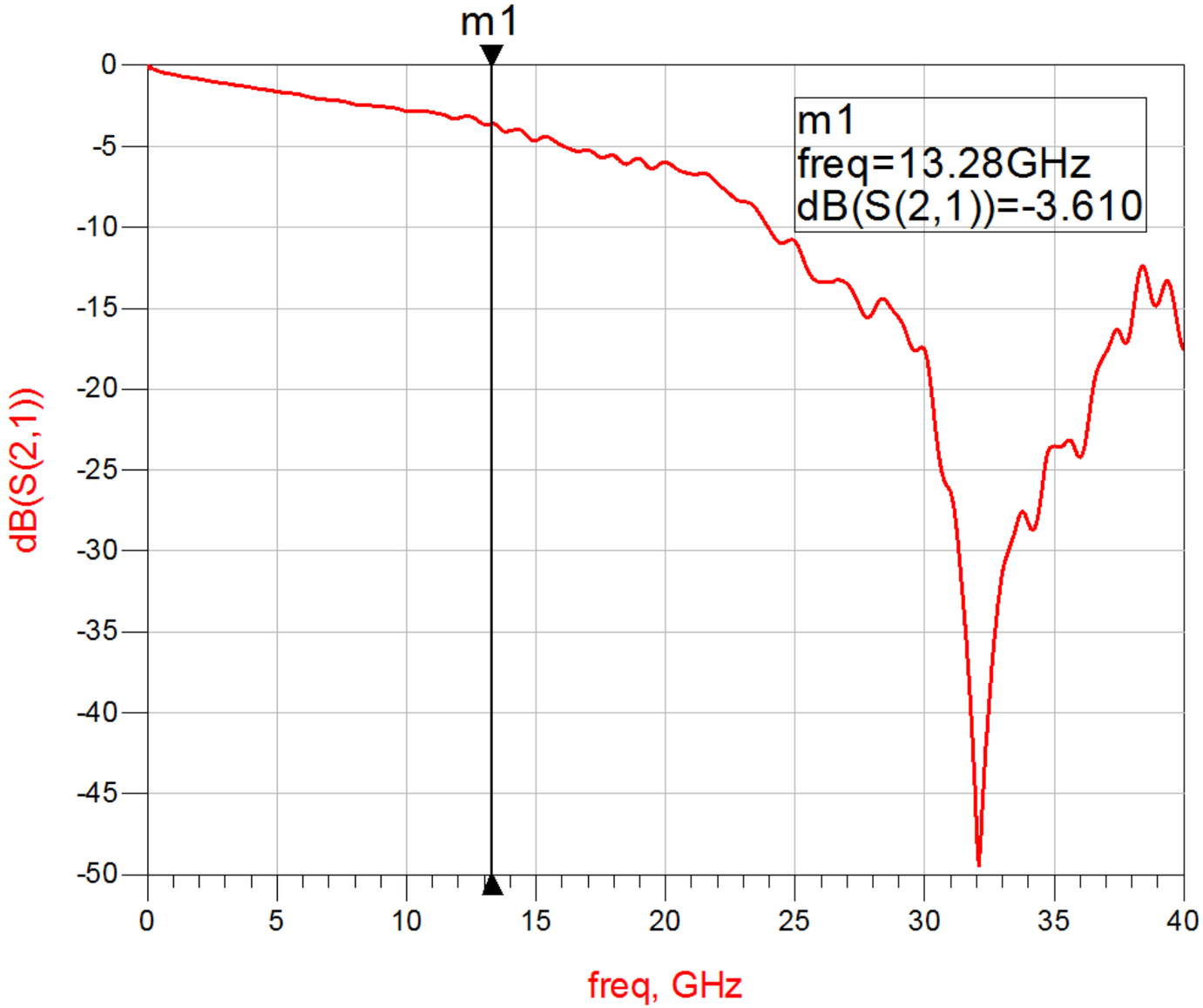


Cd=Cp=0pF
Z_c_pkg=Z_c_brd=100ohm

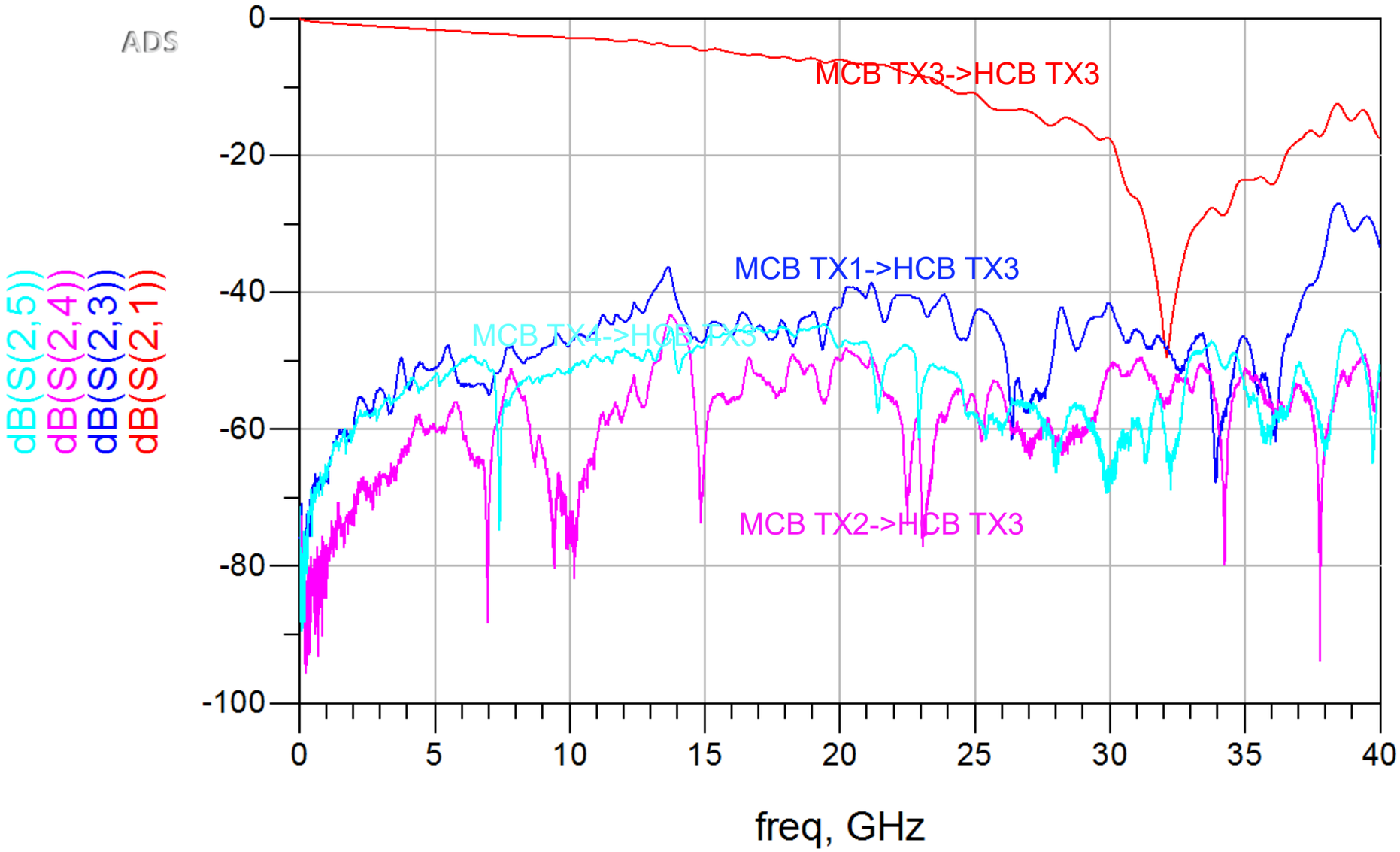
Transmitter and aggressors:

- 50ohm source impedance
- No jitter
- 0.8V peak voltage swing
- 5ps 20-80% risetime

Mated QSFP test fixture insertion loss

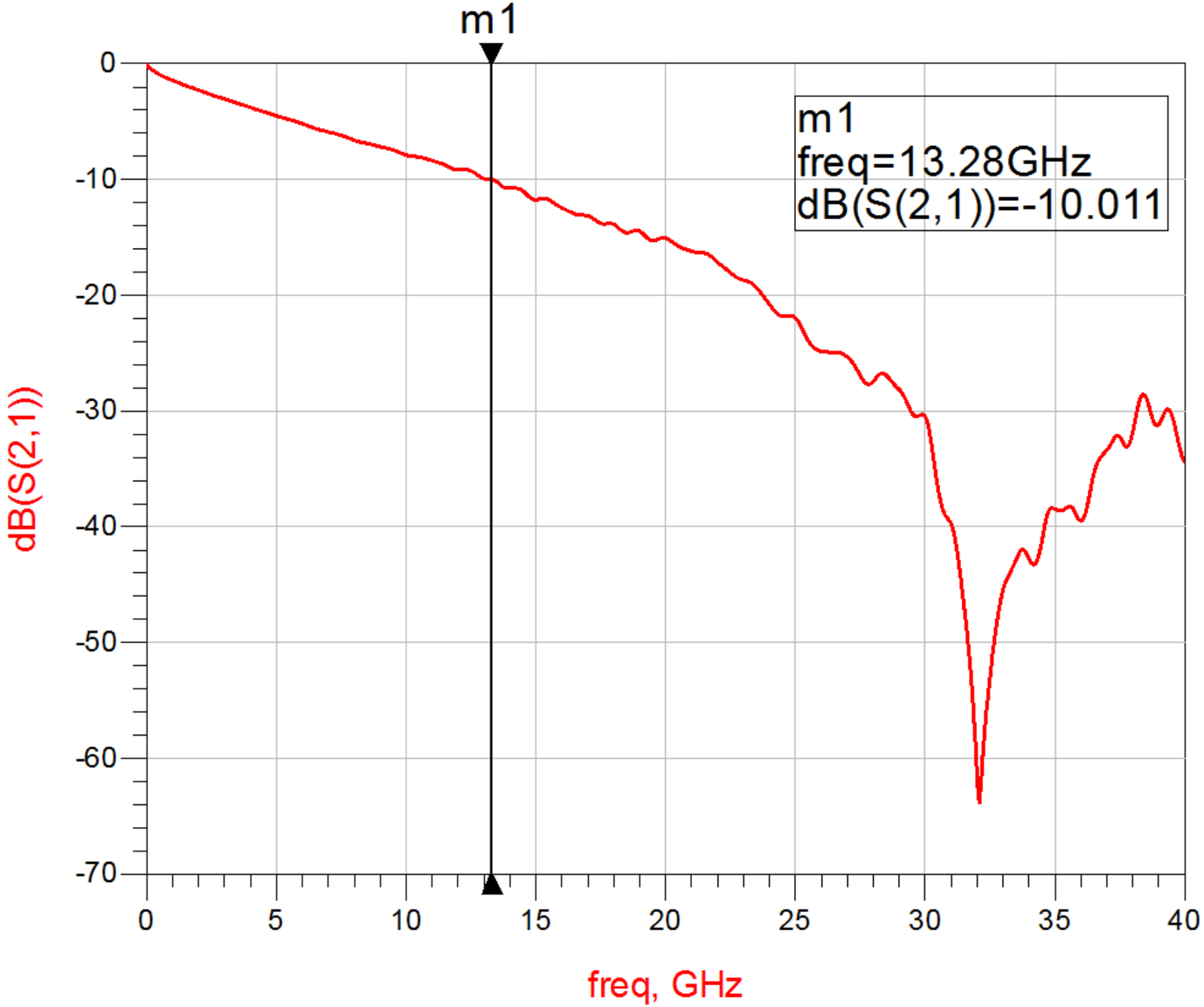


QSFP mated test fixtures THRU and FEXT

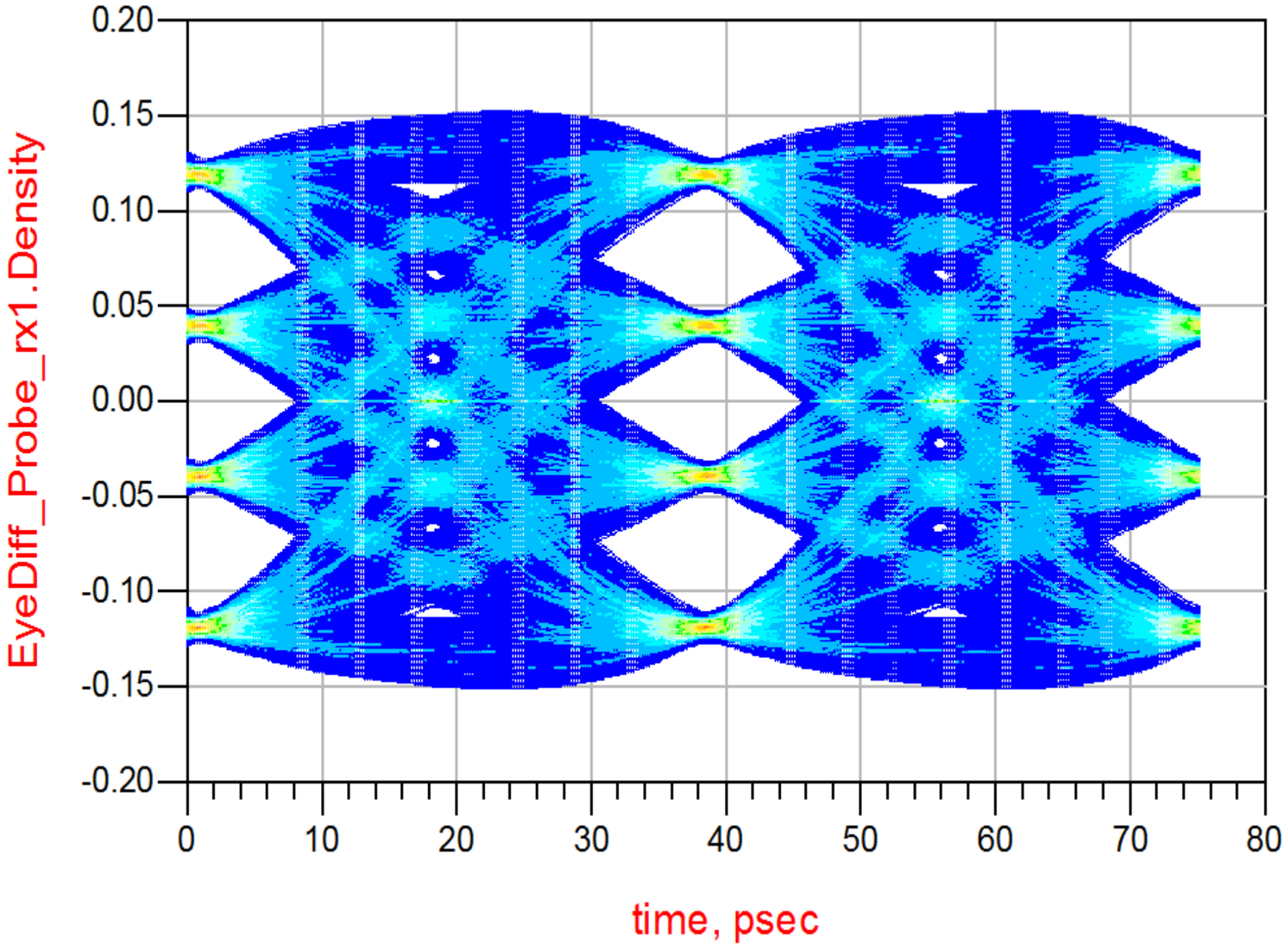


FEXT measured per procedure for mated test boards =2.7mV rms.

151mm 100ohm PCB plus mated QSFP test fixture insertion loss



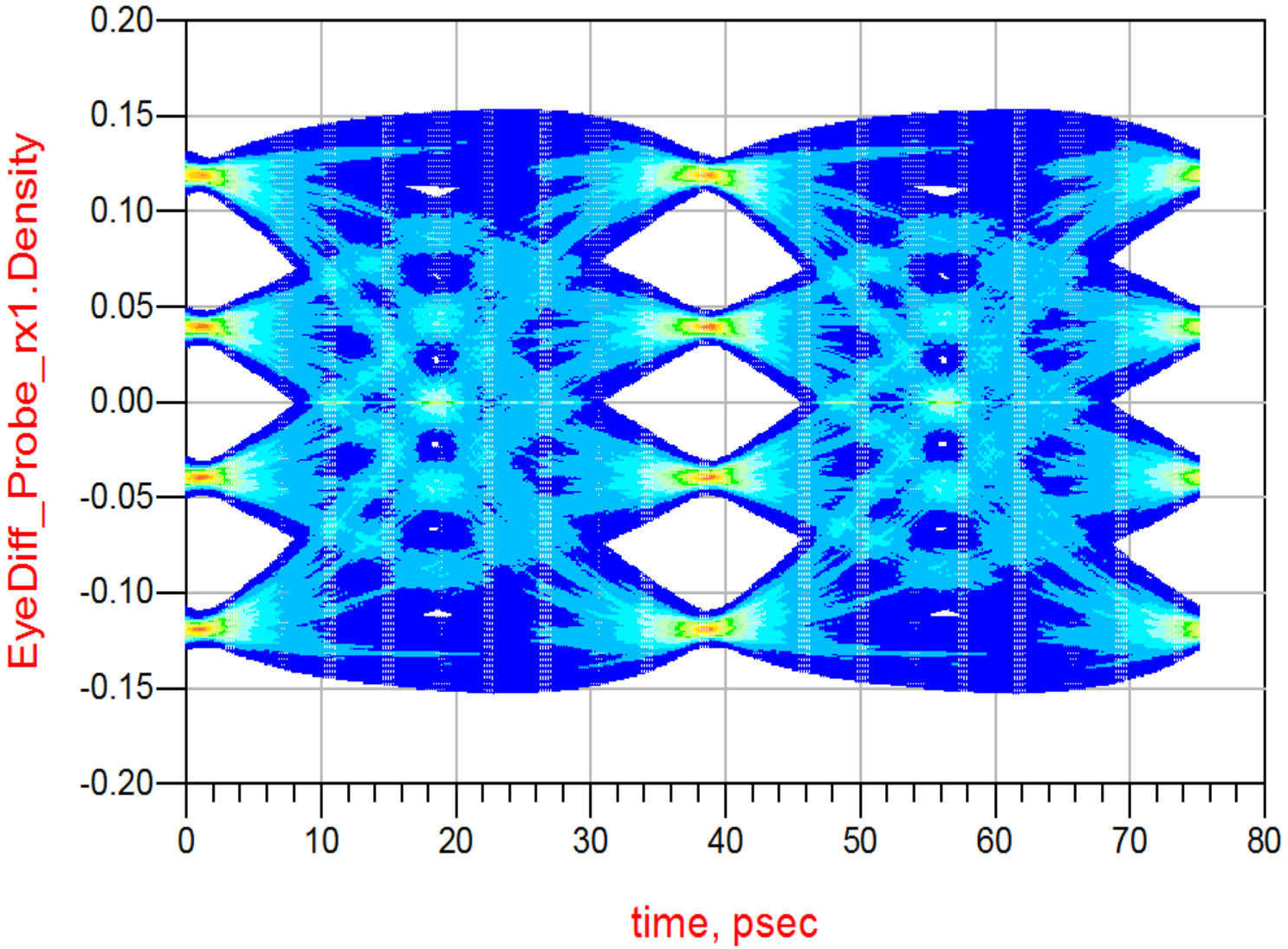
ADS BER 1E-5 eye as measured by “scope” w/o xtalk



measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.506E-11
WidthAtBER1	1.506E-11
WidthAtBER2	1.544E-11
HeightAtBER0	0.064
HeightAtBER1	0.063
HeightAtBER2	0.065

Optimal settings:
FIR: -0.1 0.85 -0.05
CTLE: 6.5dB

ADS BER 1E-5 eye as measured by “scope” w/ xtalk



measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.468E-11
WidthAtBER1	1.468E-11
WidthAtBER2	1.506E-11
HeightAtBER0	0.062
HeightAtBER1	0.061
HeightAtBER2	0.063

Optimal settings:
FIR: -0.1 0.85 -0.05
CTLE: 6.5dB

COM simulation

COM configurations

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0 0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[30]	mm	[test cases]
z_p (NEXT)	[12]	mm	[test cases]
z_p (FEXT)	[30]	mm	[test cases]
z_p (RX)	[0 0]	mm	[test cases]
C_p	[0 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.15:0.05:0]		[min:step:max]
c(-2)	[0]		
c(1)	[-0.25:0.05:0]		[min:step:max]
g_DC	.5 3 3.5 4 4.5 5 5.5 6 6.5 7 7	dB	[min:step:max]
f_z	6.155 5.733 5.353 5.007 4.	GHz	
f_p1	6 15.6 15.6 15.6 15.6 15.6 1	GHz	
f_p2	1 14.1 14.1 14.1 14.1 14.1 1	GHz	
A_v	0.4	V	
A_fe	0.4	V	
A_ne	0.4	V	
L	4		
M	32		
N_b	0	UI	
b_max(1)	0		
b_max(2..N_b)	0		
sigma_RJ	0	UI	
A_DD	0	UI	
eta_0	0.00E+00	V^2/GHz	
SNR_TX	100	dB	
R_LM	1		
DER_0	1.00E-05		
Operational control		1	
COM Pass threshold	3	dB	
Include PCB	1	Value	0, 1
PHY_type	C2M		
EH_min	32	Value	EH limit
EH_max	34	Value	EH limit
f_HP_P	1.2 1.2 1.2 1.2 1.2 1.2 1.2	GHz	
f_HP_Z	1 1.075 1.05 1.025 1 1 1 1	GHz	

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
Display frequency domain	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\C2C_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	c2m_MTF	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	5.00E-03	ns
FORCE_TR	1	logical

Non standard control options		
INC_PACKAGE	1	logical
IDEAL_RX_TERM	1	logical
INCLUDE_CTLE	1	logical
INCLUDE_TX_RX_FILTER	1	logical
COM_CONTRIBUTION	0	logical

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	100	Ohm

Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	151	mm
z_bp (RX)	0	mm

COM results

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```
          code_revision: '1.65'
            config_file: 'eq_qsfp_mtf_jitter_xtalk_0307_row1row2.xls'
             file_names: '"c2m_MTF --A_MCB_P1P3_TX3_tcard_P2P4_TX3"'
                 levels: 4
              Pkg_len_TX: 30
            Pkg_len_NEXT: 12
            Pkg_len_FEXT: 30
              Pkg_len_RX: 0
           baud_rate_GHz: 26.5625
           f_Nyquist_GHz: 13.2813
channel_operating_margin_dB: 14.7807
      peak_interference_mV: 7.3100
peak_channel_interference_mV: 7.3100
            peak_ISI_mV: 7.3100
        peak_uneq_pulse_mV: 189.6184
 peak_MDXTK_interference_mV: 0
peak_MDNEXT_interference_mV: 0
peak_MDFEXT_interference_mV: 0
available_signal_after_eq_mV: 40.0822
   steady_state_voltage_mV: 126.5731
               VEO_mV: 65.5443
        VEO_normalized: 0.8176
               VEC_dB: 1.7489
      equivalent_ISI_ICN: 0
        sci_noise_FD_RMS: 0
         CTLE_zero_poles: [9.2972e+09 1.0000e+09 1.4100e+10 1.5600e+10 1.2000e+09]
         CTLE_DC_gain_dB: -6.5000
              TXLE_taps: [0 -0.1000 0.8500 -0.0500 0 0]
               DFE_taps: [0×1 double]
        cci_noise_TD_BER: 0
  peak_interference_at_BER: 0.0073
                   FOM: 26.1098
              DFE4_RSS: 0
              DFE2_RSS: 0
```

No xtalk

```
com_ieee8023_93a_165('eq_qsfp_mtf.xls', 0, 0,
'A_MCB_P1P3_TX3_tcard_P2P4_TX3.s4p')
```

```
          code_revision: '1.65'
            config_file: 'eq_qsfp_mtf_jitter_xtalk_0307_row1row2.xls'
             file_names: '"c2m_MTF --A_MCB_P1P3_TX3_tcard_P2P4_TX3,c2m_MTF --MCB_P1P3_TX1_HCB_P2P...
                 levels: 4
              Pkg_len_TX: 30
            Pkg_len_NEXT: 12
            Pkg_len_FEXT: 30
              Pkg_len_RX: 0
           baud_rate_GHz: 26.5625
           f_Nyquist_GHz: 13.2813
annel_operating_margin_dB: 14.0736
      peak_interference_mV: 7.9300
k_channel_interference_mV: 7.9300
            peak_ISI_mV: 7.3100
        peak_uneq_pulse_mV: 0.4301
eak_MDXTK_interference_mV: 2.4400
ak_MDNEXT_interference_mV: 0
ak_MDFEXT_interference_mV: 2.4400
ilable_signal_after_eq_mV: 40.0822
   steady_state_voltage_mV: 126.5731
               VEO_mV: 64.3043
        VEO_normalized: 0.8022
               VEC_dB: 1.9148
      equivalent_ISI_ICN: 4.6485e-04
        sci_noise_FD_RMS: 0
         CTLE_zero_poles: [9.2972e+09 1.0000e+09 1.4100e+10 1.5600e+10 1.2000e+09]
         CTLE_DC_gain_dB: -6.5000
              TXLE_taps: [0 -0.1000 0.8500 -0.0500 0 0]
               DFE_taps: [0×1 double]
        cci_noise_TD_BER: 0.0024
  peak_interference_at_BER: 0.0079
                   FOM: 25.6388
              DFE4_RSS: 0
              DFE2_RSS: 0
```

With xtalk

```
com_ieee8023_93a_165('eq_qsfp_mtf.xls', 3, 0,
'A_MCB_P1P3_TX3_tcard_P2P4_TX3.s4p',
'MCB_P1P3_TX1_HCB_P2P4_TX3_term_changed.s4p',
'MCB_P1P3_TX2_HCB_P2P4_TX3_term_changed.s4p',
'MCB_P1P3_TX4_HCB_P2P4_TX3_term_changed.s4p')
```

Conclusions from initial simulations.

- With the risetime corrected and using a 3 tap FIR the adaptation in COM found the same optimum settings for eye height as ADS.
- The COM VEO is 2-3mV larger than the ADS simulation with these same settings.
- With an unrealistically good host and IC package the 32mV eye amplitude is easily achieved with a 10dB channel
- There is a small degradation in eye height with test board FEXT of 2.7mV.
- Note that this comparison between COM and ADS results is very different from the March 6 presentation to the ad-hoc. In that presentation using a 4 tap FIR, COM adjusted its tap weights such that although COM reported a similar VEO, ADS simulation with the same tap weights reported a much worse eye.

Adding Impairments

Impairments methodology and limitations.

- Perform simulation w/ various source impedance, package impedance, board impedance, Cd and Cp, jitter and noise.
- For each set of parameters adjust Av such that Vf=0.4V at TP0a with Np=13.
- When Jitter is added it is added in the ADS transmitter with the values Jitter: 0.01UI RJ; 0.02UI DJ
- For calculating the effect of Tx_SNR, noise was added to the receiver equal to the rms value of the noise created by the Tx_SNR when passed through the channel.
- Due to limitations in the simulation environment the effect of RLM was not investigated.
- Additional board degradations and reflections are not included.
- Tx die risetime of 5ps is likely to be somewhat optimistic.

Eye @ BER 1E-5

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Row	Av (V)	Rd (ohm)	Cd (pF)	Cp (pF)	Vf (Np= 13) (V)	Package Zc (ohm)	Board Zc (ohm)	SNR_TX (dB)	Jitter On	CTLE peaking (dB)	TX FIR	Mated Board FEXT (mV)	Lower Eye Width (pS)	Center Eye Width (pS)	Upper Eye Width (pS)	Lower Eye Height (mV)	Center Eye Height (mV)	Upper Eye Height (mV)
1	0.4	50	0	0	0.385	100	100	No Tx noise	No	6.5	[-0.1 0.85 -0.05]	0	15.1	15.1	15.4	64	63	65
2	0.4	50	0	0	0.385	100	100	No Tx noise	No	6.5	[-0.1 0.85 -0.05]	2.7	14.7	14.7	15.1	62	61	63
3	0.416	50	0	0	0.4	100	100	No Tx noise	Yes	6.5	[-0.1 0.85 -0.05]	3.5	12.6	13.2	13.6	57	57	59
4	0.418	50	0.18	0.11	0.4	100	100	No Tx noise	Yes	6	[-0.1 0.8 -0.1]	3.5	11.5	11.7	11.5	47	50	49
5	0.418	50	0.28	0.11	0.4	100	100	No Tx noise	Yes	5	[-0.1 0.75 -0.15]	3.5	10.4	10.4	10.2	38	40	41
6	0.442	55	0.18	0.11	0.4	90	109.8	No Tx noise	Yes	6	[-0.1 0.8 -0.1]	3.5	11.3	11.5	11.5	46	45	48
7	0.445	55	0.28	0.11	0.4	85	109.8	No Tx noise	Yes	5	[-0.1 0.75 -0.15]	3.5	9.8	10.4	10.2	38	38	40
8	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	3.5	8.7	8.3	8.7	30	28	31
9	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	5.1	8.5	8.3	8.3	29	28	31
10	0.442	55	0.18	0.11	0.4	90	109.8	31	Yes	6	[-0.1 0.8 -0.1]	5.1	9.8	10.0	10.0	37	37	39
11	0.442	55	0.18	0.11	0.4	90	109.8	32.5	Yes	6	[-0.1 0.8 -0.1]	5.1	10.6	10.4	10.2	40	38	41

802.3 bs draft 3.0 120D

802.3 cd draft 1.2 clause 137

Note that 0.22UI eye width (120E draft 3.0 spec) = 8.28ps and it is expected that ADS eye width is optimistic compared to 120E test methodology.

The Mated Board FEXT numbers quoted are what would have been measured using the 1200mV amplitude and 9.6ps risetime specified in the mated board FEXT test. They are not the actual FEXT produced in the simulation which will be smaller due to lower amplitude aggressors and the package and board losses.

Eye @ BER 1E-5

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100K bits

Row	Av (V)	Rd (ohm)	Cd (pF)	Cp (pF)	Vf (Np=13) (V)	Package Zc (ohm)	Board Zc (ohm)	SNR_TX (dB)	Jitter On	CTLE peaking (dB)	TX FIR	Mated Board FEXT (mV)	Lower Eye Width (pS)	Center Eye Width (pS)	Upper Eye Width (pS)	Lower Eye Height (mV)	Center Eye Height (mV)	Upper Eye Height (mV)
8	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	3.5	8.7	8.3	8.7	30	28	31
9	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	5.1	8.5	8.3	8.3	29	28	31
11	0.442	55	0.18	0.11	0.4	90	109.8	32.5	Yes	6	[-0.1 0.8 -0.1]	5.1	10.6	10.4	10.2	40	38	41

10Million bits

Row	Av (V)	Rd (ohm)	Cd (pF)	Cp (pF)	Vf (Np=13) (V)	Package Zc (ohm)	Board Zc (ohm)	SNR_TX (dB)	Jitter On	CTLE peaking (dB)	TX FIR	Mated Board FEXT (mV)	Lower Eye Width (pS)	Center Eye Width (pS)	Upper Eye Width (pS)	Lower Eye Height (mV)	Center Eye Height (mV)	Upper Eye Height (mV)
8	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	3.5	8.5	8.3	8.7	29	29	31
9	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	5.1	8.5	8.3	8.7	28	29	31
11	0.442	55	0.18	0.11	0.4	90	109.8	32.5	Yes	6	[-0.1 0.8 -0.1]	5.1	10.6	10.2	9.98	39	38	40

COM

Row	Av (V)	Rd (ohm)	Cd (pF)	Cp (pF)	Vf (Np=13) (V)	Package Zc (ohm)	Board Zc (ohm)	SNR_TX (dB)	Jitter On	CTLE peaking (dB)	TX FIR	Mated Board FEXT (mV)	Height (VEO) (mV)
8	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	3.5	26.4
9	0.445	55	0.28	0.11	0.4	85	109.8	31	Yes	5	[-0.1 0.75 -0.15]	5.1	25.96
11	0.442	55	0.18	0.11	0.4	90	109.8	32.5	Yes	6	[-0.1 0.8 -0.1]	5.1	36.1

802.3 bs draft 3.0 120D

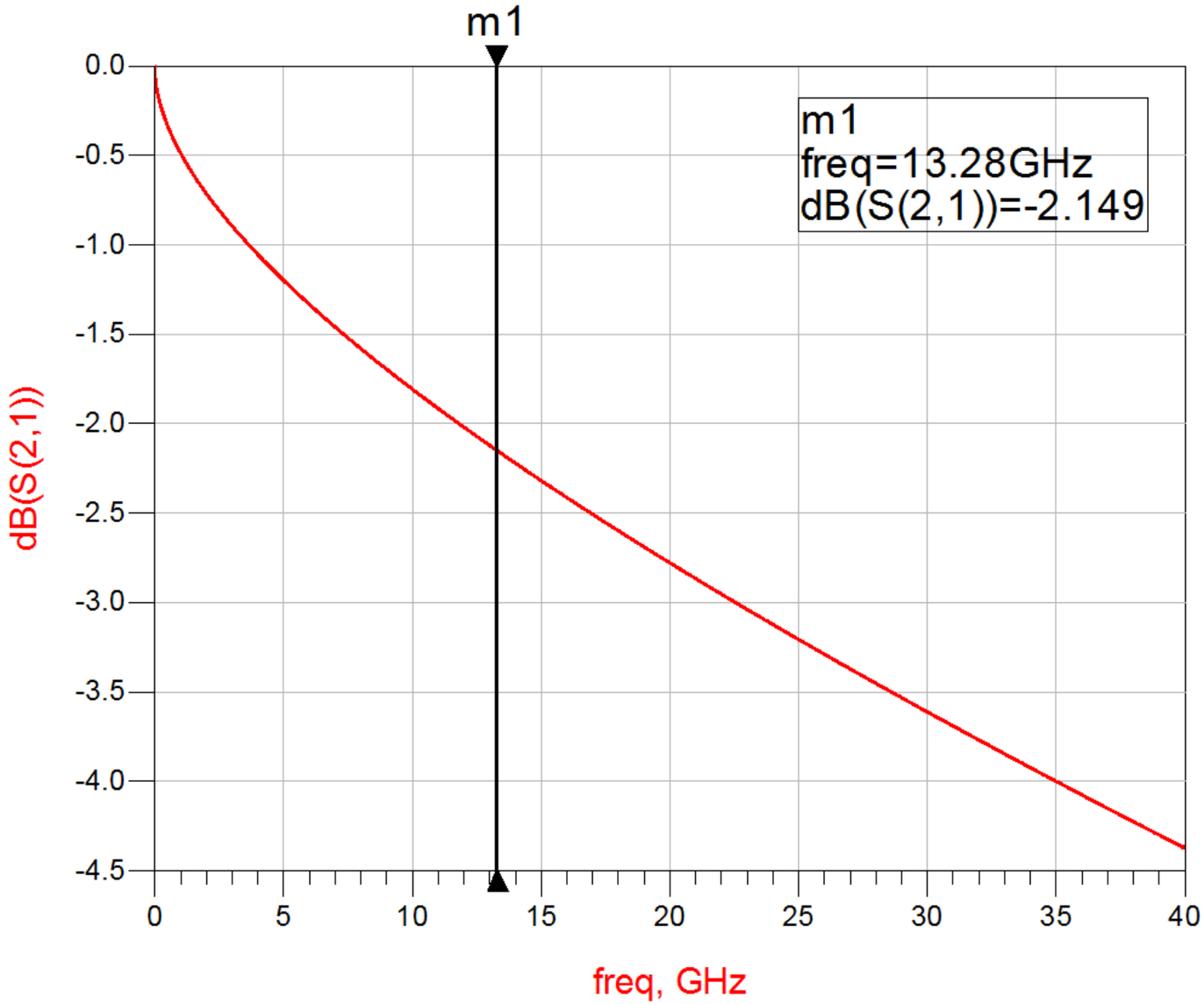
802.3 cd draft 1.2 clause 137

Conclusions.

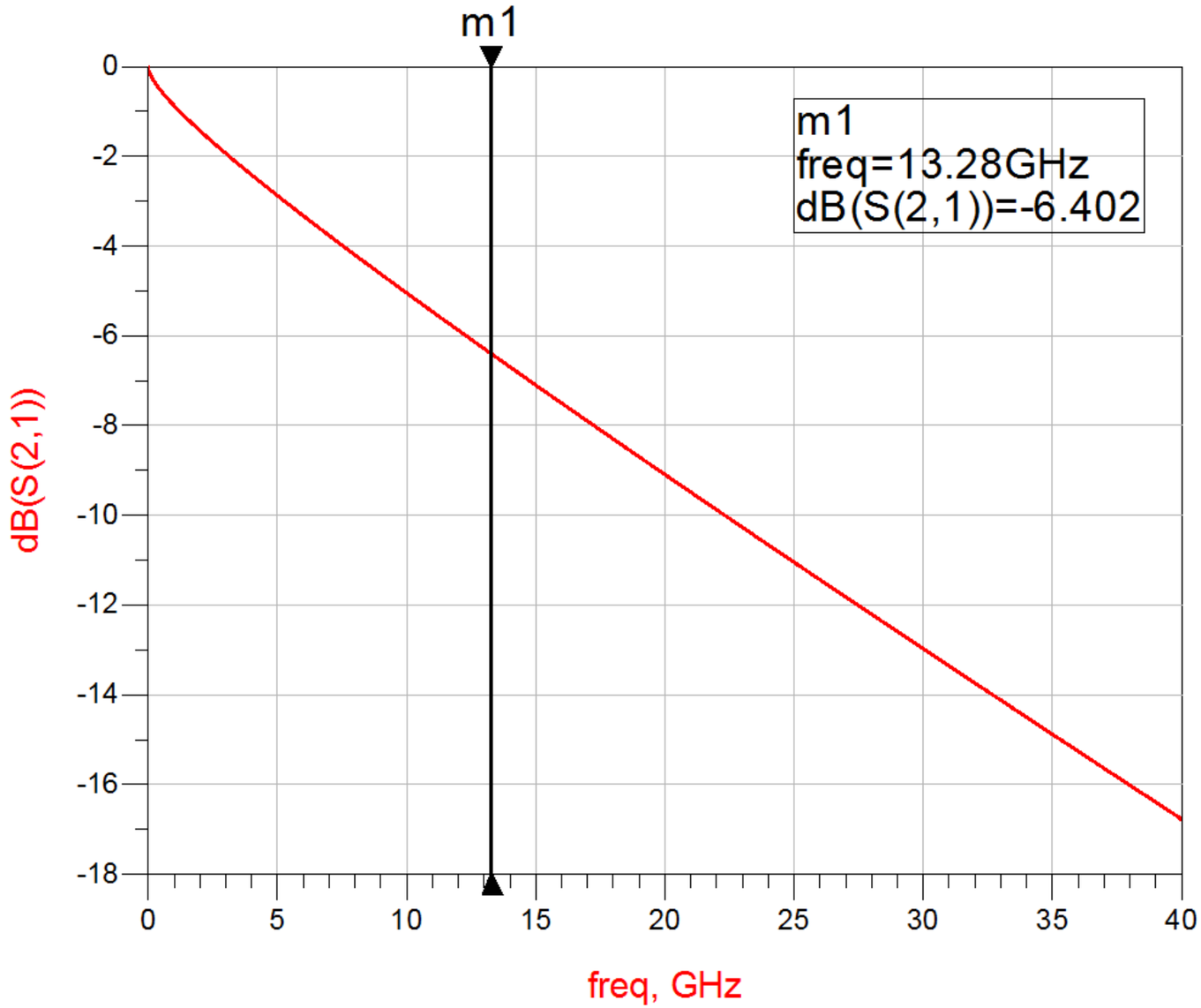
- Increasing the number of bits for the simulation beyond 10^5 only makes a small difference.
- For the impaired channels COM also found the same optimal equalizer settings (with 3 tap FIR).
- In contrast to the no impairment channel where COM VEO was 2-3mV larger than the ADS simulation with the same settings, with these impaired channels COM VEO is giving 2-3mV smaller VEO than ADS.
- The 32mV eye amplitude specification is not achieved with the worst case 120D draft 3.0 transmitter even without including the effects of RLM and additional host PCB issues.
- The 32mV eye amplitude specification does look achievable with the 802.3cd draft 1.2 clause 137 transmitter.
- Key parameters are die capacitance, Tx_SNR.
- Transmitter noise appears to be swamping out the effect of the FEXT. Both COM and ADS are showing this effect.

Backup.

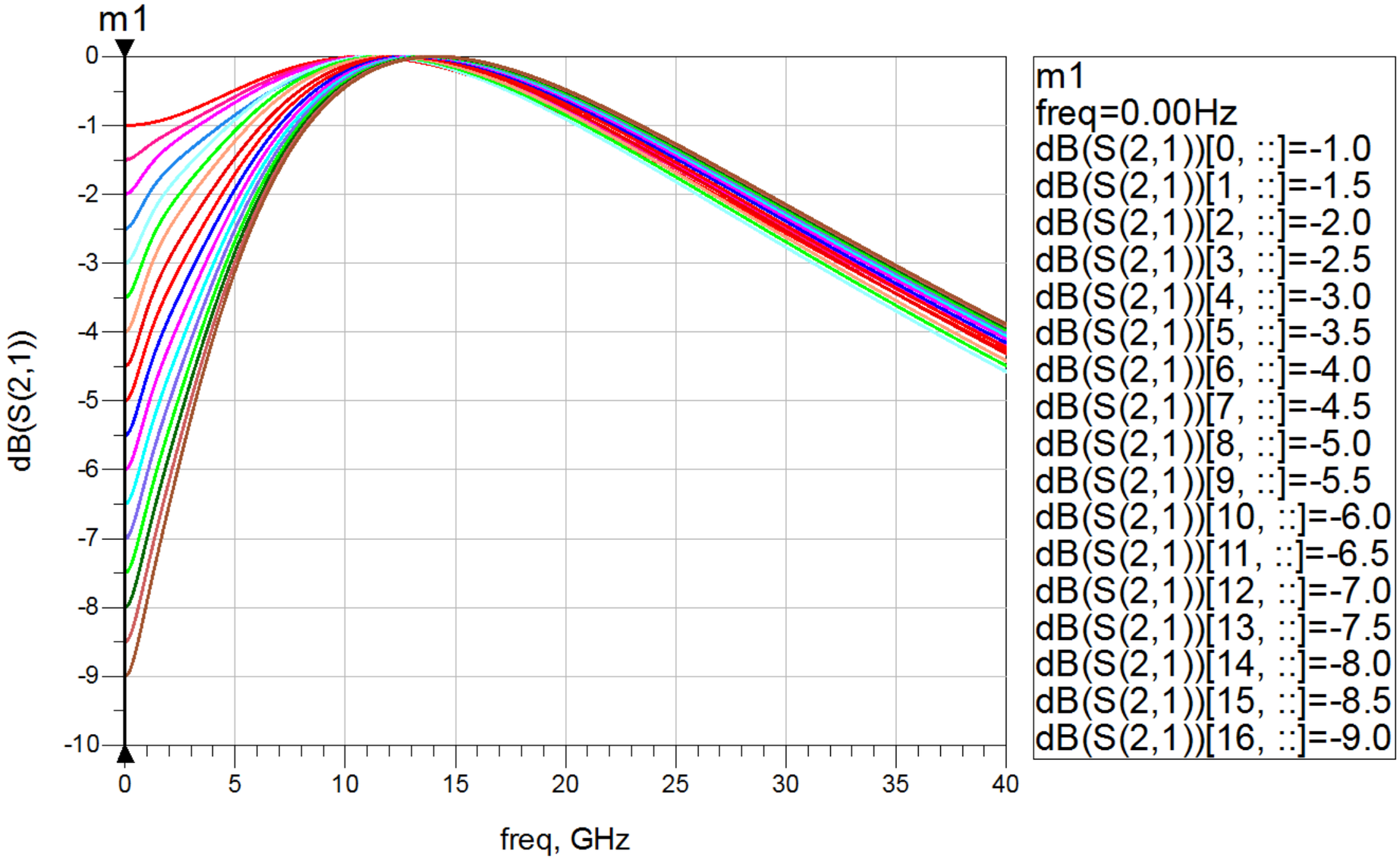
30mm 100ohm COM package insertion loss



151mm 100ohm COM PCB insertion loss



CTLE curves


m1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
dB(S(2,1))
0
5
10
15
20
25
30
35
40
freq, GHz
m1
freq=0.00Hz
dB(S(2,1))[0, ::]=-1.0
dB(S(2,1))[1, ::]=-1.5
dB(S(2,1))[2, ::]=-2.0
dB(S(2,1))[3, ::]=-2.5
dB(S(2,1))[4, ::]=-3.0
dB(S(2,1))[5, ::]=-3.5
dB(S(2,1))[6, ::]=-4.0
dB(S(2,1))[7, ::]=-4.5
dB(S(2,1))[8, ::]=-5.0
dB(S(2,1))[9, ::]=-5.5
dB(S(2,1))[10, ::]=-6.0
dB(S(2,1))[11, ::]=-6.5
dB(S(2,1))[12, ::]=-7.0
dB(S(2,1))[13, ::]=-7.5
dB(S(2,1))[14, ::]=-8.0
dB(S(2,1))[15, ::]=-8.5
dB(S(2,1))[16, ::]=-9.0