Impact of Clock Content on the CDR with Propose Resolution

Ali Ghiasi – Ghiasi Quantum, Phil Sun – Credo, Xiang He and Xinyuan Wang - Huawei

IEEE 802.3bs Task Force

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List of supporters

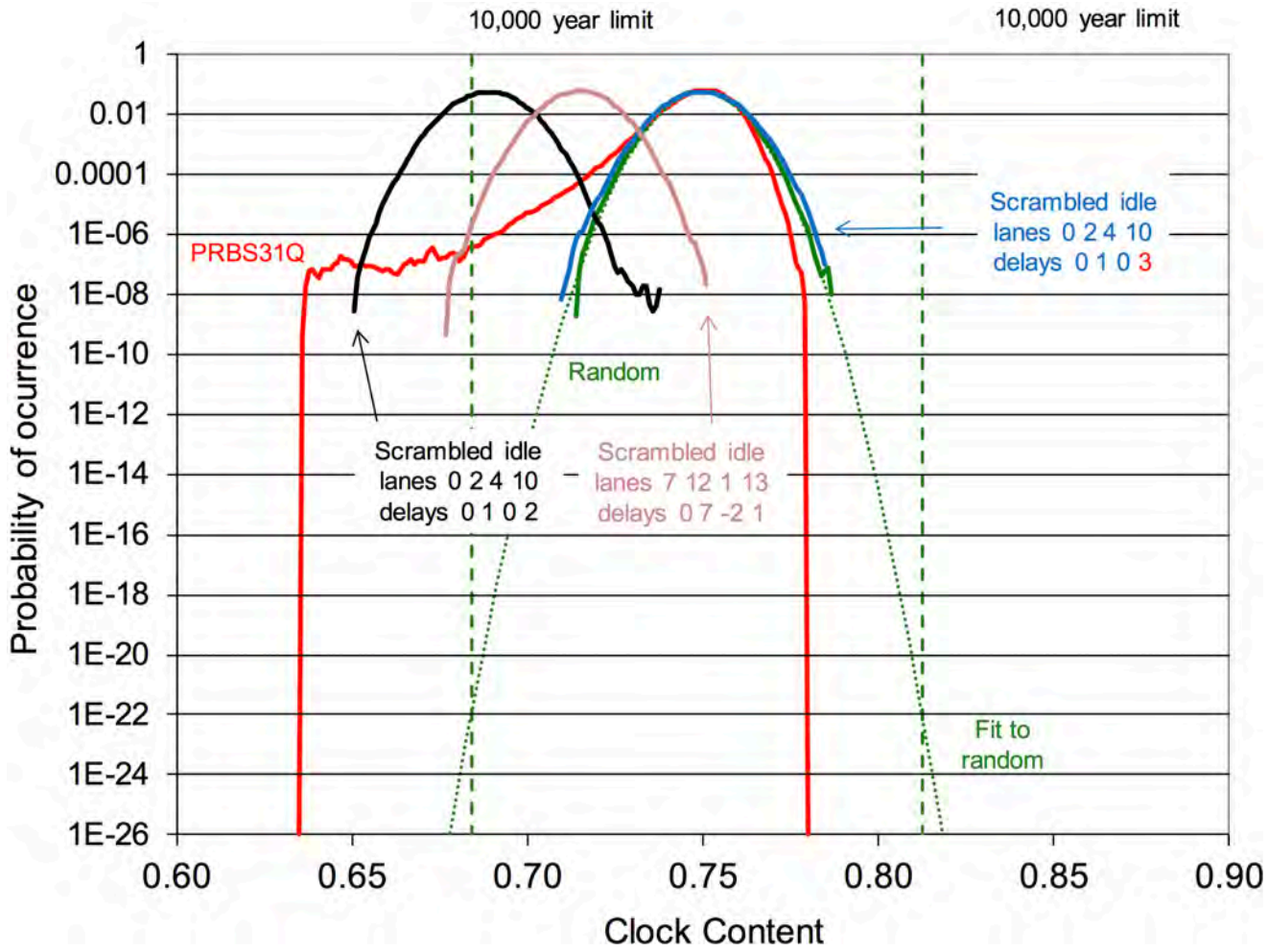
- **Eric Baden – Broadcom**
- **Rob Stone - Broadcom**

Background

- **In support of comments 92 and 93.**
- **It has been identified that a certain PCS when muxed with specific delay causes reduction in PAM4 transition density (TD) from 0.75 to ~0.683**
  - http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf
- **Follow on contribution showed that impact of reduction in transition density is reduction in CDR BW http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/ghiasi_01_0217_logic.pdf**
  - Symmetrical transition through the signal average − nominal TD 25% pathological PCS sequence results in 28% reduction in TD
  - All transitions through signal average − nominal TD 50% immune to TD reduction
  - All transitions − nominal TD 75% pathological PCS sequence results in 9% reduction in TD
- **TD variation in this range can be tolerated by a good CDR design**
  - Most modern CDR tolerate TD reduction and the associated reduction in the CDR BW
  - Understanding of the subject is important before attempting to make substantive change to the draft
- **This contribution investigate feasibility of using existing scrambled X^58, SSPRQ as well as defining new test patterns to improve the CDR JTOL test coverage by protecting against worst case clock content**
  - If we are going to define a new pattern scrambled X^58 is better representative for worst case clock content than defining an SSPRQ2
- **Even if we do nothing JTOL penalty for a 400 GbE symmetrical through average CDR is just 0.0167!**

The Extent of Clock Content Issue for All Transitions

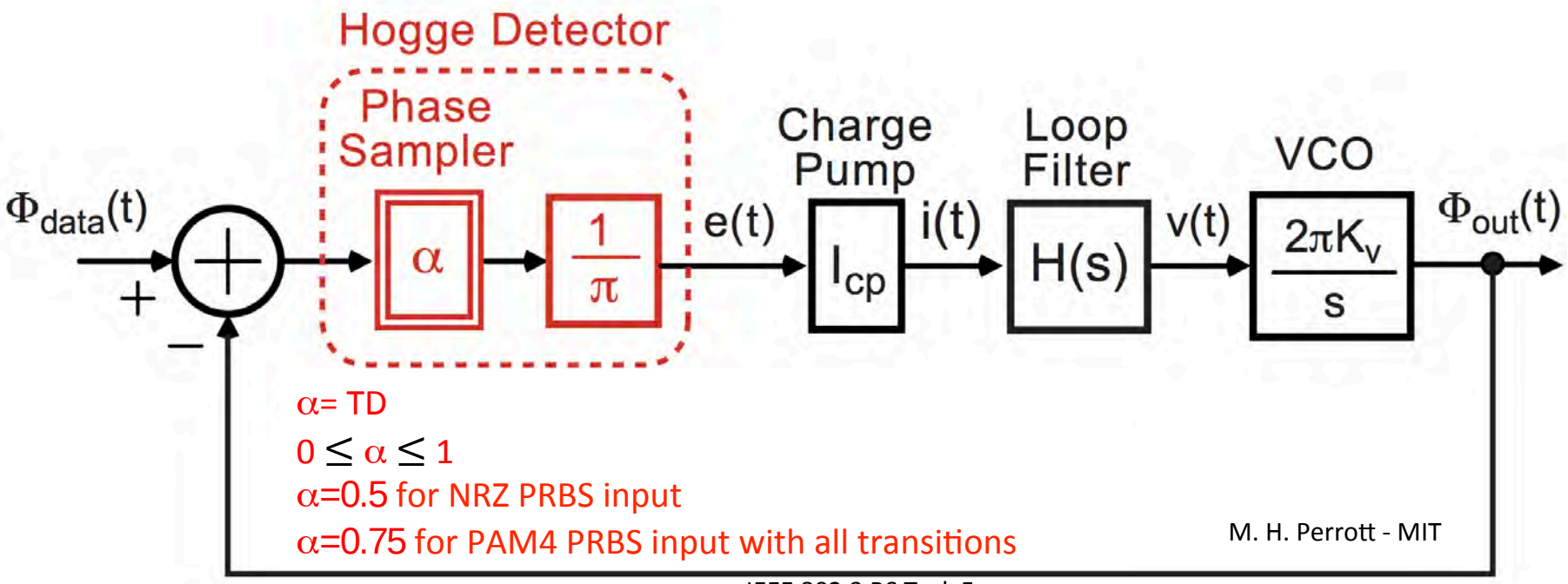
- **Lets assume given CDR operates with all transitions and the nominal CDR BW=4MHz**
- **High probability occurrence determine CDR BW with low probability occurrences washed out**
  - PRBS31Q with peak TD=0.75 and large left shoulder may result in negligible reduction in CDR BW from 4 MHz
  - Scrambled idle (blue) and random data will result in CDR BW of 4 MHz
  - Scrambled idle (pink) with TD=0.72 results in CDR=3.84 MHz
  - Scrambled idle (black) with TD=0.683 results in CDR BW=3.64 MHz
- **Given TD peak the CDR BW reduction is pretty much determined proportionally by TD shift.**



http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf

Basic Operation of the CDR

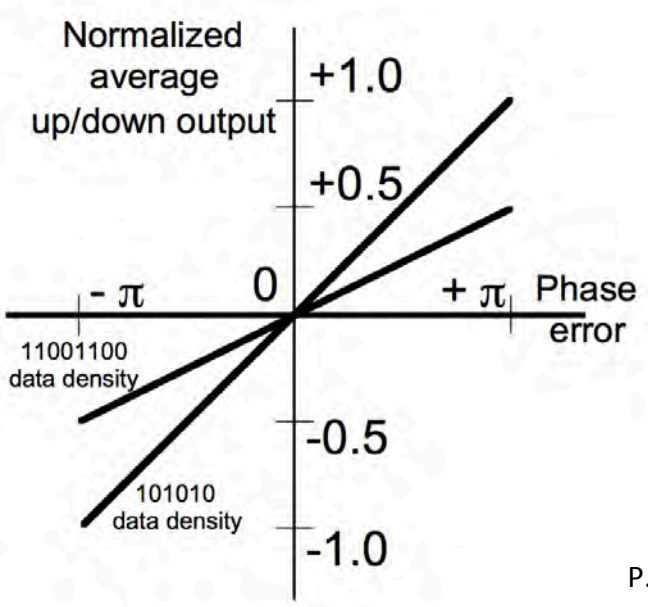
- **Key element of CDR are the phase detector, charge pump, loop filter and VCO**
  - Common implementation of phase detector is based on Hogge Detector where TD affects the loop gain and loop BW
  - $CDR\ BW = Nominal\ loop\ BW \times TD$
- A CDR designed for 802.3bs applications has a BW of 4 MHz assuming nominal PAM4 TD.



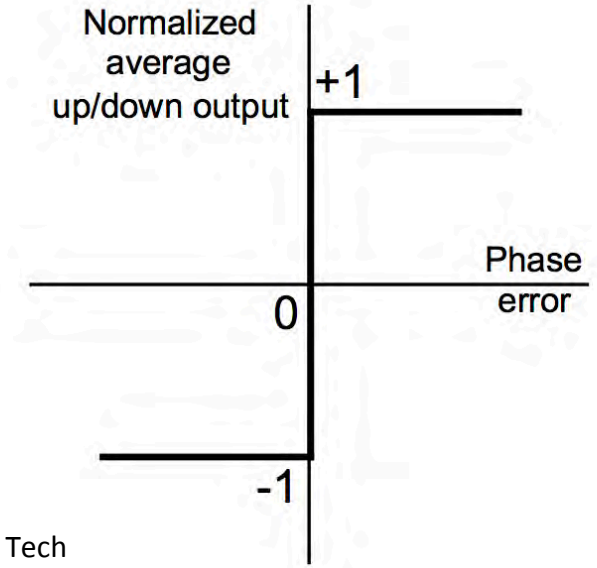
Transfer Characteristics of the Hogge Phase Detector

- **Example of linear and binary phase detector**
  - Linear phase detector response
    - Pattern 11001100 with TD=0.5 has gain of 0.5
    - Pattern 10101010 with TD=1.0 has gain of 1.0
- **A sophisticated CDR may have TD detector and accordingly adjust the loop gain to maintain target loop BW**
- **8B10B coding run length are limited to 5 bit but TD varies drastically or from 0.3 to 1.0!**

Linear Phase Detector



Binary Phase Detector

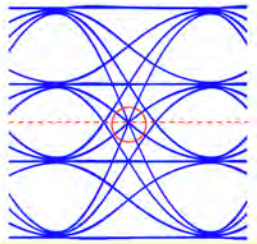


P.E. Allen-G. Tech

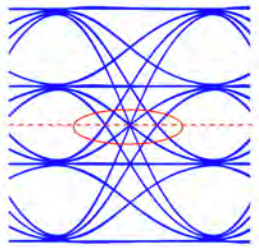
PAM4 CDR Implementation

- **PAM4 CDR architecture is very similar to NRZ with addition of PAM4 to Binary convertor**

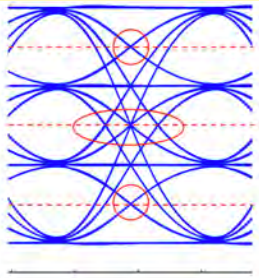
Symmetrical through average CDR



All transitions through average CDR

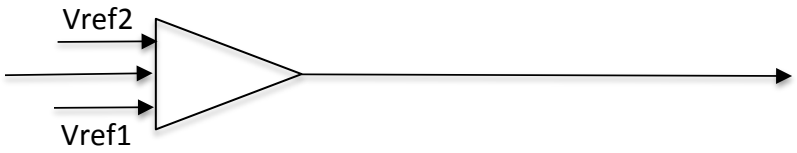


All transitions CDR



PAM4 to Binary Convertor

Simple PAM4 to Binary Convertor operating with 25% TD

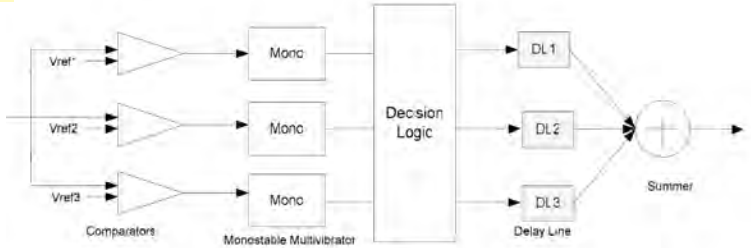


PCS Pattern may Reduce TD to 0.18 Nominal CDR BW Reduces from 4 MHz to 2.88 MHz!

Simple PAM4 to Binary Convertor operating with 50% TD

PCS Pattern doesn't Change TD and CDR BW is not effected!

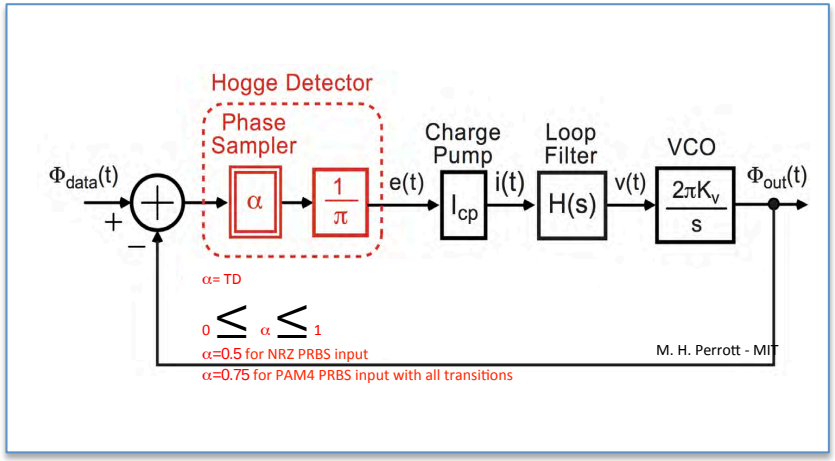
More robust implementation sampling all 3 eyes operating with 75% TD



Kim, Proceeding IDEAS 2005

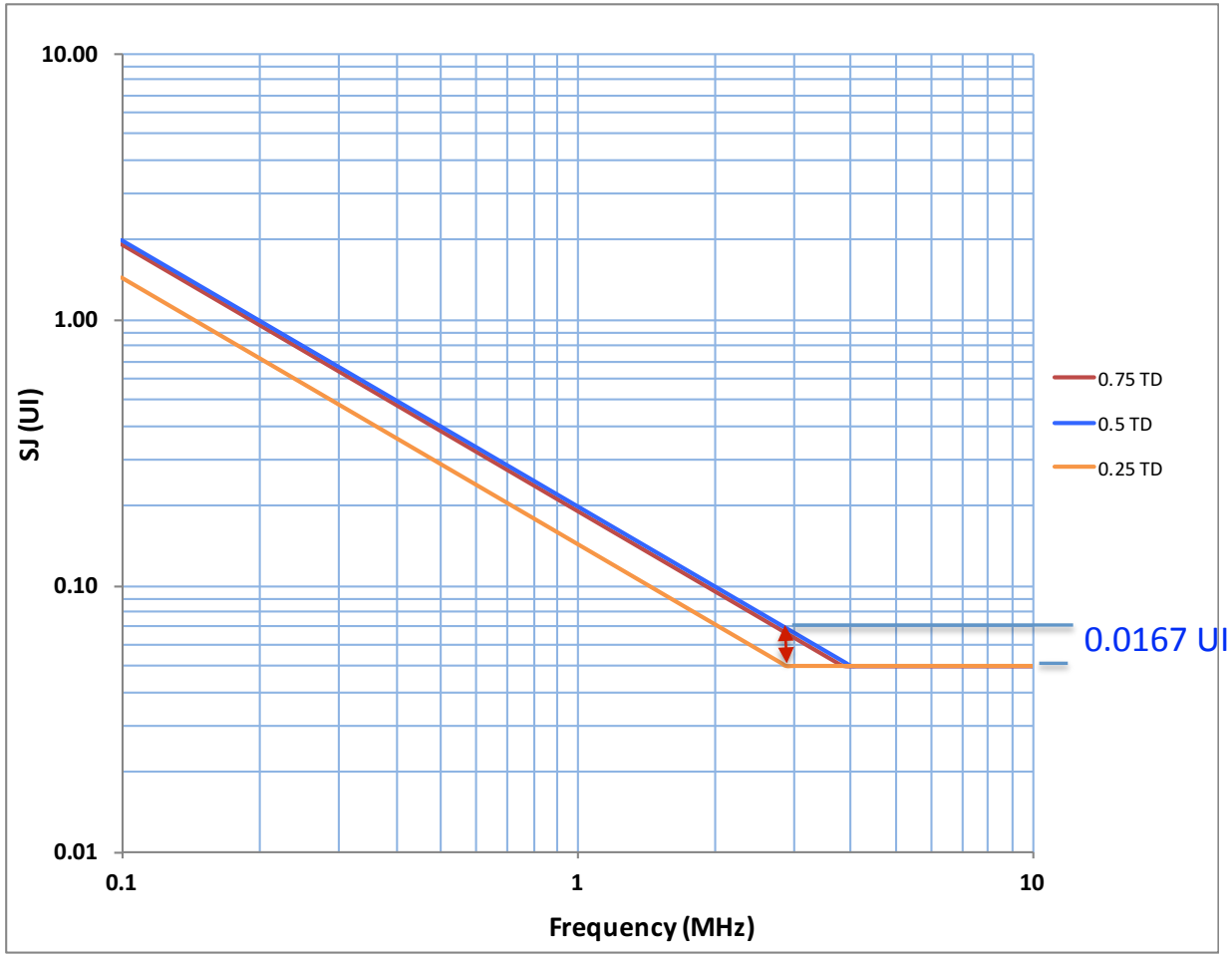
PCS Pattern may Reduce TD to 0.683 Nominal CDR BW Reduces from 4 MHz to 3.64 MHz!

Generic CDR



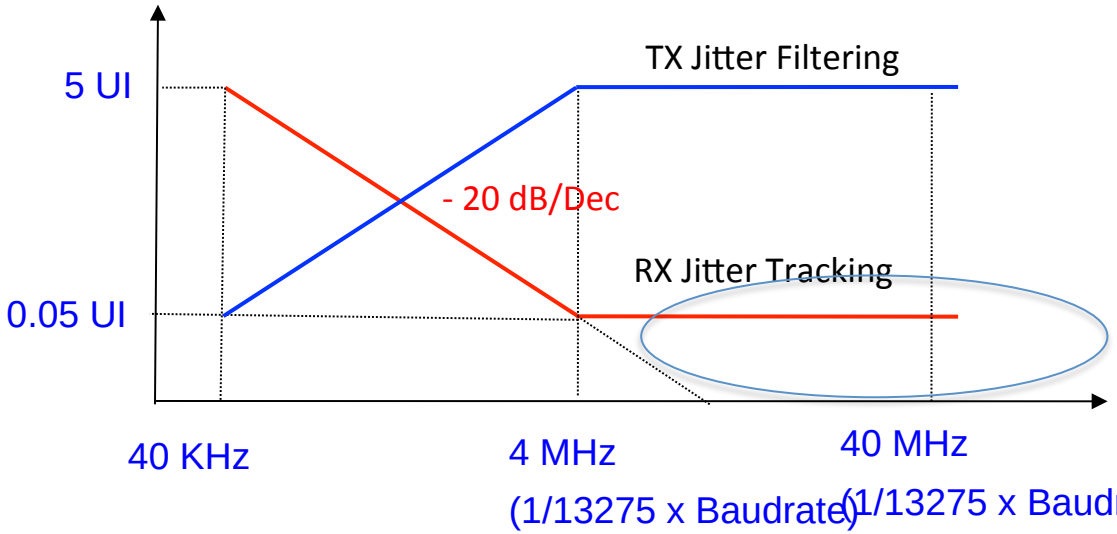
Penalty as Result of Clock Content on Jitter Tolerance

- **The three type of CDR**
  - A CDR operating with symmetrical transition through average corner frequency reduced to 2.88 MHz
  - A CDR operating with transition through average corner frequency remain 4 MHz
  - A CDR operating with all transition corner frequency reduced to 3.84 MHz
- **The worst case penalty as result of clock content for a CDR operating symmetrical transition through average is only 0.0167 UI!**
  - For CDR operating with all transitions is even less 0.0021 UI!



Could JTOL Test Protect Against Clock Content?

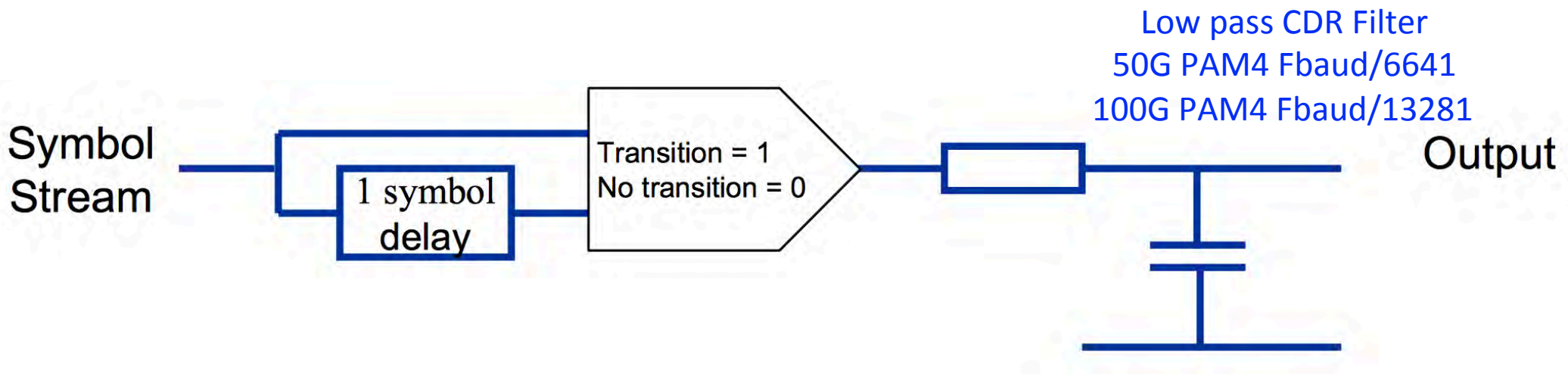
- **Clock content issue as result of pathological PCS lane mux and delay has the effect of reducing CDR BW due to low transition density**
  - Yes it can, if the CDR is tested with a data pattern that has similar effect reducing CDR BW
  - We looked at test patterns with lower TD as a JTOL test
  - It has been argued that JTOL test with 0.05 UI from 4-40 MHz is over stressing the receiver, maybe there is enough margin to cover 0.016 UI as result of clock content!



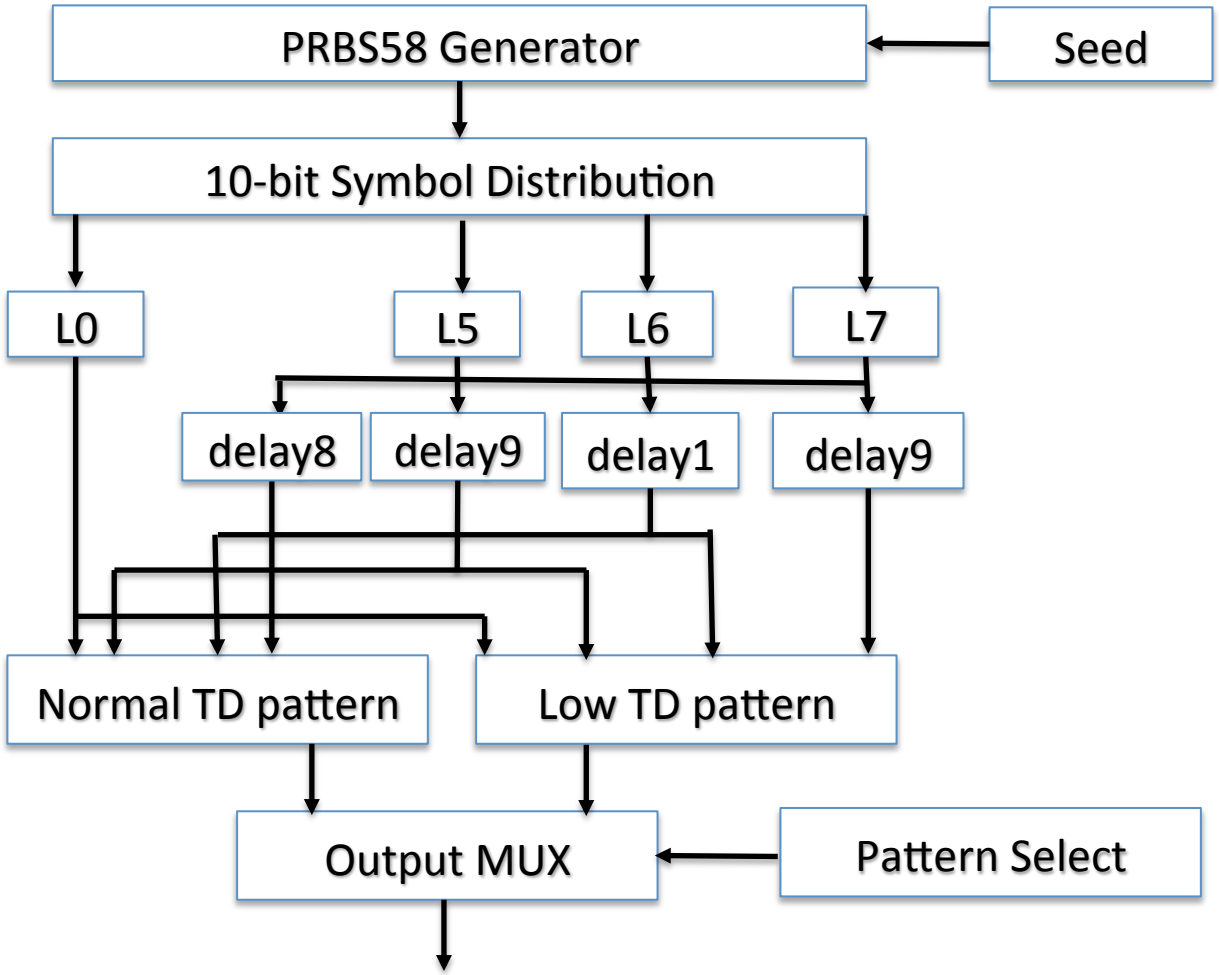
40 KHz

Clock Content Evaluated

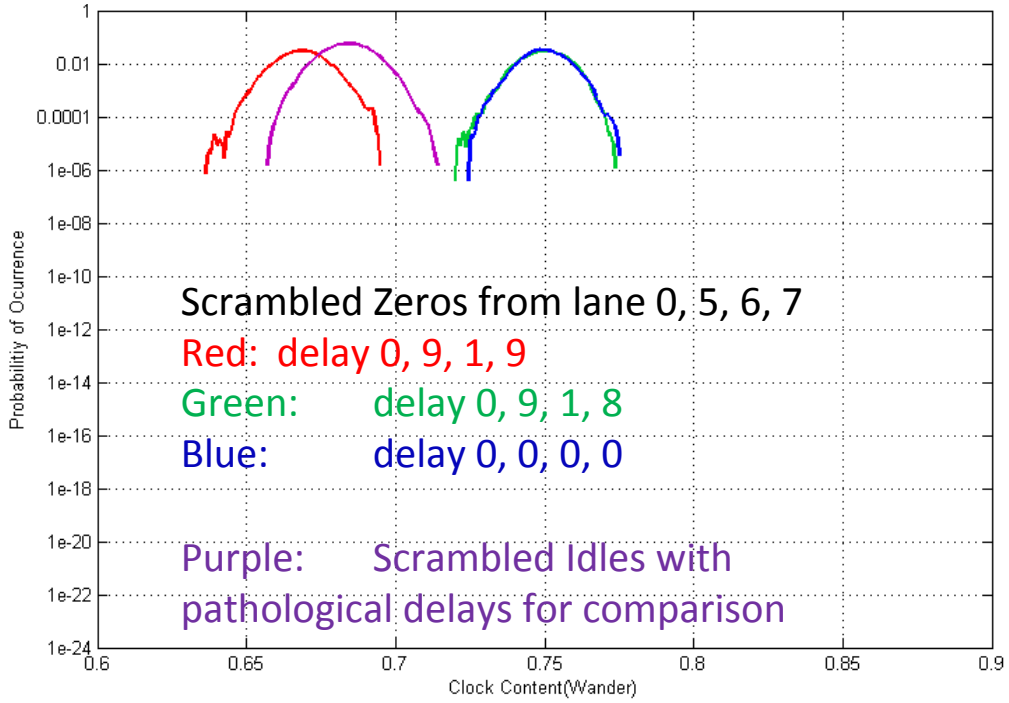
- **Data pattern transitions are filtered with a fix 4 MHz low pass filter ignoring CDR BW dependent on TD**
  - The 4 MHz 1st order low pass filter represent CDR tracking to the data
  - See http://www.ieee802.org/3/bs/public/adhoc/logic/oct27_16/anslow_02a_1016_logic.pdf.



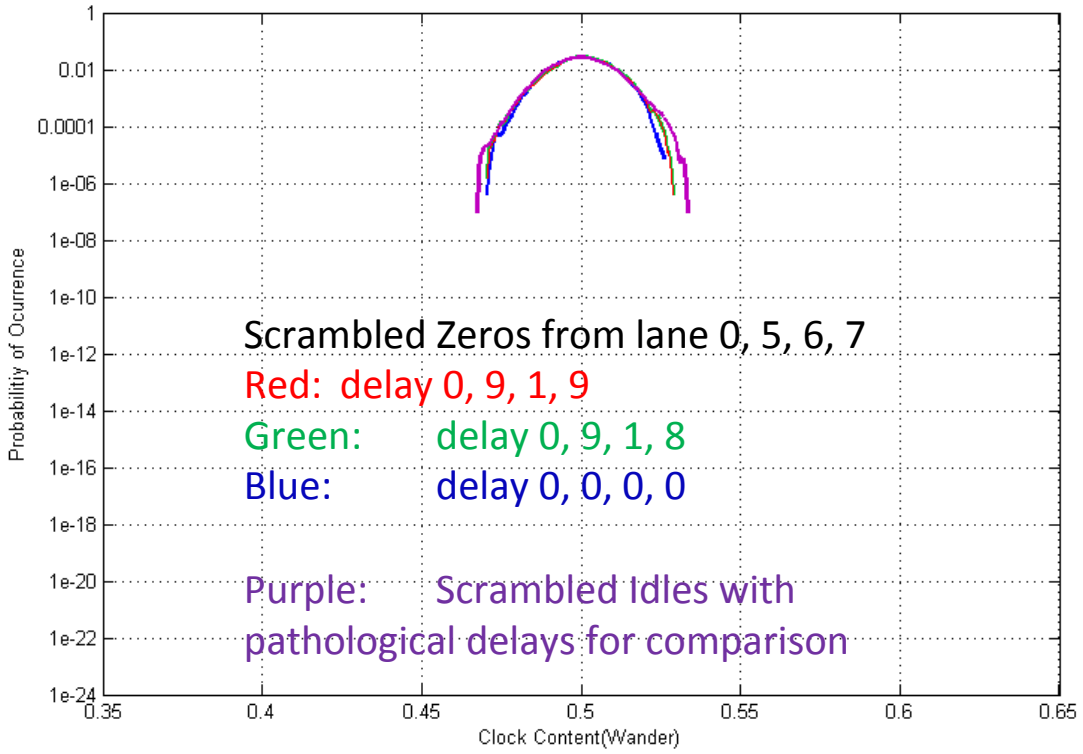
Generating Worst Clock Content Scrambled Pattern

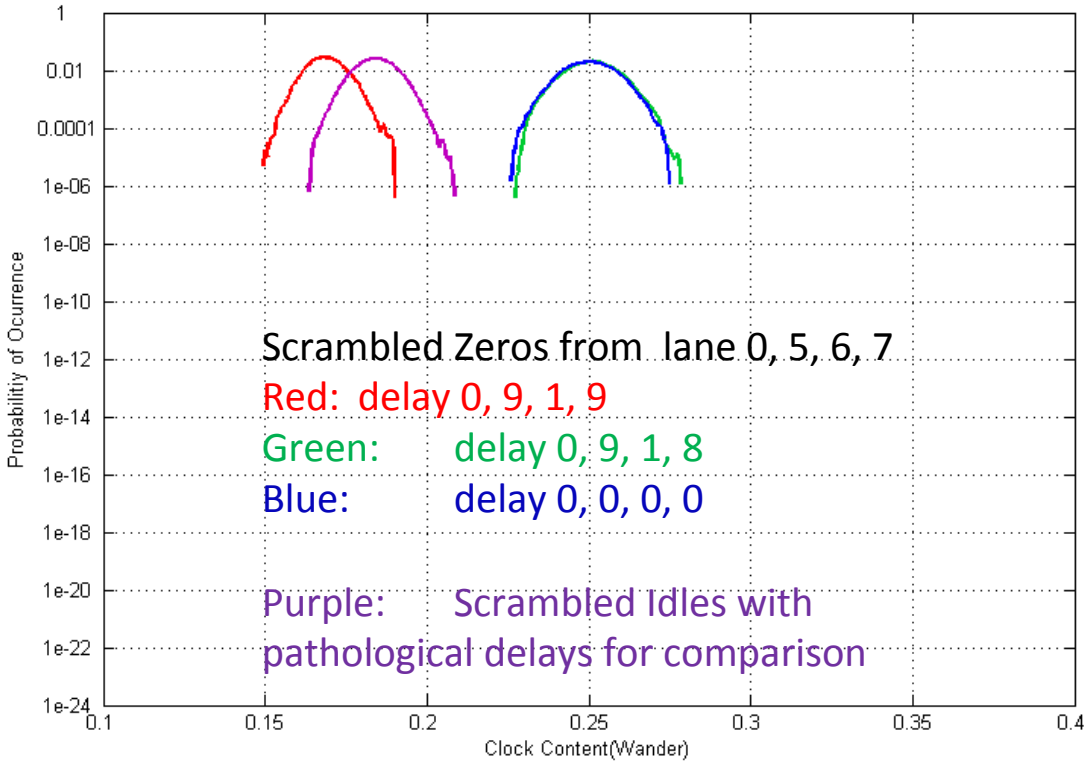


- Pattern Select toggles between normal and lower TD patters every 1048576 bits
- Seed is 0xccc0ccc0ccc0cc



Generating Worst Clock Content Scrambled Pattern





- **For 0.5 TD case, TD of this test pattern is very close to scrambled idles.**
- **For 0.25 and 0.5 TD cases, this test pattern provides about 10% extra stress on low TD tests.**

Testing CDR with Stress Pattern to Protect Against Worse Case Clock Content

- **SSPRQ pattern is a repeating 216-1 PAM4 symbol sequence constructed out of 3 sections of PRBS31 as shown in table 120-2 sequence A**
  - SSPRQ has variable TD from 0.65-0.74 and already more stressful than PRBS31 for the CDR
  - Sequence B is two repetition of sequence A with 1st and last bit removed creating 65534 bit sequence

Table 120–2—SSPRQ bit sequence A

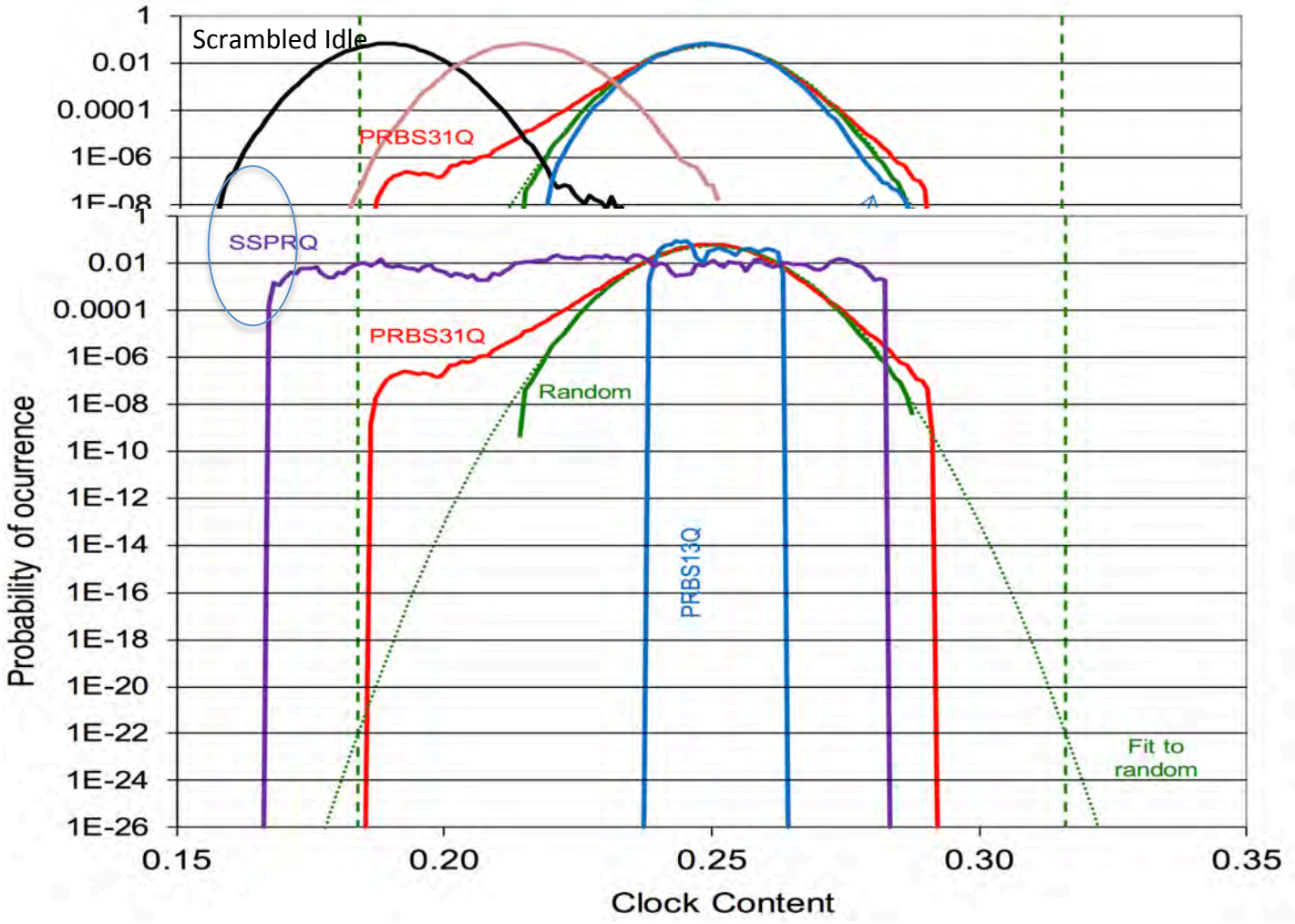
Pattern	Seed	Length
PRBS31	0x00000002	10924 bits
	0x34013FF7	10922 bits
	0x0CCCCCCC	10922 bits

- **Optional SSPRQ2 with dual bell shape response was created using standard PRBS31 for sequence A but using weighted PRBS31 having p1=0.328 for sequence B**
  - This option is tabled in favor of scrambled X^58.

Comparing Worst Case Clock Content to SSPRQ

- **For symmetrical transition through average**
- **Existing SSPRQ test pattern for all transitions is actually much more stressful than worst case clock content scrambled idle (black)!**
  - TD data include a 4 MHz low pass filtered so the CDR loop BW will adjust proportionally to the reduction in the TD
  - For a bell shape TD the CDR stays at the center of the bell, scrambled idle(black) will result in 2.88 MHz BW
  - But for SSPRQ at 1E-6 probability of occurrence varying from ~0.158-0.28 results in a CDR BW to drop to as low as 2.64 MHz
  - Scrambled idle (black) at 1E-6 (left shoulder) would be by 0.0022 UI more stressful than SSPRQ!

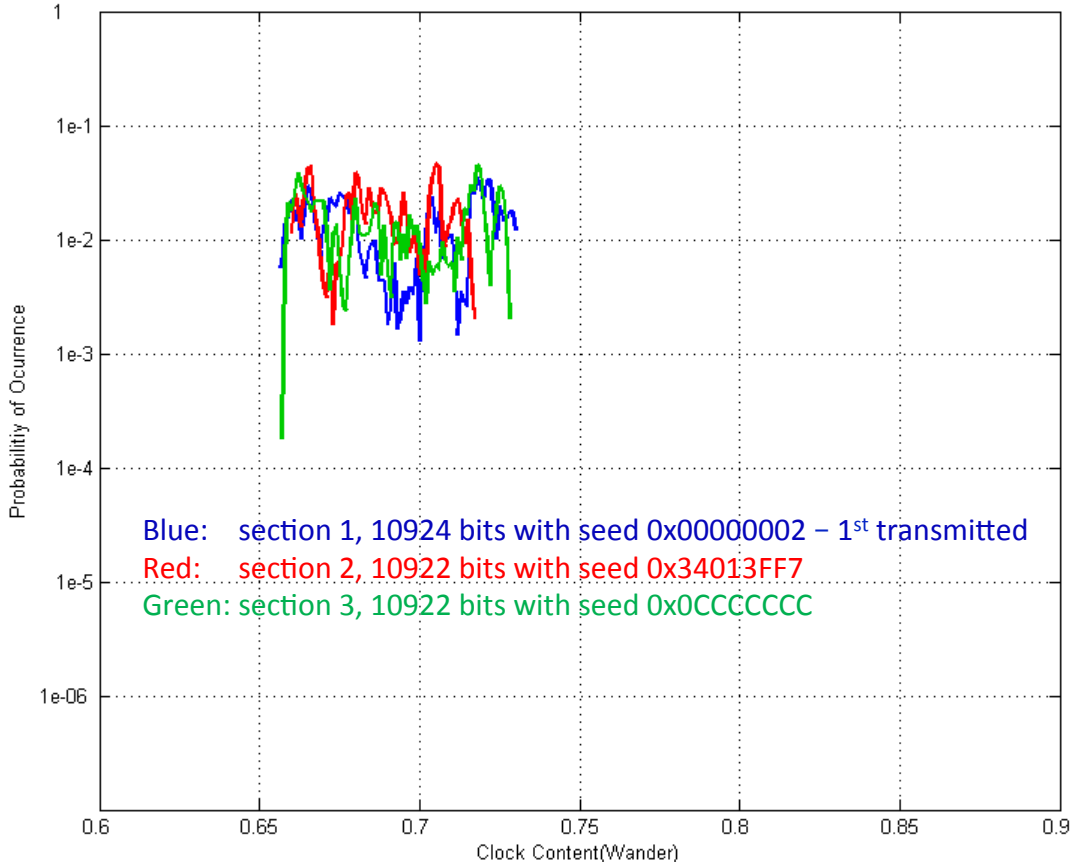
http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf



http://www.ieee802.org/3/bs/public/adhoc/logic/oct27_16/anslow_02a_1016_logic.pdf

Lets Look at SSPRQ Further

- **Looking at the SSPRQ TD time evolution for each of the 3 seeds and sequence A and B**
  - SSPRQ TD pattern exercises CDR over greater range than the reported clock content issue!



How to Protect Against Lower TD Data Pattern

- **CDR JTOL due to reduction in TD reduces CDR BW and can be protected in several ways:**
  - Reduce TX golden PLL corner frequency to ~2.88 MHz and keep the 4 MHz CDR BW to allow CDR implementation based on 25%, 50%, or 75% TD
  - Keep TX golden PLL corner frequency at 4 MHz and increase the CDR BW to ~5.56 MHz to allow CDR implementation based on 25%, 50%, or 75% TD
  - Test the DUT with a test pattern having variable TD forcing the CDR operate with nominal and low BW
- **The right approach without penalizing all transmitters or receivers is to test with a representative test pattern**
  - Given SSPRQ has the necessary property exercising the CDR linearly through the full range, expected to be more stressful and is our preferred solution
- **Existing SSPRQ can guard against potential CDR systematic weakness due to possible pathological clock content.**

Text Update to CL 124 in Support of Worst Case Clock Content

- **CDR tracking can be tested with pattern generated from PRBS58 alternatively SSPRQ could be used to test CDR tracking.**

Table 124–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3
7	PRBS58Q	120.5.11.2.3

Table 124–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 400GBASE-R signal	124.8.2
Side mode suppression ratio	3, 5, 6 or valid 400GBASE-R signal	—
Average optical power	3, 5, 6 or valid 400GBASE-R signal	124.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	124.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	124.8.5
Extinction ratio	4 or 6	124.8.6
$RIN_{21.4}OMA$	Square wave	124.8.7
Stressed receiver conformance test signal calibration	6	124.8.9
Stressed receiver sensitivity	3 or 5 and 6 or 7*	124.8.9

* Pattern 6 is to test for CDR tracking.

Summary

- **Worst case pathological clock content indicate:**
  - A CDR operating with all transition TD reduced by 9% - CDR BW drop by 9%
  - A CDR operating with all transitions through average not impacted – CDR BW not impacted
  - A CDR operating with only symmetrical transitions TD reduced by 28% - CDR BW dropped by 28%
- **The overall clock content impact on the CDR is minor with just 0.0167 UI for a CDR operating with symmetrical transitions through average and just 0.0021 UI for a CDR operating with all transitions**
- **Worst case clock content will reduce the nominal CDR BW but a well designed CDR can tolerate certain reduction in CDR tracking BW**
- **Instead of testing all CDRs with higher JTOL corner a better approach is to test the CDR with a test pattern having similar or slightly greater TD range**
- **PRBS58 generated patterns has a transition density range close to TD variation reported with a little extra stress.**
- **TD test pattern generators can be easily implemented in test instruments**
- **P802.3bs has comprehensive JTOL test with 0.05 UI of high frequency SJ which is about 3x max clock content effect and some have argued JTOL test is over-stressing the receiver!**