Logic Ad Hoc Report

IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force

March 2017 Vancouver

Mark Gustlin – Xilinx

400GbE Logic Report

- The stated charter is: **To address all issues in relation to the overall architecture of IEEE P802.3bs to ensure progress towards a technically complete draft**

- Dates of future logic ad hoc meetings will be announced via the reflector

- The 400 Gb/s Ethernet Task Force Logic Ad Hoc held four meetings since the last task force

Agenda 1/26/17

- Possible Solutions for Clock Content Issue - Mark Gustlin, Xilinx
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- Restricted muxing option - Mark Gustlin, Xilinx
- On clock content issue over four lane interleaving– Ryan Wong, Broadcom

Agenda 2/16/17

- Restricted muxing option (update) - Mark Gustlin, Xilinx
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- 4 Lanes Muxing Limited Clock Content Analysis - Oded Wertheim, Mellanox
- Impact of Transition Density on CDR – Ali Ghiasi

Agenda 3/2/17

- Possible 7b scrambler text changes - Mark Gustlin, Xilinx
- Generating Variable Transition Density Patterns – Ali Ghiasi

Agenda 3/9/17

- Proposed restricted muxing rules – Kapil Shrikhande, Innovium
- Impact of Clock Content on the CDR with Proposed Resolution – Ali Ghiasi
- Proposed FEC degrade signaling changes - Steve Trowbridge, Nokia

Thanks!