# Possible Solutions for Clock Content Issue

Mark Gustlin - Xilinx

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# Solution Options

1. Assume it is ok for receivers, don’t change the PCS
2. Restrict muxing to natural pairs for 50G lanes
3. Add new PRBS7 scrambler per FEC message
4. Use a precoder
5. Move scrambler location or other tweaks to PCS stack

# Understand why the problem occurs

- Everyone would feel more comfortable if we understand why this is happing, and it would give us confidence in the solution
- See: http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/wertheim_01_0217_logic.pdf

# Opt 1: Assume it is ok for receivers, don't change the PCS

- Is it ok?
- Early days for 56G SerDes, we don't know if this is a problem
- Assuming we thought the SerDes would be ok, we would need to create a new test pattern to cover this shift
  - This ensures that tested components will work in the field in all possible scenarios
- A new test pattern could impact other things such as TDECQ etc.
- See:

http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/ghiasi_01_0217_logic.pdf

http://www.ieee802.org/3/bs/public/adhoc/logic/mar02_17/ghiasi_01_0317_logic.pdf

http://www.ieee802.org/3/bs/public/adhoc/logic/mar09_17/ghiasi_02_0317_logic.pdf

# Opt 2: Restricted muxing to natural pairs for 50G lanes

- In this case a natural muxed pair is considered as PCS lane 0+1, or 2+3, or 4+5 etc.
- So a bit mux of two natural pairs (to a 100G lane) does not show a problem (at least with sims so far)
- See:

http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/gustlin_01_0217_logic.pdf

http://www.ieee802.org/3/bs/public/adhoc/logic/mar09_17/shrikhande_01_0317_logic.pdf

- See shrikhande_3bs_01_0317 for proposed text if this choice is adopted

# Opt 3: Add new PRBS7 scrambler per FEC message

- For details see:

  http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf

- Looks like it fixes the problem
- If we decide to go down this path, we would like to do further sims for 400GE (greater than +/- 10b of skew) to be ensure we have a good fix
- See gustlin_3bs_03_0317 for proposed text if this choice is adopted

## Opt 4: Use a precoder

- This seems to fix the problem based on simulation run by Ryan Wong
- Impact is a >doubling of the BER for random error model links
  - The impact has been evaluated by many optics focused people, it seems that it would be a significant impact and not worth pursuing

## Opt 5: Move scrambler or other tweak to PCS stack

- Other PCS tweaks might solve the problem?
- Oded is looking the impact of moving the scrambler to before transcoding and other possible changes
  - Moving scramble to before transcoding does not fully solve the problem
  - Distributing blocks on 257b boundaries (vs. 10b) is looking promising
- Turning off of Gray coding might help? Is the impact smaller than precoding?
- No presentations have been made proposing a change that fixes the problem in this area

Thanks!