Four lane interleaving

Pete Anslow, Ciena

IEEE P802.3bs Task Force, December 2016

Introduction

Ryan Wong from Broadcom has pointed out an issue that can occur when interleaving four PCS lanes from 200 Gb/s Ethernet to form a 100 Gb/s physical lane.

For most of the possible combinations of PCS lane and relative delay, the clock content characteristics are as shown in previous plots analysing the alignment markers. See for example anslow_01_1016_logic. However, for a few “rogue” combinations of PCS lane with particular relative delays the entire distribution of clock content shifts to lower values for both the “symmetrical transitions through average” and the “all transitions” plots.

Baseline wander

Previous NRZ contributions have used a “baseline wander” parameter

This was defined as:

Baseline wander is the instantaneous offset (in %) in the signal generated by AC coupling at the Baud rate / 10,000.

This analysis re-uses this definition unmodified, but it should be noted that for PAM4, the eye height is 1/3 that of NRZ so the effects of a given amount of baseline wander will be greater.

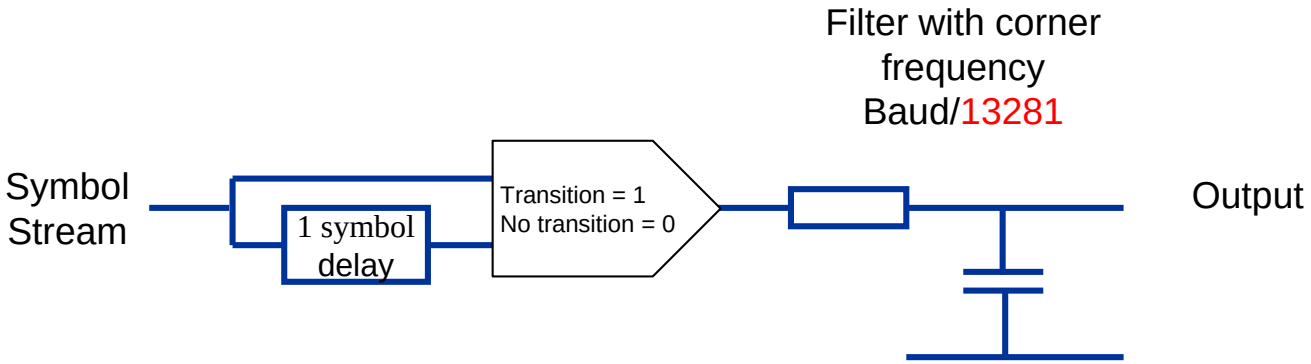
Clock content

The “clock content” parameter is defined here as:

Create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/13281.

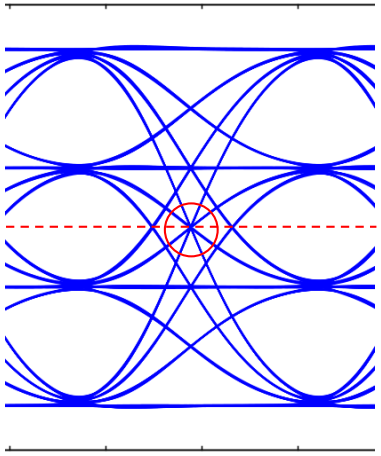
This analysis defines a transition as one of three possibilities (as per healey_3bs_01_1115):

- Symmetrical transitions through the signal average
- Transitions through the signal average
- All transitions

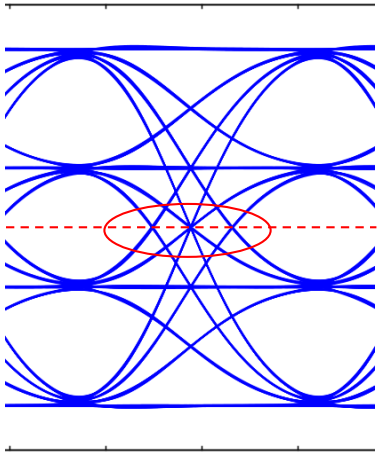


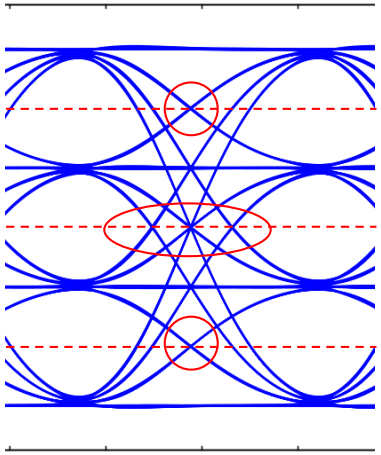
Clock content illustration

Symmetrical transitions through the signal average



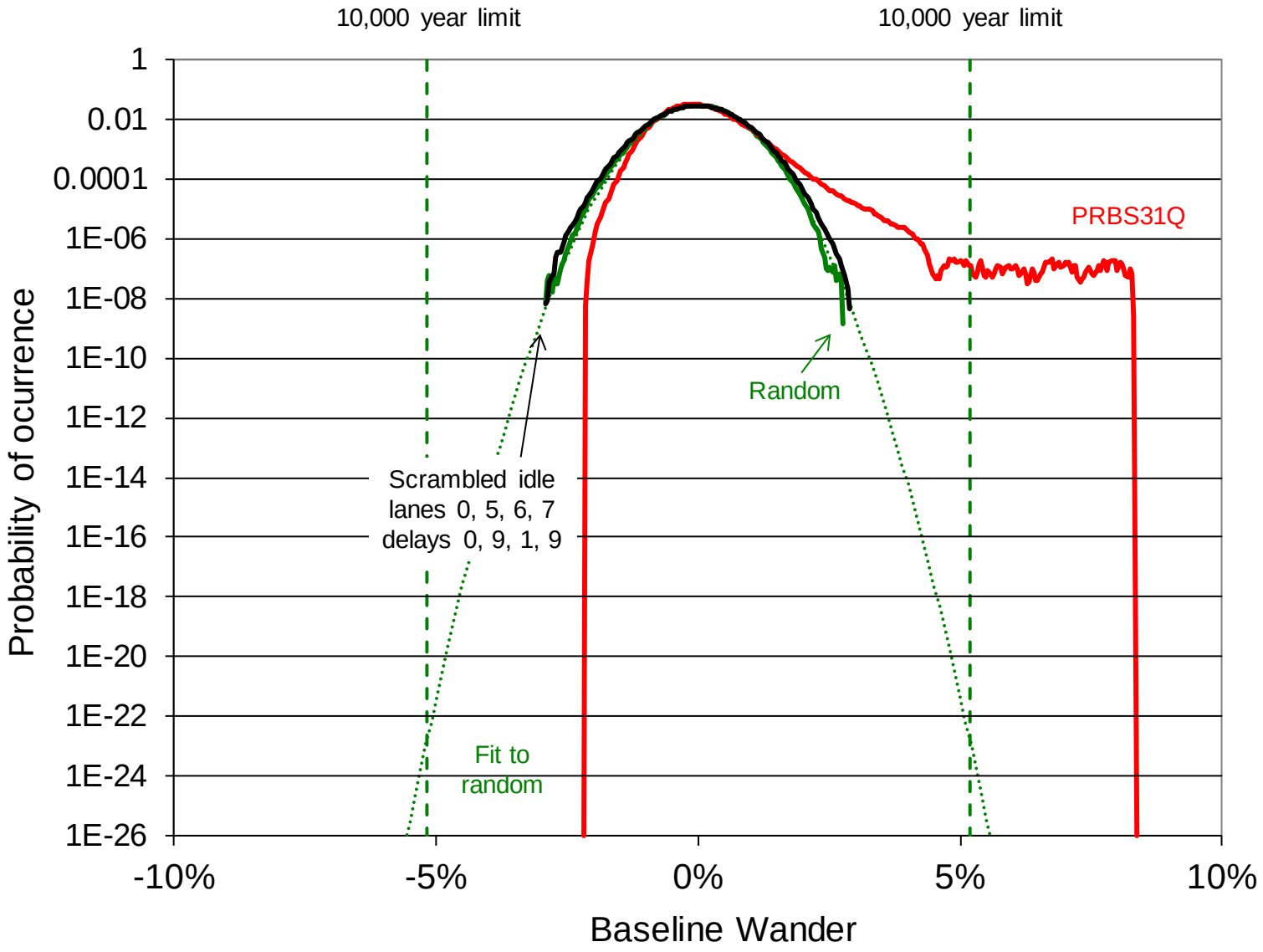
Transitions through the signal average



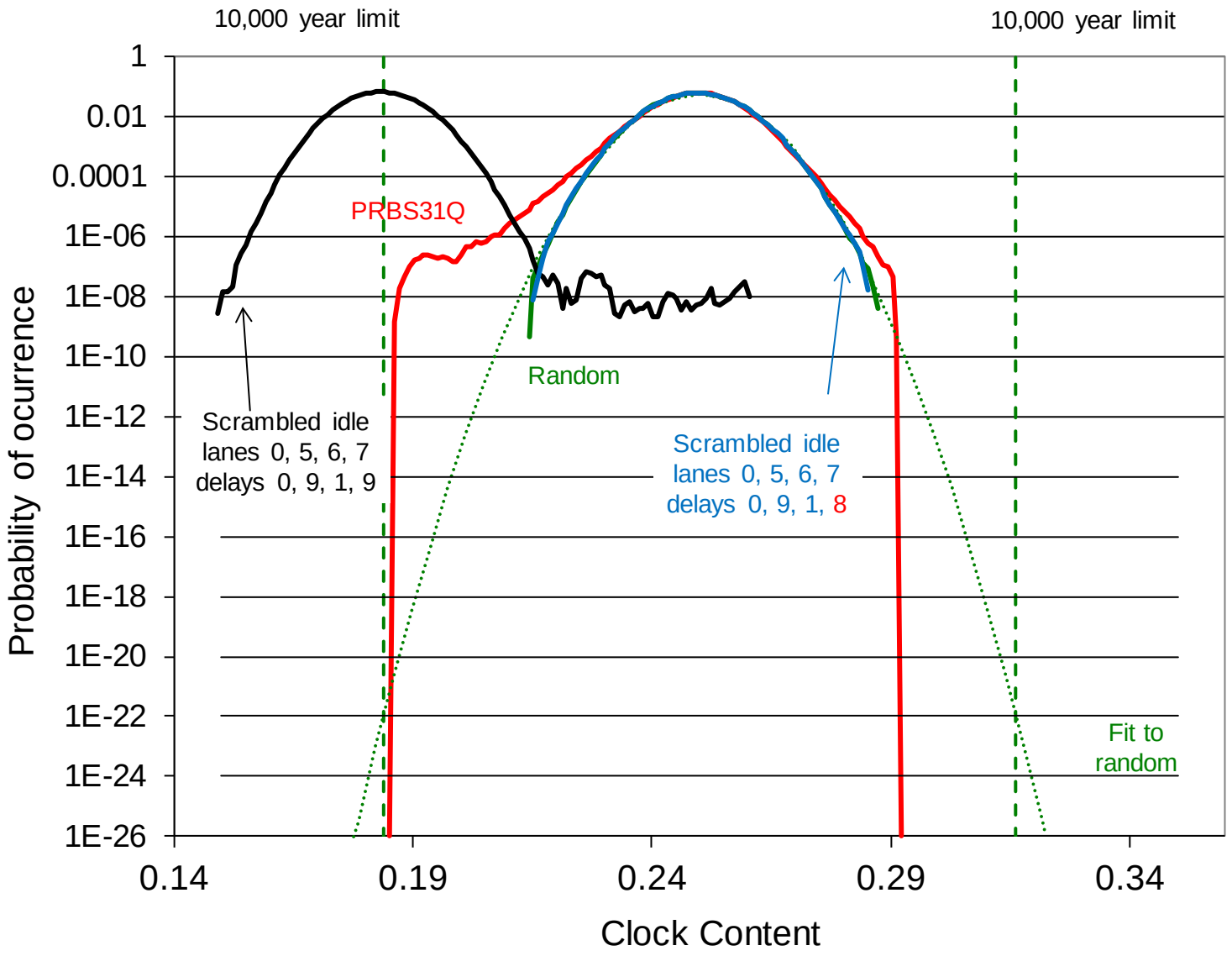


All transitions

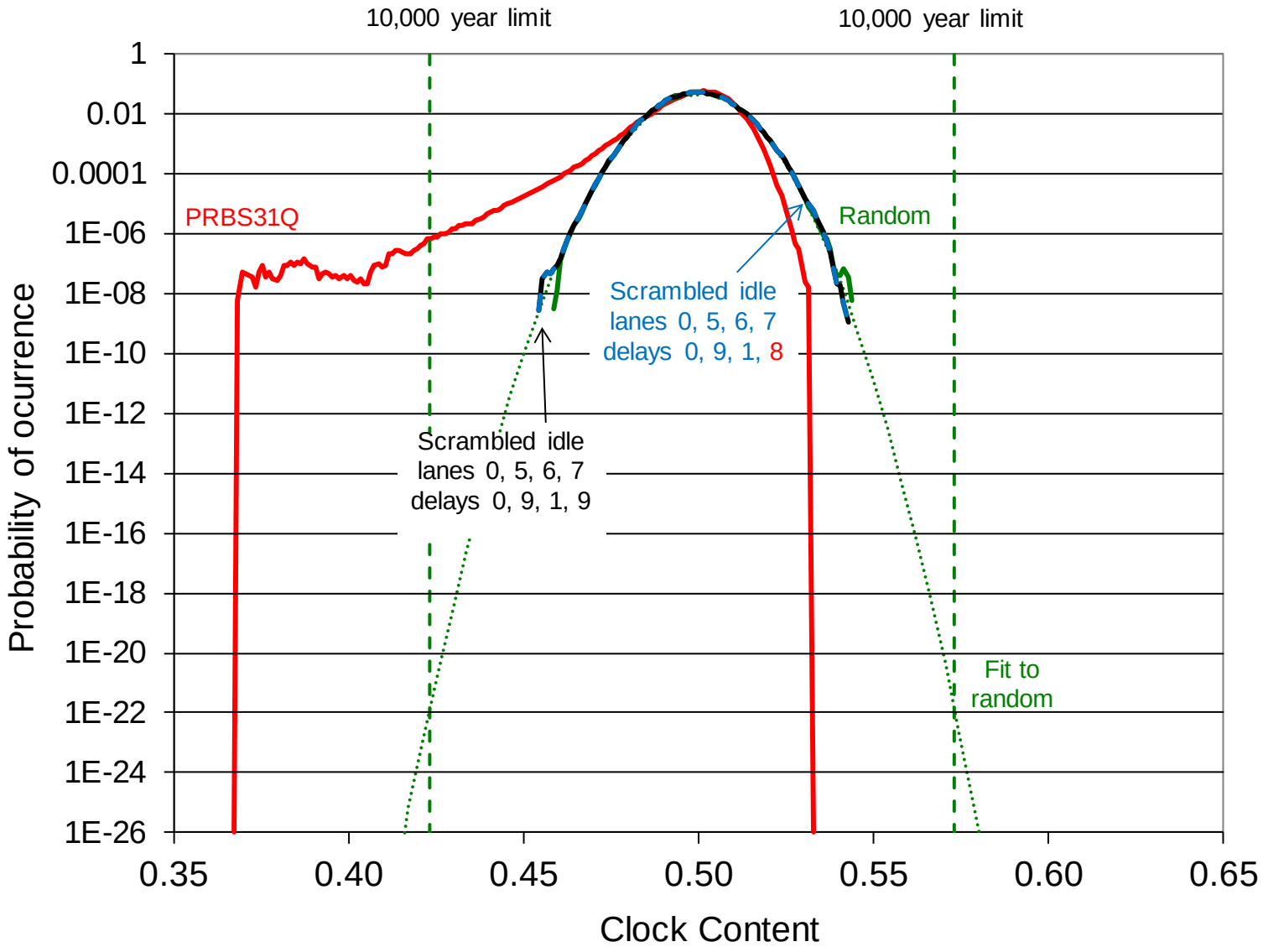
200GbE baseline wander, 0, 5, 6, 7



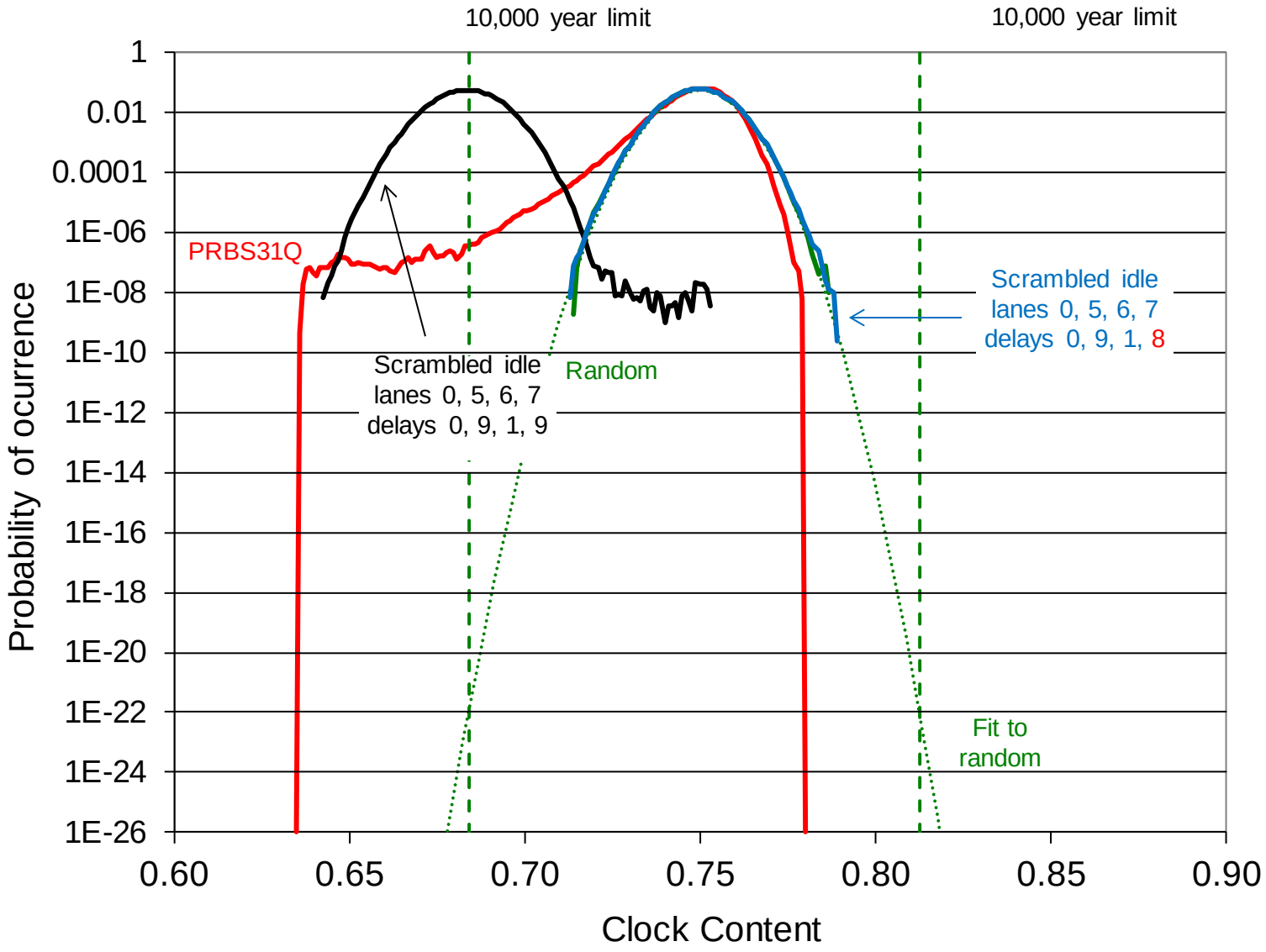
200GbE clock, sym trans through ave, 0, 5, 6, 7



200GbE clock, trans through ave, 0, 5, 6, 7



200GbE clock, all transitions, 0, 5, 6, 7



200GbE search

All possible combinations of 200GbE PCS lanes for 4:1 bit interleaving to form 100 Gb/s lanes were searched to find any with unusual Clock Content (CC) after Gray coding to PAM4 symbols. This search included lane delays of -40 to +40 bits.

Out of 892,820,880 possibilities, 1117 were identified as having similar characteristics to the plots shown on the previous slides. These are listed in a companion contribution.

For all identified combinations the delays are in the range 17 to -18 bits.

A search of all possible combinations of 200GbE PCS lanes for 2:1 bit interleaving to form 50 Gb/s lanes with delays from -100 to 100 bits did not find any with unusual Clock Content.

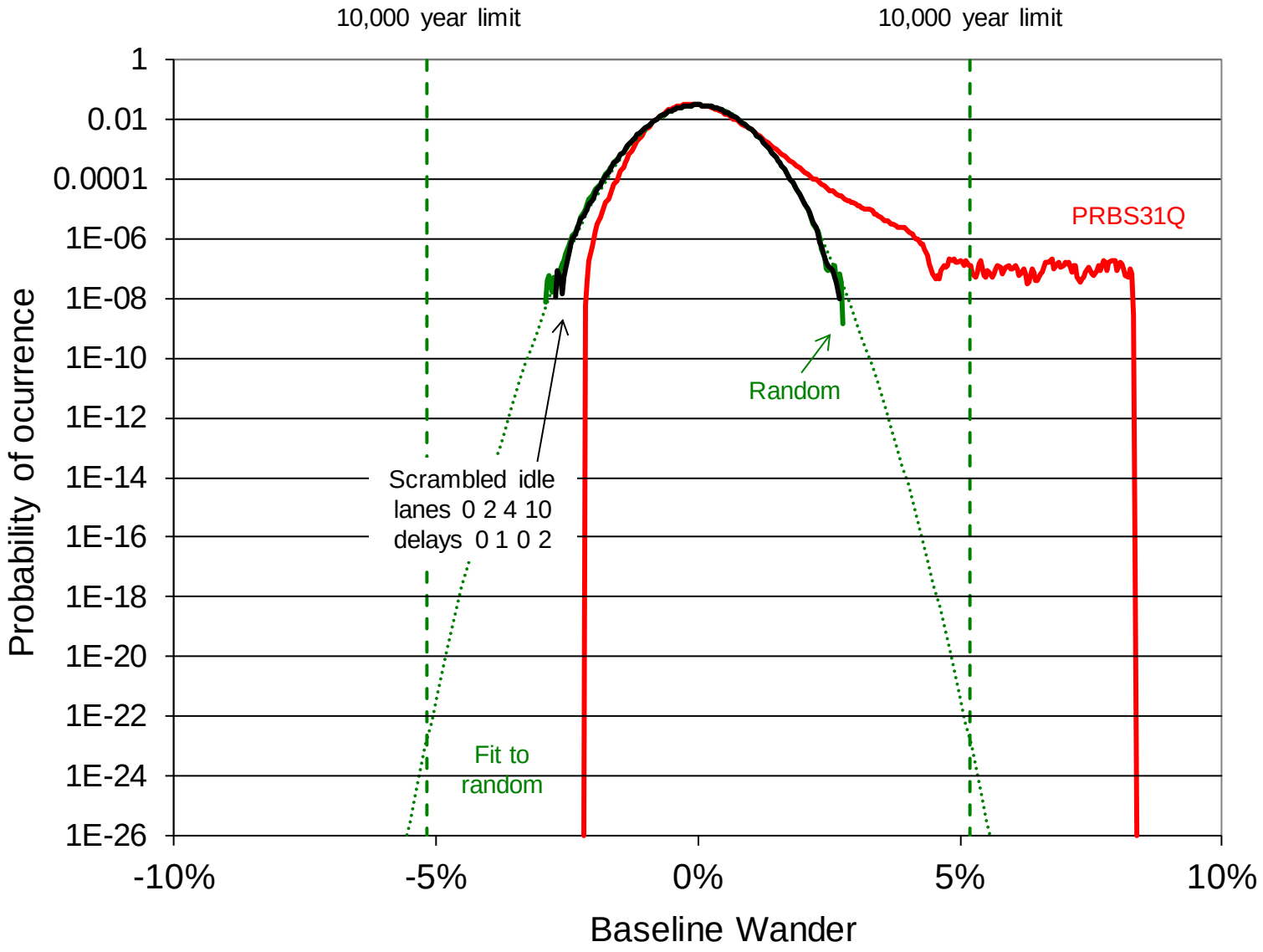
400GbE search

All possible combinations of 400GbE PCS lanes for 4:1 bit interleaving to form 100 Gb/s lanes were searched to find any with unusual Clock Content (CC) after Gray coding to PAM4 symbols. This search included lane delays of -10 to +10 bits.

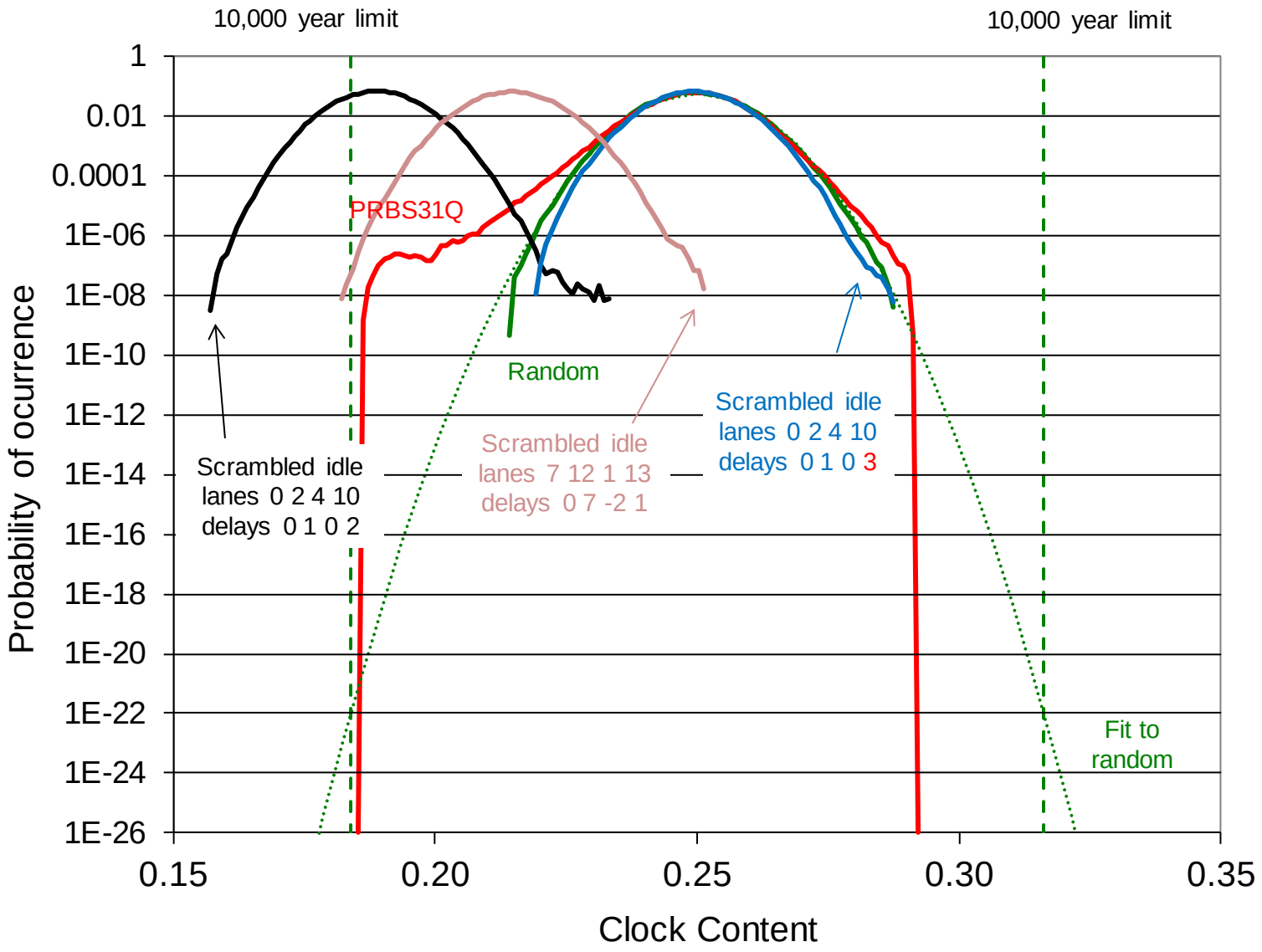
Out of 404,520,480 possibilities, 3162 were identified as having similar characteristics to the plots shown on the following slides. These are listed in a companion contribution.

A search of all possible combinations of 400GbE PCS lanes for 2:1 bit interleaving to form 50 Gb/s lanes with delays from -100 to 100 bits did not find any with unusual Clock Content.

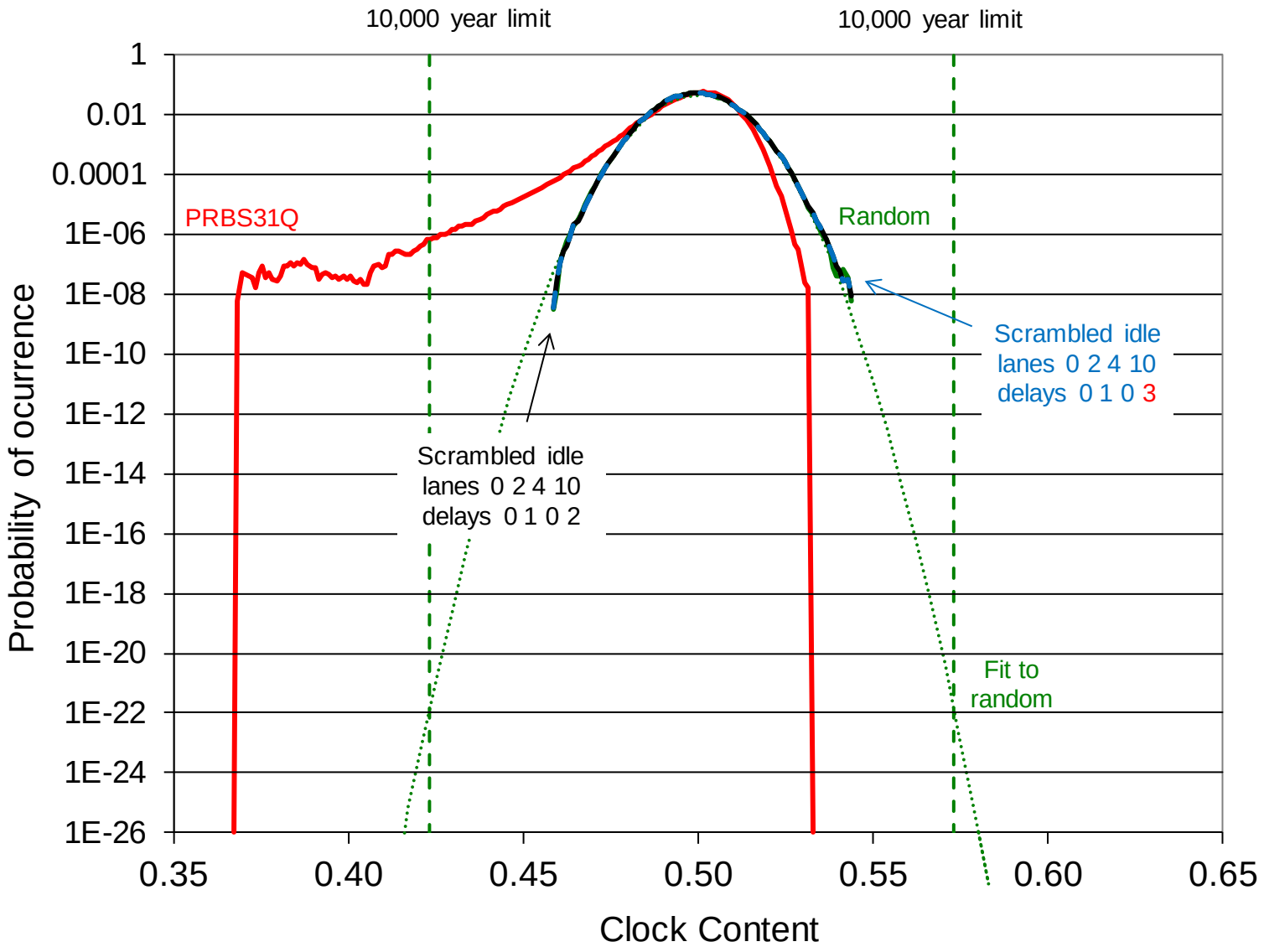
400GbE baseline wander, 0, 2, 4, 10



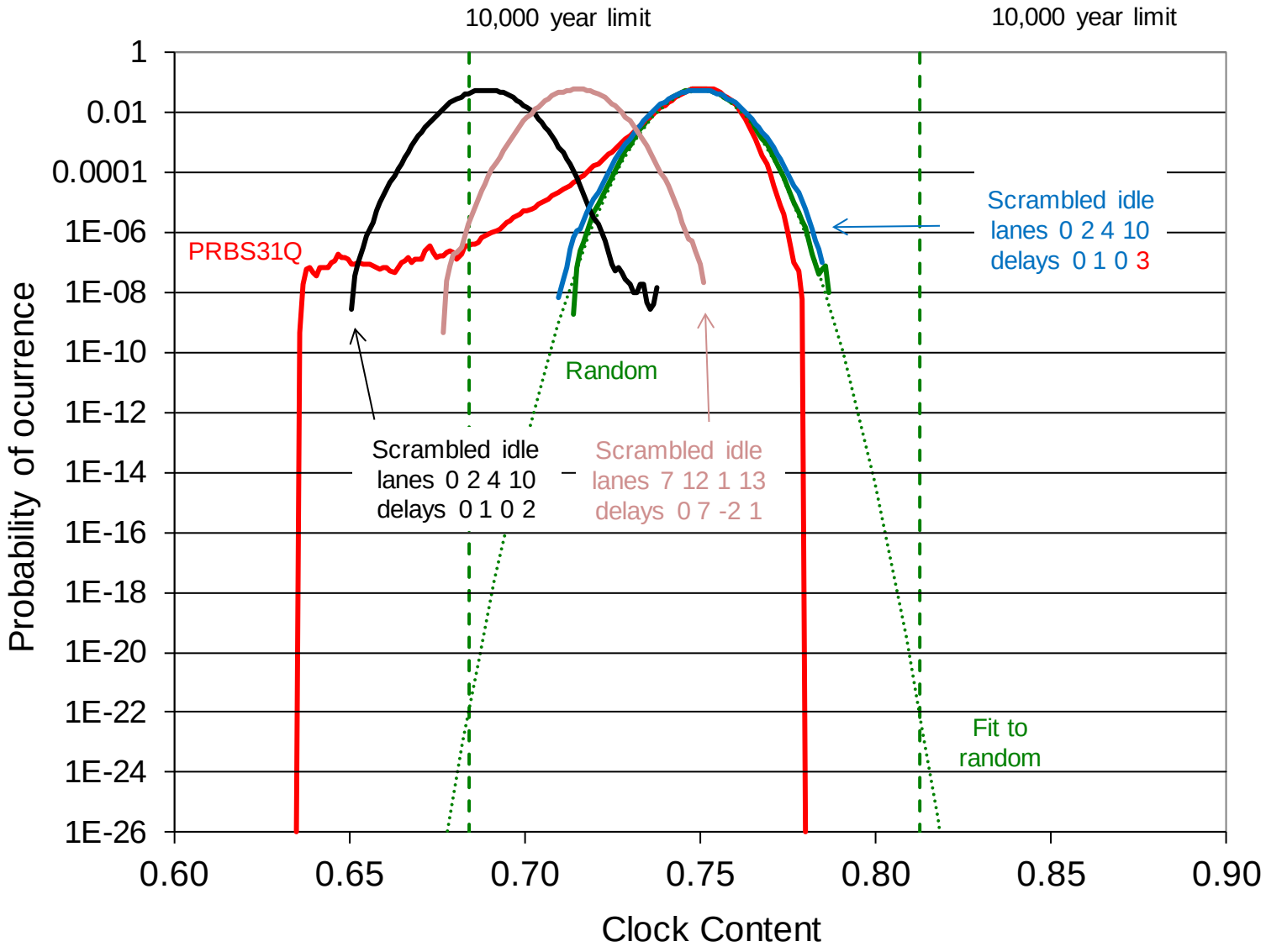
400GbE clock, sym trans through ave, 0, 2, 4, 10



400GbE clock, trans through ave, 0, 2, 4, 10



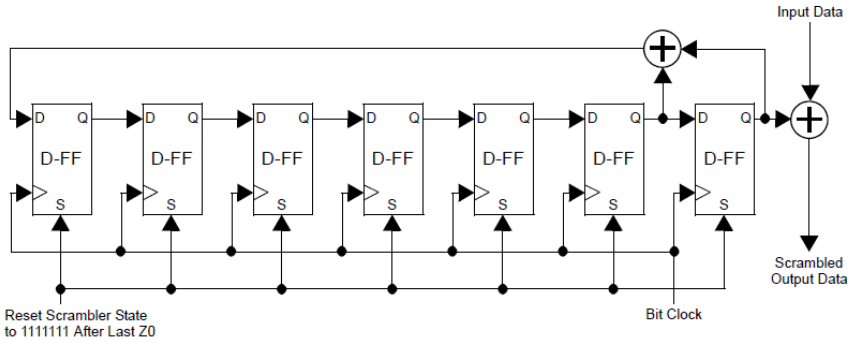
400GbE clock, all transitions, 0, 2, 4, 10



Potential solution

Apply a PRBS7 scrambler to the two 5140-bit messages prior to RS-encoding.

Use the frame-synchronous scrambler shown in Figure 50-9:



Reset the scrambler state to 1111111 prior to first bit of each message. This has no effect on error statistics.

For 200G, do not scramble the first 480 bits of message A or message B if they contain AMs.

For 400G, do not scramble the first 960 bits of message A or message B if they contain AMs.

Result of adding extra scrambler

A search of all possible combinations of PCS lanes for:

- 200GbE 4:1 interleaving with delays from -40 to 40 bits
- 200GbE 2:1 interleaving with delays from -100 to 100 bits
- 400GbE 4:1 interleaving with delays from -10 to 10 bits
- 400GbE 2:1 interleaving with delays from -100 to 100 bits

did not find any with unusual Clock Content when the extra scrambling as per the previous slide was applied.

[Side note: A search of all possible combinations of PCS lanes for:

- 100GbE 4:1 interleaving with delays from -100 to 100 bits as per P802.3cd project

did not find any with unusual Clock Content without any extra scrambling.]

Thanks!