



100Gb/s/Lambda 2km PAM4 with KP4 FEC:

System Modelling & The Big Ticket Items

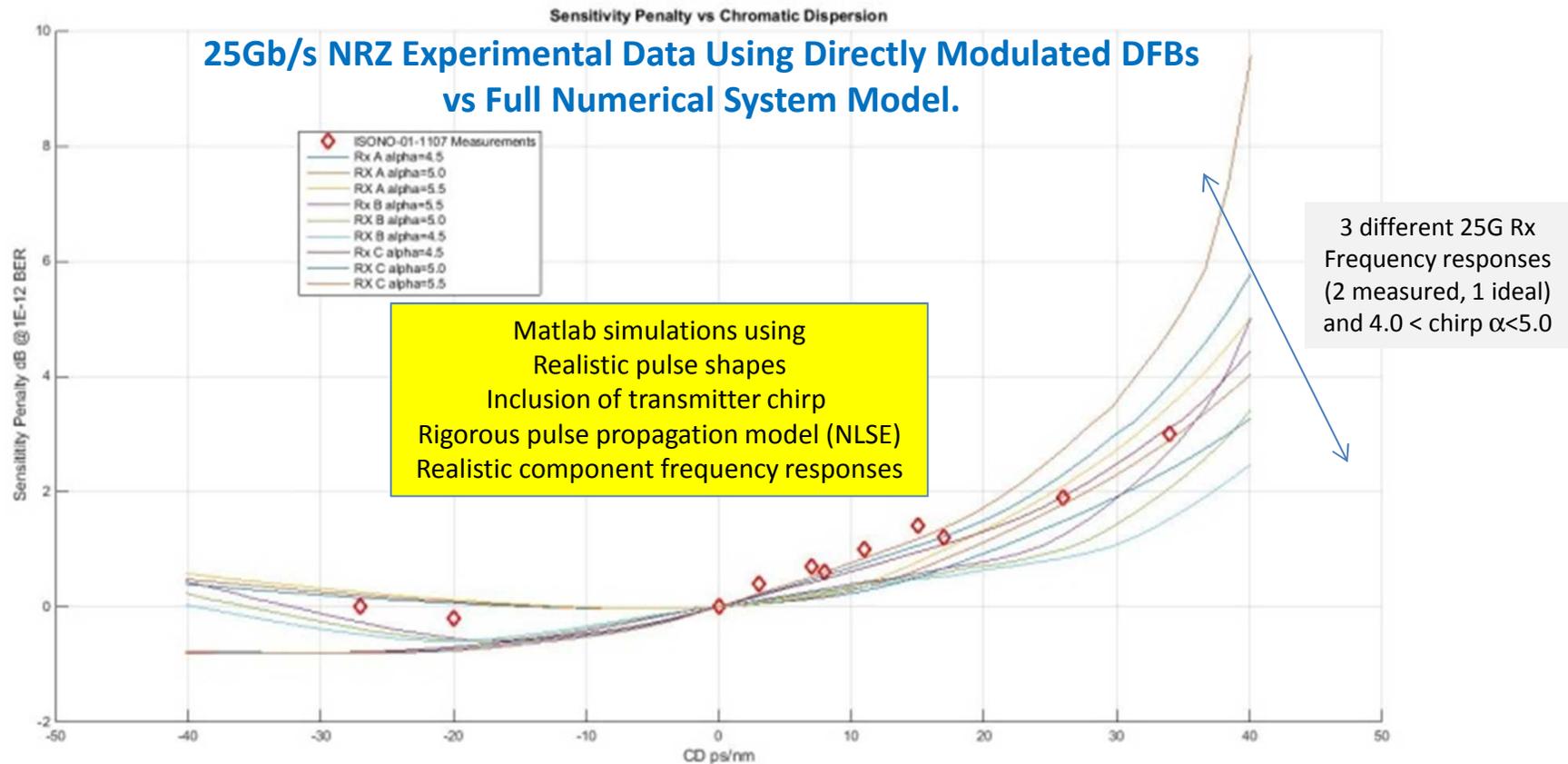
Alan Tipper 24 FEB 2015

Big Ticket Items

- lewis_3bs_01a_0115 (4 x 100G PAM4 Proposal)
 - Allocation for MPI penalty 1.0 dB
 - No separate CD penalty
- minutes_draft_2-Feb-2015_smf.
BTIs common to all proposals:
 - **Dispersion penalty worst case**, TDP
 - **RX sensitivity / technical feasibility**
 - **MPI**
 - More test results
 - Evaluate Coupling between electrical and optical interfaces
- stassar_01_0215_smf
 - Worst case positive dispersion 2km (1337.5nm) nm: +6.68 ps/nm
 - Worst case negative dispersion 2km (1264.5nm): -11.88 ps/nm
 - “These are non-negligible dispersion levels”

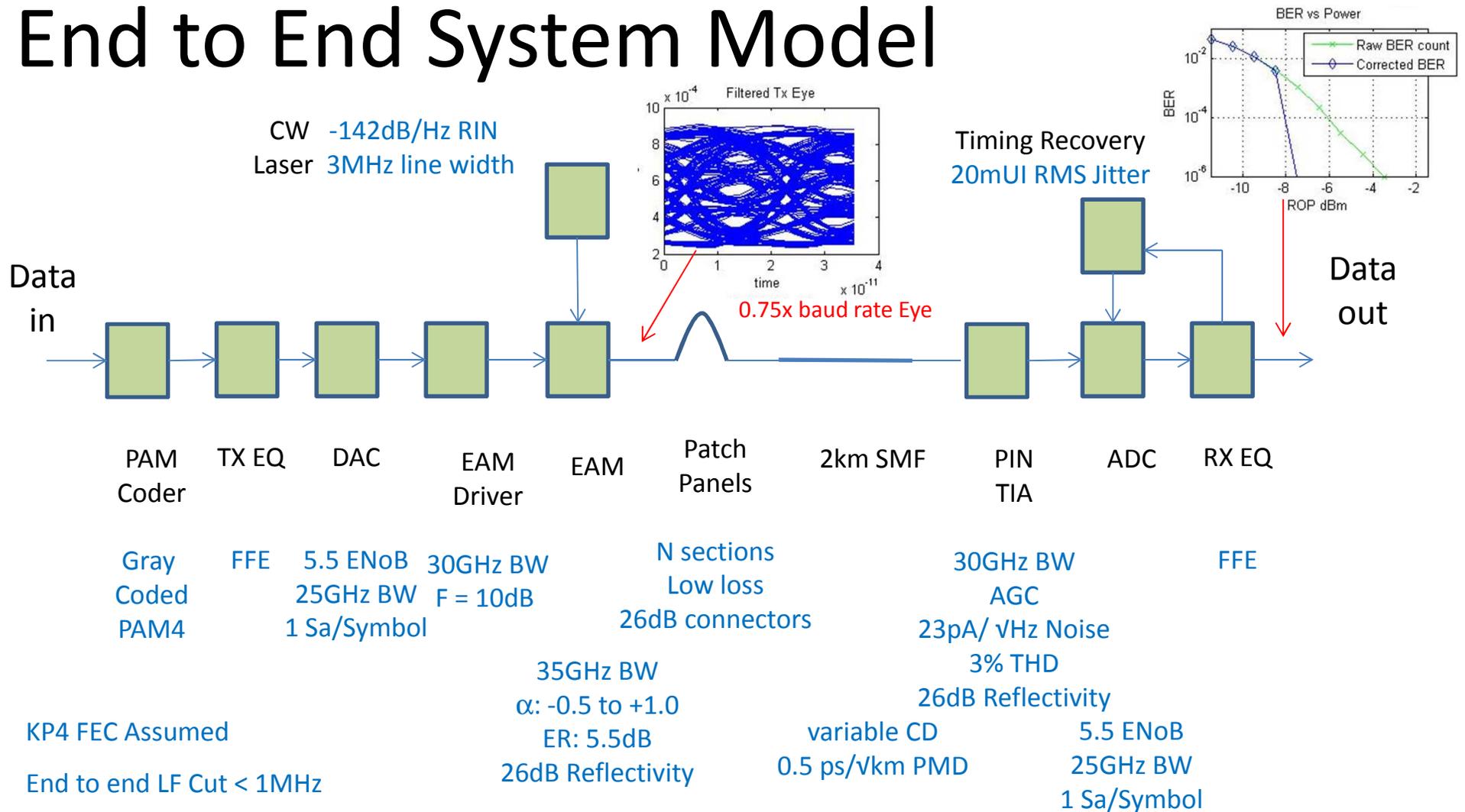
Use of System Models

Concern has been raised over the validity of “modelling” chromatic dispersion effects citing 100G BASE LR4 experimental data from ISONO_01_1107 as an example where models were inadequate.



Full numerical models including chirp are able to predict chromatic dispersion effects

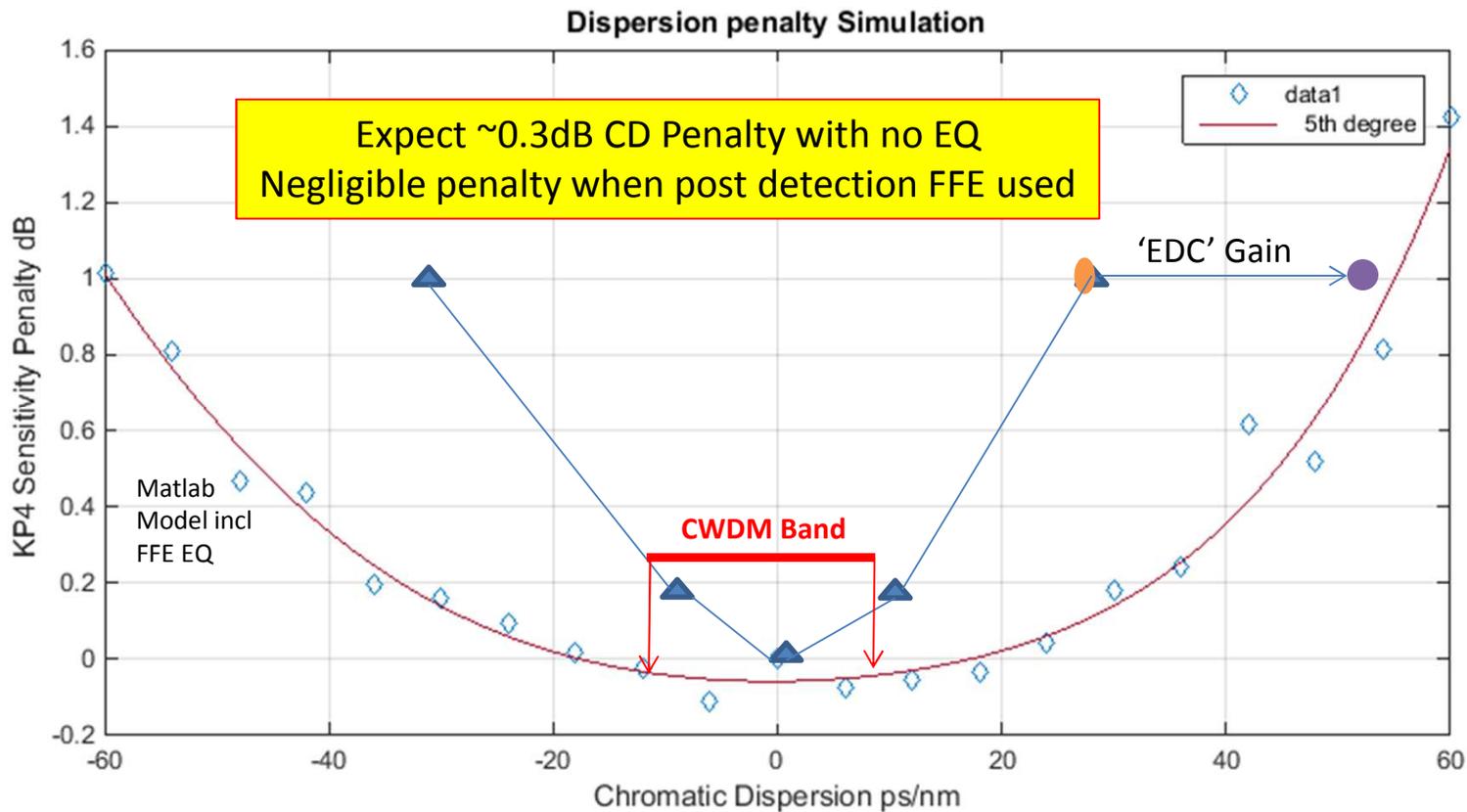
End to End System Model



Reference Architecture: Not intended to constrain Implementations

Matlab based non linear system model used for impairment analysis

CD Simulations



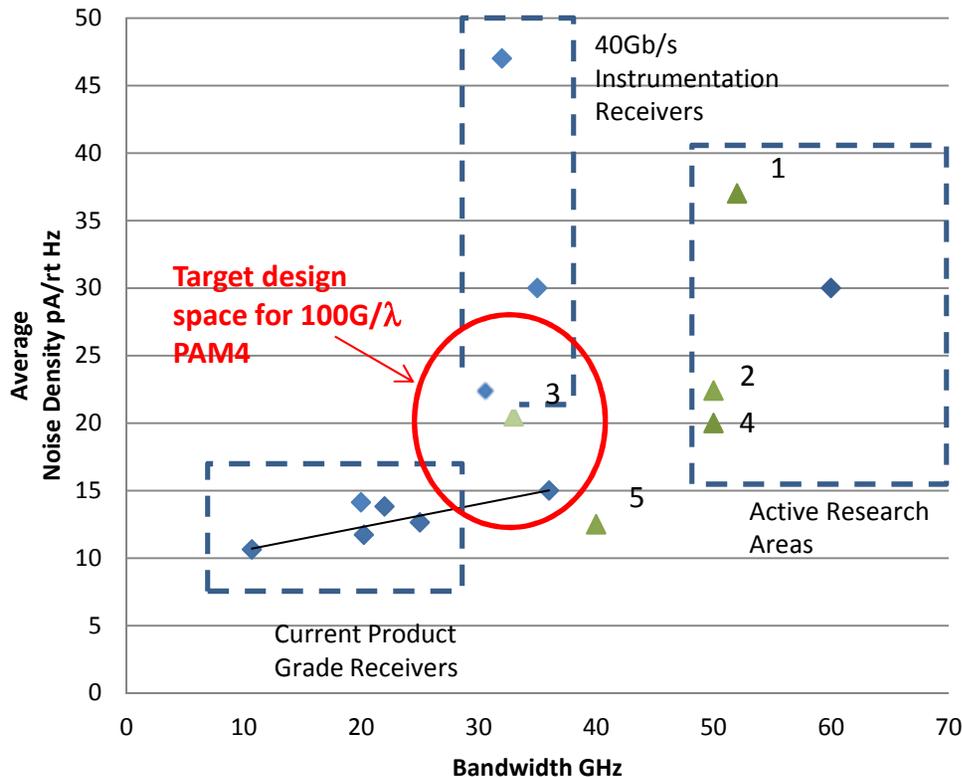
- ▲ No EQ Simulations, ideal High BW Tx & Rx zero chirp MZI
- Nicholl_01_0312_NG100GOPTX 25GBaud result scaled to 50GBaud (x 0.25)
- Based on NRZ SMF-EDC Experiments at 10Gb/s ref: S. L. Woodward et al, Demonstration

of an Electronic Dispersion Compensator in a 100-km 10-Gb/s Ring Network.
IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 15, NO. 6, JUNE 2003 (shows doubling of SMF-CD limit with EAM Tx using FFE)

RX Sensitivity / Technical Feasibility

Update to Tipper_01_3bs_0914

TIA Noise Trends



- ◆ Commercial deployments
- ▲ Research Publications

1. Monolithic Photoreceivers for 60 Gbits/s and Beyond
H.-G. Bach
OFC 2003 ThZ1
2. A 50-Gb/s Differential Transimpedance Amplifier in 65nm CMOS Technology
Sang Gyun Kim, Seung Hwan Jung, Yun Seong
Taiwan Asian Solid-State Circuits Conference
IEEE November 10 - 12, 2014/Kaohsiung,
3. A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS
Jooхва Kim, and James F. Buckwalter
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 47, NO. 3, MARCH 2012
4. SiGe Differential Transimpedance Amplifier With 50-GHz Bandwidth
Joseph S. Weiner, Andreas Leven, Vincent Houtsma, Yves Baeyens, Young-Kai Chen, Peter Paschke, Yang Yang, John Frackoviak, Wei-Jer Sung, Alaric Tate, Roberto Reyes, Rose F. Kopf, and Nils G. Weimann
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 9, SEPTEMBER 2003
5. A 40-GHz Bandwidth Transimpedance Amplifier with Adjustable Gain-Peaking in 65-nm CMOS
Ran Ding, y Zhe Xuan, Tom Baehr-Jones, Michael Hochberg
2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS),

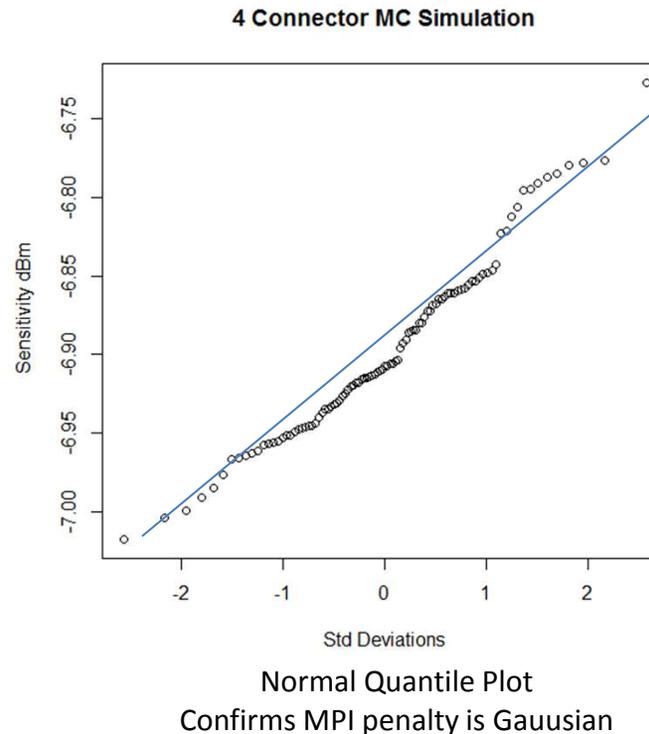
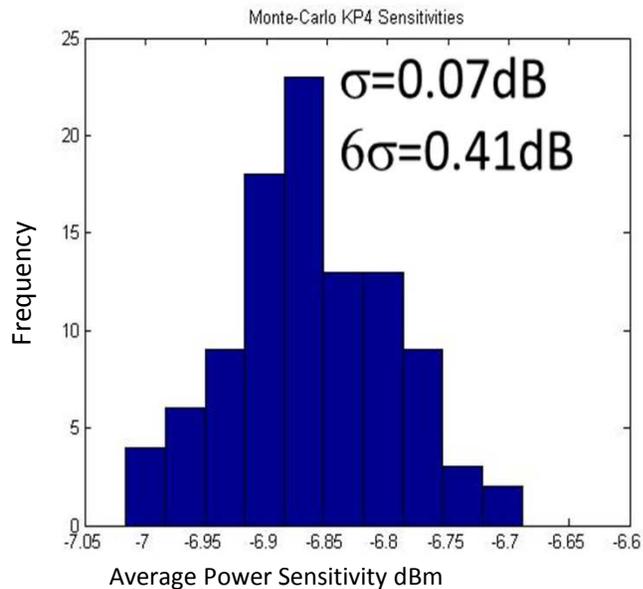
The TIA design space for 100Gb/s/λ PAM4
Is an extension of existing 25Gb/s & 40Gb/s product technology
and not dependant upon 'Futuristic Technology Research'

MPI: Monte Carlo Simulation

4 x 26dB connectors + Tx & Rx Reflectance

Randomized reflection phase & prop delay

KP4 FEC



Numerical trials with randomized reflection phases & path delays suggest 0.5dB is adequate for MPI penalty with 26dB connectors.

Summary

- Full numerical modelling has been shown to accurately predict chromatic dispersion effects when chirp is accounted for.
- CD Penalties for Equalized 2km 4 x 100G CWDM PAM4 should be negligible. Unequalized schemes should show < 0.3dB
- Rx Technology is an extension of existing designs at 25Gb/s and 40Gb/s and is not dependant upon fundamental research work. Current research frontier is low noise 50GHz+ bandwidths which is well beyond what we need for 100Gb/s/ λ PAM4 (~30GHz).
- End to End Monte-Carlo Simulations of 100Gb/s PAM4 assuming KP4 FEC indicates 0.5dB MPI link budget penalty is sufficient with 99.98% confidence for 6 reflections with 26dB back reflection and low loss
 - This will be significantly reduced by realistic connector return losses >>26dB
- 1dB Path penalty for MPI and CD is sufficient.