Power Matters

IEEE802.3bt 4-Pair Power over Ethernet Task Force

PD Diodes model and Vdiff at low and high current vs. E2EP2PCUNB

Mathematical Analysis, Simulations, Lab results

Rev 007

Supporters:

Christian Beia / ST
Dave Dwelley / LT
Lennart Yseboodt / Philips
Jean Picard / TI
Rimboim Pavlik / MSCC

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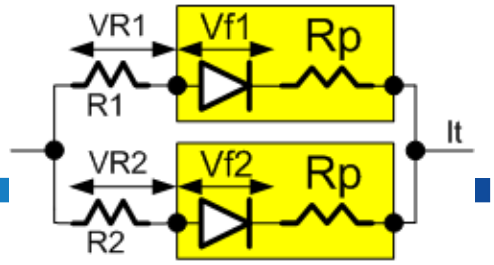
Yair Darshan
Microsemi
ydarshan@microsemi.com

Executive Summary-Updated research results (1)



Note for revision 6; Typos while adjusting results from 5mA to 5.5mA was corrected and marked in **RED.**

- Diode Vf_max and Vf_min and as a result Vdiff_max is found at low current. See Annex B1-B11**.**
  - We care about Vf only and not Vd. We have access to Vd and not Vf.
  - Vf=Vd-Id*Rp. Rp=internal resistive loses that helps balance Vdiif effect on P2P_Iunb.
  - Only at low current Vf=Vd. Therefore we test Vf at low current.

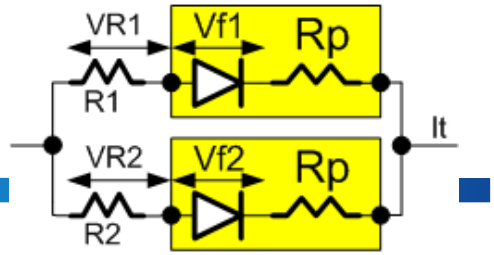
- We are focusing on Vf differences between diodes that affects P2P_Iunb at low current.

- At high current Vdiff effect on p2p_Iunb is reduced by a factor of 1/(VR1+VR2).
  - It is due to higher voltage drop on resistive elements (Rp+R) that reduces Diode Vdiff weight on the effect on P2P_Iunb. R is the pair end to end resistance. **See Annexes B12-B14**.

- PD_Vdiff need to be limited by specification (OR by other relevant parameter, see later alternative specifications) to values below the worst case found in the market in order to guarantee some minimum current over a pair to allow independent DC disconnect functionality over each pair-set and open wire detection.
  - There are solutions that are not requiring limiting Vdiff of diodes. **See Annex M for examples.**
  - There are solutions that PSE don't care about PD p2p_Iunb at low current. **See slide 17**

- Final PD Vdiff_max value will be reduced by PSE Vdiff later.
- In this work, VPSE Vdiff was set to 0. Later PD Vdiff will have to be reduced by PSE_Vdiff value.
  - (P2P_Iunb is function of total system P2P_Vdiff. i.e. Vdiff=PSE_Vdiff+PDVdiff.

Executive Summary-Updated research results (2)



- **Specifications possible solutions**
- (1) Limit PD P2P input voltage offset at MPS current range to Vdiff_max=34mV for having 5.5mA minimum over pair when PD min. current=22mA

  -Previous presentation version proposal was 34mV for having 5mA min with 20mA load

  - Total system Vdiff is 36mV. Reducing PSE Vdiff=2mV results with PD Vdiff=34mV.

  - Higher PD Vdiff can be used if minimum PD current is increased by 0.7mA per 1mV increase in Vdiff up to 120mV max (TBD, is limited by max. pair current requirements, transformers and PD available power. See Annex D8) . It increases PD design flexibility. **See slides 18,19 for detailed calculation conditions**)

- Alternative **implementation independent** specifications solution:

- (2) Specifying guaranteed PD minimum pair current=5.5mA (TBD) when PD total MPS minimum load is 22mA.

  (It is equivalent to solution (1) without limiting Diode Vdiff at low current.

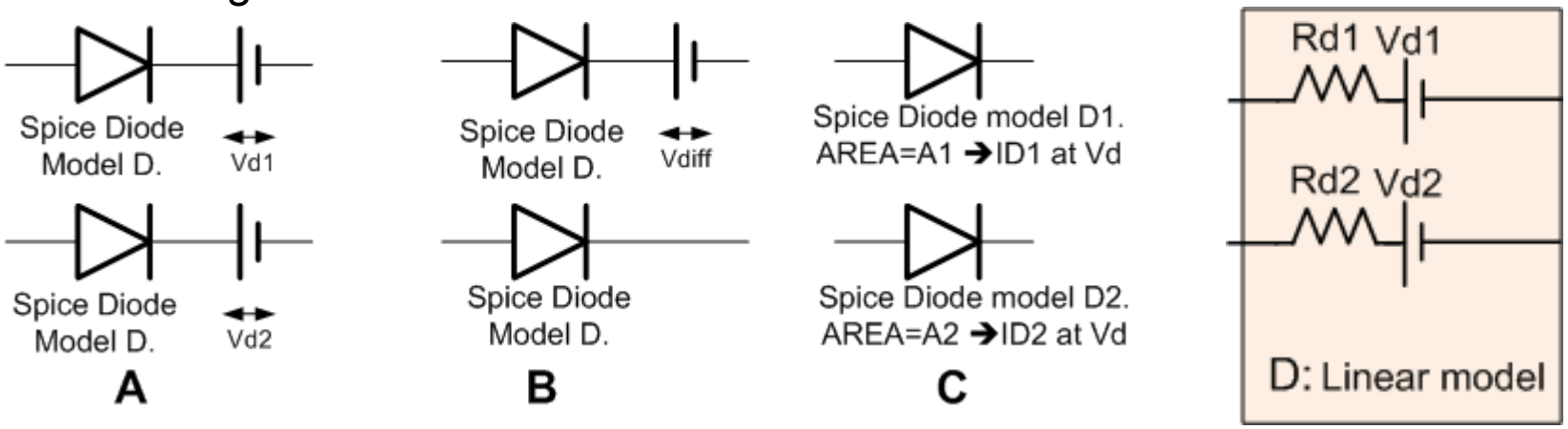
  - Specifying PD pair maximum current, Imax at 4P operation for high currents.

Objectives

- Present the diode models that are used in our system unbalance research.
  - Reflects behavior of decreasing Vdiff effect on P2P_Iunb when current is increased
  - Reflects accurate behavior at low currents
- Finding PD diode to diode Vf differences that are currently used in PDs:
  - Analytical Calculation – Prediction of the possible max values
  - Lab results of Diode Vdiff only
  - Characterization data from diode vendors
  - Lab results of system unbalance at short channels as function of Vdiff
- Deciding what is the Vdiff_max for achieving the desired system unbalance at low currents (DC disconnect range) and yet allow for low cost implementations in the PD e.g. allowing using PN or Schottkey diode and/or alternative parameters.
  - At high currents Vdiff effect on P2P_Iunb will be lower, resulting with better P2P_Iunb.
- Why we are doing this?
  - Vdiff is needed for calculating final system end to end channel pair to pair resistance/current unbalance at low and high current.
  - As a result, maximum pair current under unbalance conditions can be calculated.
  - Recommendations for DC disconnect current thresholds can be evaluated
  - Then we can specify PSE and PD PI unbalance parameters

Existing diode models used in E2ECP2PRUNB adhoc database slides. (See complete system model in Annex F)

- See details in Annex A1, A2, A3, A4, A5 and A6.
- Models A,B and C are equivalent diode models for simulating current unbalance at low and high loads. All verified with simulations and lab tests.



- Model A: Vdiff=Vd1-Vd2. Diodes are the same spice diode model.
- Model B: Just using Vdiff in series to the diode.
- Model C: Same Spice diode model with different numbers for AREA parameter OR complete different Spice model parameters set for each diode. **See Annex A6**. It creates different vf / Id curves.
- Model D: Diode linear model. Accurate for high currents. Can't be used for low currents. **See Annex A1-A6**

The questions are:

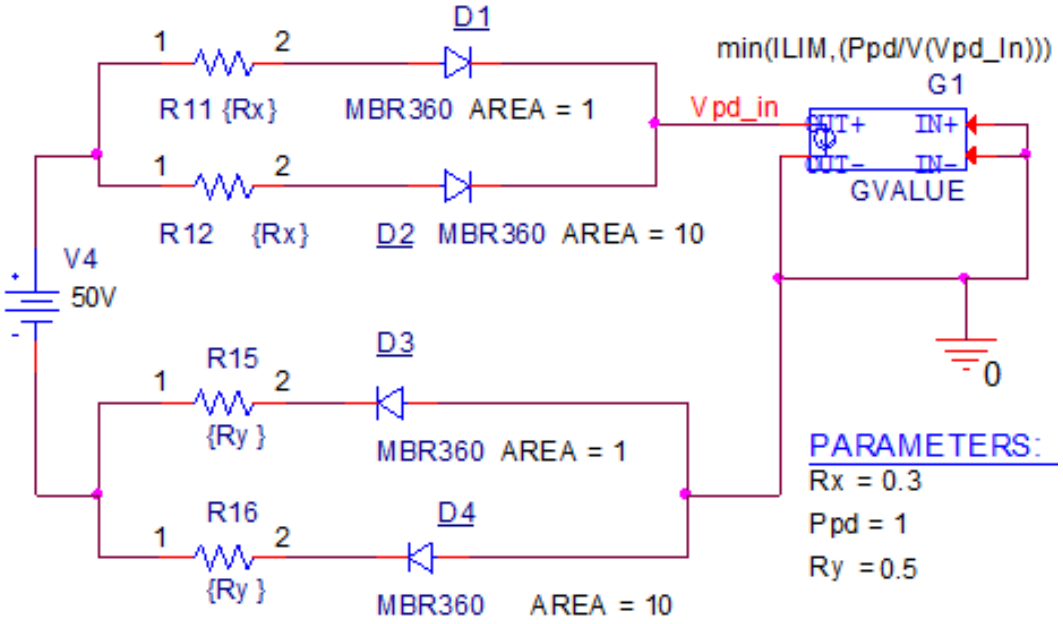
1. What is Vd1-Vd2=Vdiff_max that exists in typical PD implementations?
2. To which value to limit Vdiff for meeting our system P2P Iunb needs?

What is Vd1-Vd2=Vdiff_max that exists in typical PD implementations?

- We can get the answer from the following data sources:
  - Mathematical Analysis
  - Simulations
  - Lab results
  - Diodes Data Sheets (Characterization data)
- Comparing between them and select **worst case realistic value that represents** existing diode solutions. *Then we can generate diode model that behaves accordingly and use it in our simulations.*
- Why we are doing this?
  - To answer the question if we can use this data as it is in our PD P2P_Iunb specifications or ask for tighter diode Vdiff_max requirements?

Mathematical Analysis: Vdiff at Low current and short channel

- See Annex **B1 to B15** for details.
- Vf_max and Vdiff_min between diodes are found at low current test. See Annex B6.
  - Vf=Vd-Id*Rp. Only when Id is low, Vf=Vd. We need Vf.
- P2P_Iunb=(Id1-Id2)/(Id1+Id2) on positive pairs. P2P_Iunb=(Id3-Id4)/(Id3+Id4) on negative pairs.
- Key point: At low current and short channel, D1 and D2 are in parallel.
  - Vd1=Vd2=Vd_min=Vf_min. Equation can be solved.



$$Id_1 = Is_1 \cdot \left(\exp^{\frac{q \cdot Vf_1}{n_1 \cdot k \cdot T}} - 1 \right)$$

$$Id_2 = Is_2 \cdot \left(\exp^{\frac{q \cdot Vf_2}{n2 \cdot k \cdot T}} - 1 \right)$$

$$Vf_1 = Vf_2 = Vf_{\min}$$

Mathematical analysis: Possible Vdiff range at low current.

- See details in Annex B1 to B15.
- The main factors affecting I_d is the diode reverse current I_s and the silicon material Ideality Factor n.
- Typical diodes will be with n1=n2≅1. Is2/Is1=10 (assumed process accuracy of the area in which current is flowing) at T=300°K (~27 °C) and k*T/q=25.85mV we will get:

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 59.5mV$$

Significant probability of Vf_min and Vf_max at the same time on pairs of the same polarity at the same port. **See Annex J and slide 12 .**

- Vdiff_max is found by using n=2 and Is2/Is1=10 at the same time.

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 119mV$$

- Or Is2/Is1=100 with n≅1:

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 119mV$$

Very low probability of Vf_min and Vf_max at the same time on pairs of the same polarity at the same port. **See Annex J.**

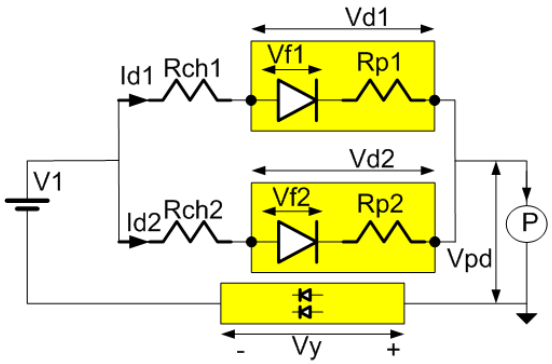
- Conclusion: Math agrees with lab characterization.
  - Vdiff_max will gets ~120mV between two random components

Mathematical analysis: Vdiff at High current

- At high currents Vdiff effect on P2P_Iunb is significantly reduced by the voltage drop on all the resistive elements (PSE PI, PD PI, cables and connectors) that reduces the weight of diode Vdiff in the P2P Iunb equation.

$$Iunb = \frac{Vd_2 - Vd_1}{VR_2 + VR_1} = \frac{Vdiff}{VR_2 + VR_1}$$

for VR_1 and VR_2>0



  - It helps even at short cable.
  - At longer cables it is significantly improve the 2P_Iunb

- See Annex B12-B14 for details.
- See Annex D8 and D9 for simulation results
- We focus on low currents case because this maximizes Vdiff effect at short and long channel.
  - Once it is defined, it will be used for high currents as well.

Lab tests: Diode characterization at low current

- Diode part number: STPS2H100
  - Source: Christian Beia /ST

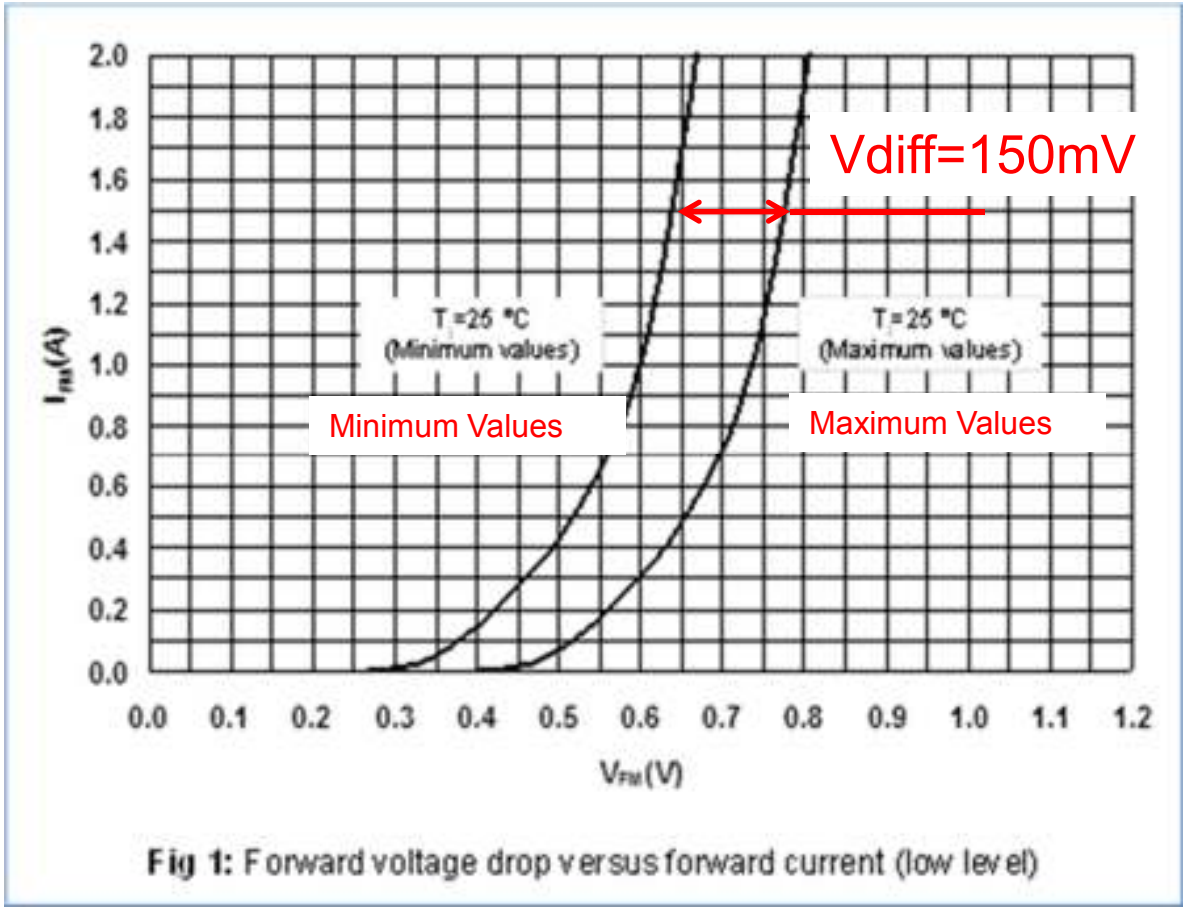


Fig 1: Forward voltage drop versus forward current (low level)

- Vdiff=150mV
- Vdiff extends 6 sigma (w. assumption).
- Vdiff_max is ~constant regardless of Vf. (*So Vdiff can not be specified as Vdiff/Vf=α_max=constant.)*
- Ta=25°C

- See Annex J for the probability to get Vf_min and Vf_max resulting with Vdiff=150mV on the same port and on the same pair.

Lab Results

Maximum Vdiff of diodes of same part number and vendor that are used for PoE applications:

~406-295=111mV ➔ ~110mV.

- **Part #1:**
  - 16 items: Vf=401mV to 406mV
  - 43 items: Vf=295mV to 303mV
- **Part #2:**
  - 60 items: Vf=300mV to 310mV.
- Total 120 units.
- Schottkey diodes
- All diodes were tested with constant current of 5mA. See Annex B6.
  (Testing with different low current will results with similar Vdiff)
- Although the results make sense compared to the other data sources, larger samples with more P/N are required to draw final conclusions for the above information source (Lennart plans to do it for March 2015).

System tests

- Test conditions
  - PSE connected to PD through 1m cable (short channel).
- System test results
  - Low load current (12mA load was in that tester)
    - 1.5mA on one pair and 10.5mA on the 2nd pair.
    - 1.25mA and 8.75mA with 10mA load. (converting as if it was 10mA load).
- The E2ECP2PRUNB_max was 75% which is equivalent to PD Vdiff =~60mV
  - See Annex D7 for the curve used to transfer from P2P_Iunb to Vdiff.

Summary of PD diode Vdiff data sources of currently used diodes in the market.

Source	Vdiff max. [mV]	Notes
Manufacture Characterization	150 to 170	-See note 1 for probability to happen.
Mathematical Analysis	120	-See **Annex B** for details. -See note 1 for probability to happen.
Lab tests of discrete diodes	110	-See note 1 for probability to happen.
	10	66% of two part numbers,60 samples each. Waiting for larger sample tests for confirmation.
System tests of Iunb at 10mA load. Very large sample.	60	-Significant probability to happen on the same pair.

Notes:
1. Probability to have both Vf_min **and** Vf_max on the same port **and** on the same pair is well below 10^-11. See Annex J for details.

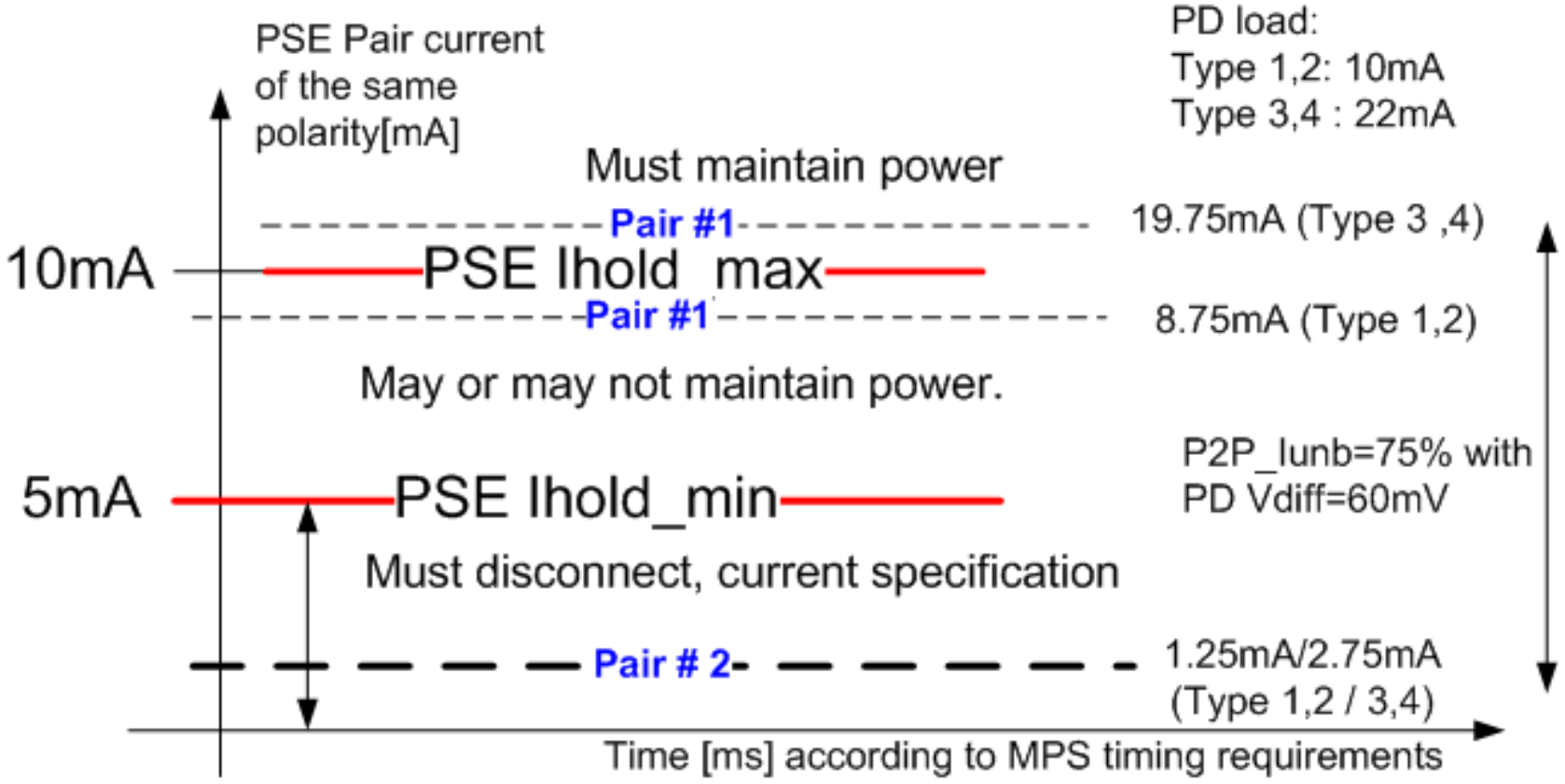
Conclusions: PD diode Vdiff currently used.

Source	Vdiff max. [mV]	Notes
*Discrete diode r*ealistic worst case value *on the normal curve* for Vdiff=Vf_max-Vf_min:	120	-Low probability to happen on the same pairs of the same polarity. See note 1 below.
	60	***-Possible to happen.***
	10	66% of the diodes of same part number and same manufacturer . Waiting for larger sample tests to confirm it (Lennart).
Notes: 1. Probability to have both Vf_min **and** Vf_max on the same port **and** on the same pair is well below 10^-11. See Annex J for details.		

- Next question would be:
- What is the Vdiff_max specification for the PD to meet our system needs?
  - Focusing now on P2P_Iunb at low current.

What is the PD Vdiff that we need? – Current Spec.

- The answer is: The value at low current that is required for DC disconnect.
- The following is P2P_Iunb at low current with existing Schottkey diodes in PDs at short channel.
- Pair #2 may disconnected with the current Ihold_min at diff=60mV.



Possible DC Disconnect Solutions (1)

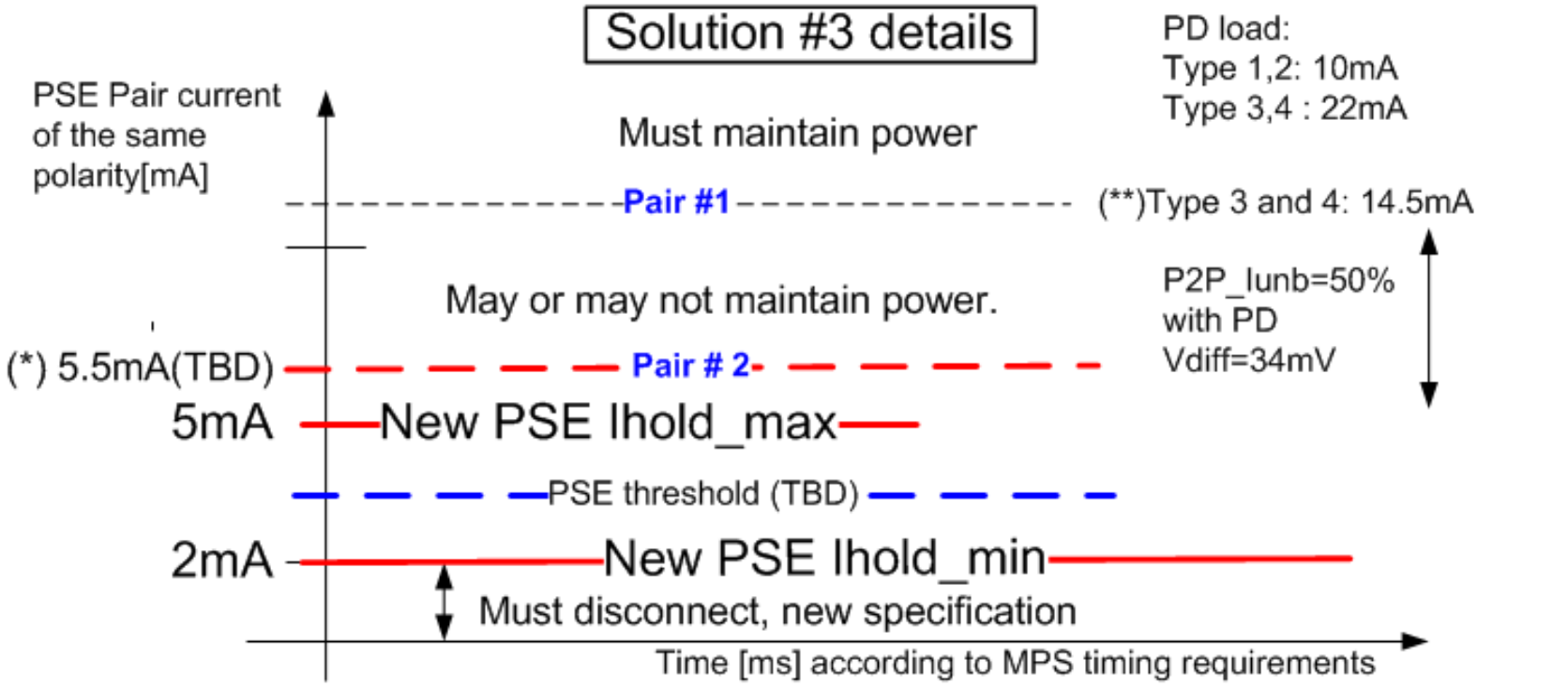
- Solution #1: Look at the sum of both pairs current. (See Annex K)
- It can be done by single MOSFET or Dual MOSFET power channel architectures.

- Solution #2: After connection check if single load PD was identified:
  - Monitor the pair with the highest current for DC disconnect function
  - Monitor the 2nd pair for I>0 (to prevent powering open pairs)

- Solution #3:
- Objective: To allow interoperability and backwards compatibility between Different PSE and PD types. It can be done by full DC disconnect functionality for each pair-set independently by:
  - Tighter PD Vdiff requirements (lower than 60mV) at 22mA (TBD) minimum total PD load. This to guarantee minimum 5.5mA (TBD). It solves P2P_Iunb for any current down to 100uA load range.
  - Equivalent solutions without limiting PD Vdiff are presented too.
- It is desired to allow all possible solutions in the specification for flexible PSE system architectures.
- In addition, it will ease the design of low cost PD implementations. See next slides.

Addressing solution #3 for DC disconnect (2)

- **First step for all solutions in Type 3 and 4 systems**: In order to make it easier to monitor DC disconnect and monitor open wires over each pair set, it is suggested to lower Ihold_min from 5mA to 2mA (not lower than 1mA, noise, accuracy etc.).



(*) PD minimum guaranteed pair current with narrower Vdiff or minimum PD current over pair request
(**) P2P current distribution if we ask nothing from PD

Back to: What is the PD Vdiff that we need for solution #3.

- So what is the Vdiff_max that we want to allow in the PD?
- The answer is: The value that guarantee >5.5mA (TBD) minimum on a pair at short channel conditions (<3m (TBD) patch cord) with a minimum load of 22mA
- **Example calculation for 802.3bt PDs including PSE PI Vdiff=2mV:**
- If (This is example):
  - Minimum MPS current at the PD is =22mA **and**
  - I_hold_min at PSE spec is 2mA instead of 5mA **and**

    (Ihold_max stays 10mA in PSE specification for Typ1, 2, 3 and 4 PSEs)

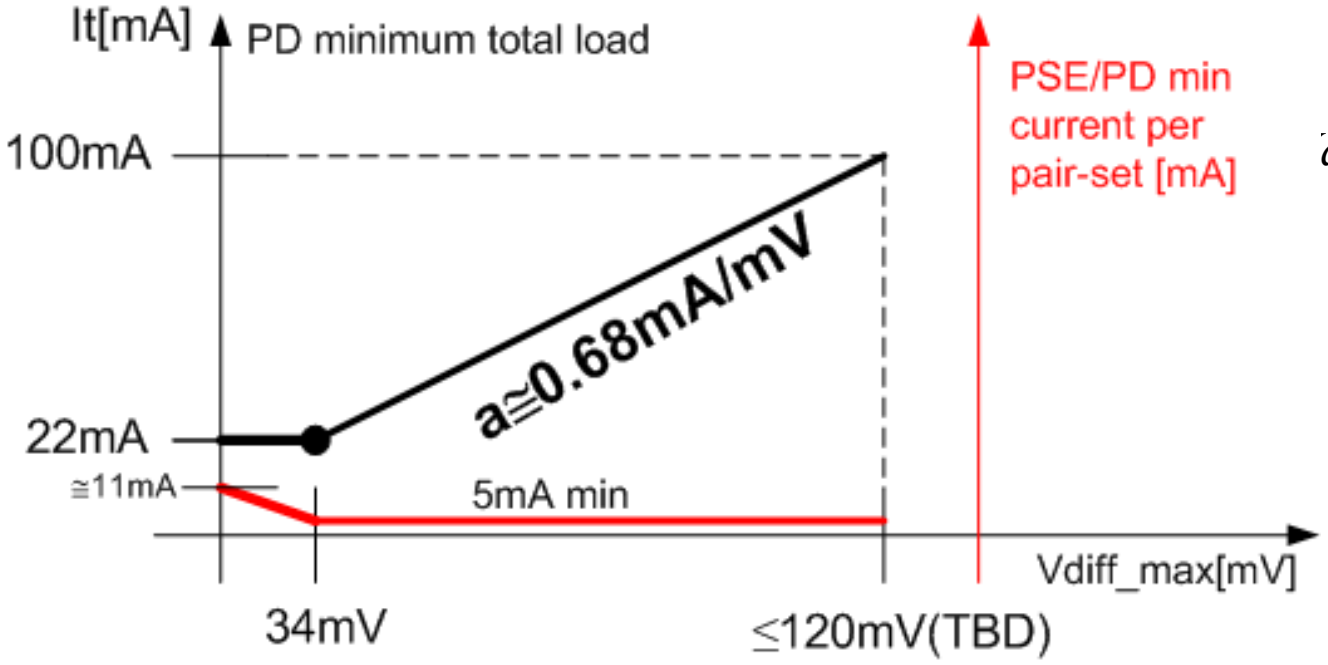
    I_hold threshold set point at PSE is 3.75mA

    Total end to end pair resistance over pair-set is 0.5Ω (worst case over the negative pair)
- Then:
  - Ipair a ≥5.5mA.
  - Ipair b < (22mA-5.5mA)=16.5mA.
  - Iunb<(16.5-5.5)/(16.5+5.5)=50% ➔ Vdiff per Annex D7 chart is 36mV max. Allocating 2mV for PSE PI Vdiff results with PD Vdiff=34mV.

- See next slides for additional PD specifications that increases design flexibility by allowing higher Vdiff_max specification limit in a PD.

What is the PD Vdiff that we need? How to allow higher PD Vdiff?

- **For improved PD design flexibility:**
- PD Vdiff can be higher than 34mV if PD minimum working current is higher than 22mA so 5.5mA minimum over a pair is guaranteed for any Vdif>34mV.
  - The points from the below curve where taken from the next slide.



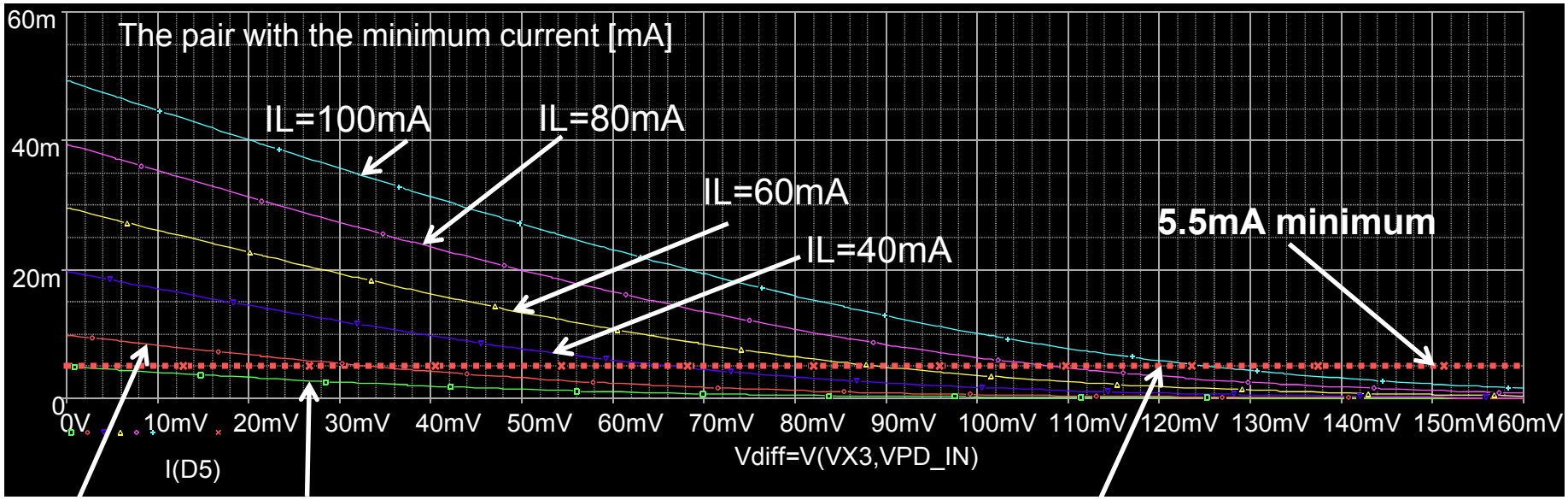
$$Vdiff = \frac{It - b}{a}$$

$$= \frac{It_{\max} - It_{\min}}{Vdiff_{\max} - Vdiff_{\min}} \cong 0.7$$

$$= It_{\min} - a \cdot Vdiff_{\min} = -3.72$$

What is the PD Vdiff that we need?

- PD minimum load IL, vs. Vdiff_max
- The objective is to have 5.5mA (TBD) minimum over a pair.
- Simulation was done with Model #2 setup.



~100mA is required to have 5.5mA minimum over a pair with Vdiff=120mV.

Current PD Diode parameters in Table G1(*)

#	Parameter	Data set 1	Data set 2
9	**Diode Bridge**[9]	Discrete Diodes: 0.39V+0.25Ω*Id min 0.53V+0.25Ω*id max. (TBD)	

(*) From Adhoc report Annex G1 page 33 at:
http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf

- Vdiff=0.53V-0.39V=0.14V (for the linear diode model).
- See Annex A for different diode models including linear model used above.

Suggested new PD Diode parameters in Table G1 And PD Vdiff numbers for 802.3bt Table 33-18

#	Parameter	Data set 1	Data set 2
9	Diode Bridge[9]	See next slides for details, pending the final specification concepts.	

Note 9: Diode model is constructed by Pspice diode model with series DC voltage source for setting different Vf per diode.

Suggested update to PSE Specifications Table 33-11 item 17:

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
17	DC MPS current	Ihold	mA	5	10	1,2	33.2.9.1.2
17a				2	5 (or 7)	3,4	For PD class TBD or higher (*)
17b				TBD	TBD	3,4	For PD class 0-3 (TBD)

(*) to support solution #3.
All new items and numbers are TBD and presented for discussion. However it present the concept that we need address.

Proposal #1: Update PD specification Table 33-18.

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1a	Input voltage pair to pair DC offset of pairs with the same polarity in the MDI_POWER1 state.	VPort_PD_diff	mV		per equation 33-xxx	3,4	
xxx2	the same as in proposal #2 next slide. It_PD_min=22mA.						
xxx3	the same as in proposal #2 next slide. Maximum pair current under P2P_Iunb conditions						

$$Vport\_PD\_diff = \begin{cases} 34 & It\_PD\_\min = 22mA \\ \dfrac{It\_PD\_\min + 1.12}{0.68} & 22mA < It\_PD\_\min \le 80mA \\ 120 & It\_PD\_\min > 80mA \end{cases}_{mV}$$

Eq-33xxx

Where
It_PD_min [mA] is the combined both pair-sets minimum PD input current that is required to support MPS for type 3 and type 4 PDs. I.e. for Type 3 and 4 PD minimum total input current is 22mA.

Proposal #2: Update PD specification Table 33-18.

- Alternative **implementation independent** specifications instead of limiting Diode Vdiff_max at low currents.
- Specifying PD minimum pair current=5.5mA(or higher e.g. 7mA) when PD total minimum load is 22mA.
  - Specifying PD pair maximum current, Imax at 4P operation for high currents.

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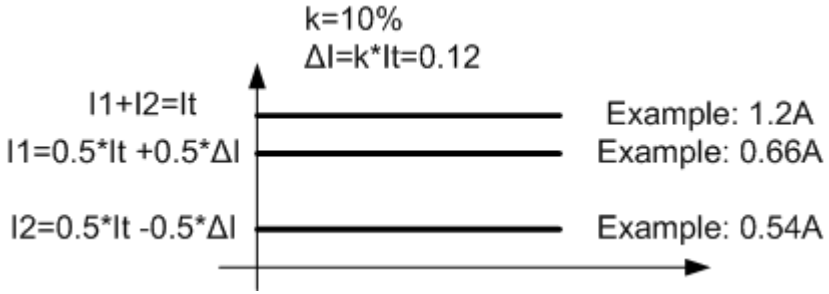
Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
xxx1	MPS current over pair_set	Ihold_gr	mA	5.5(or 7)		3,4	See TBD for test conditions
xxx2	Combined MPS current over both pair_sets	It_PD	mA	22		3,4	See TBD for test conditions
xxx3	Maximum DC pair current due to P2P_Iunb	Ipd_unb	A		Icable*k3	3	See TBD for test conditions
					Icable*k4	4	



K_i=(1+E2ECP2P_C_UNB_i)/2. i=3,4. K3 and k4 are the equivalent (transformed) end to end channel P2P_Iunb for Type 3 and 4 systems.

Proposed Next Steps

- During this meeting (January 2015) to have straw pole to measure the preferences for how to specify the behavior of PD P2P_Iunb at low currents in slides 22-24 .

- During March 2015:
- To finalize concept and numbers with base line text.
- To address the 3 solutions in slide 16 with base line text.

- Next meetings to finalize the other PSE/PD PI unbalance specifications for Type 3 and 4

Straw pole

- TBD

Thank You

Backup Slides

Table of content - 1

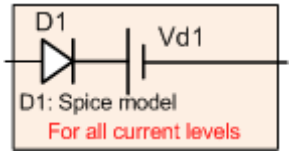
Table of content - 2

Annex A1: PD Model per ADHOC database slides

- See system model at backup slides per Annex F page 32 at: http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf

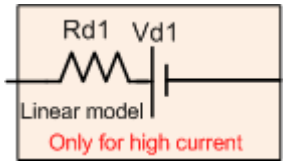
- Focusing on PD diode model…

  When PSPICE diode model D is used:

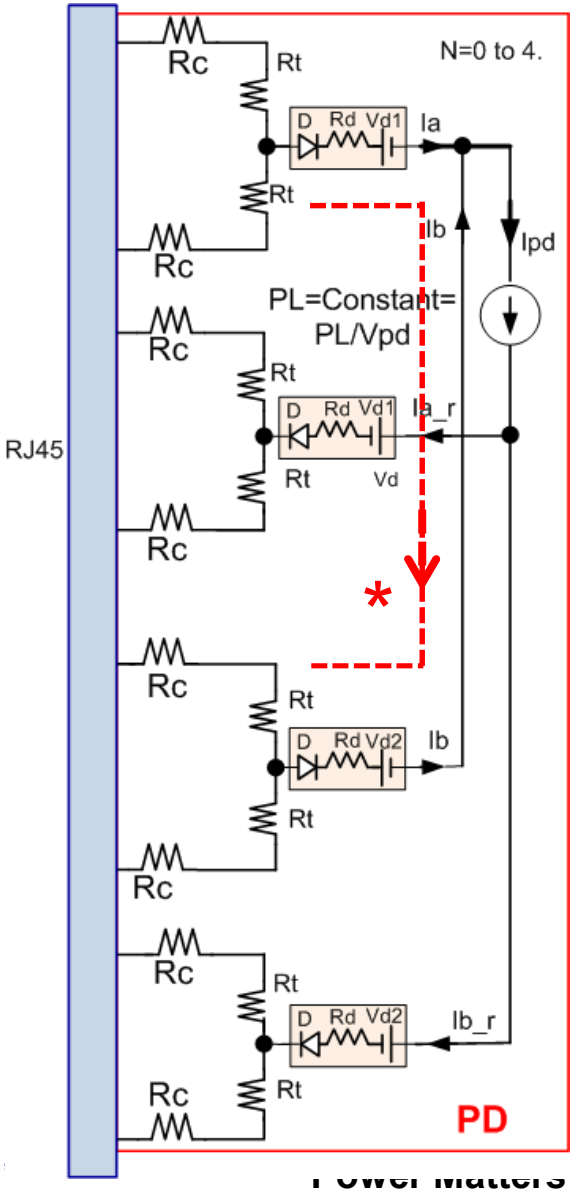


  - Set Rd=0.
    - Pspice diode model include Vf, Rd, Rp (losses) etc.
  - Vd1 and Vd2 are set to reflect Diodes Vdiff of the same diode part number.

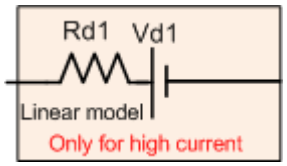
- When linear model (Vd, Rd) is used:



- D is shorted and diode model became Vd+Rd*Id
  - Good only for high currents.
  - At low currents it has errors due to internal loop currents that are created by PSE Vdiff and the absence of diodes that force the current to flow only in one direction. (* See drawing)
- See Annex F for complete system model details



Annex A2: MBR350/360 – Diode Linear Model



Tj	Vf1	If1	Vf2	If2	dVf	dIf
150	0.45	1	0.2	0.1	0.25	0.9
125	0.5	1	0.3	0.1	0.22	0.9
25	0.6	1	0.5	0.1	0.15	0.9

Vf=If*Rd+b	Rd=dVf/dIf	b=Vf1-Rd*If1
	0.277777778	0.172222222
	0.244444444	0.255555556
	0.166666667	0.433333333

- Vf increased when If increased as expected.
- Vf vs. Temp: Need to replace model parameters per temperature or include temperature coefficient in the model.
- Temperature balance between the 4 diodes in a bridge is required and can be achieved with suitable placement design.

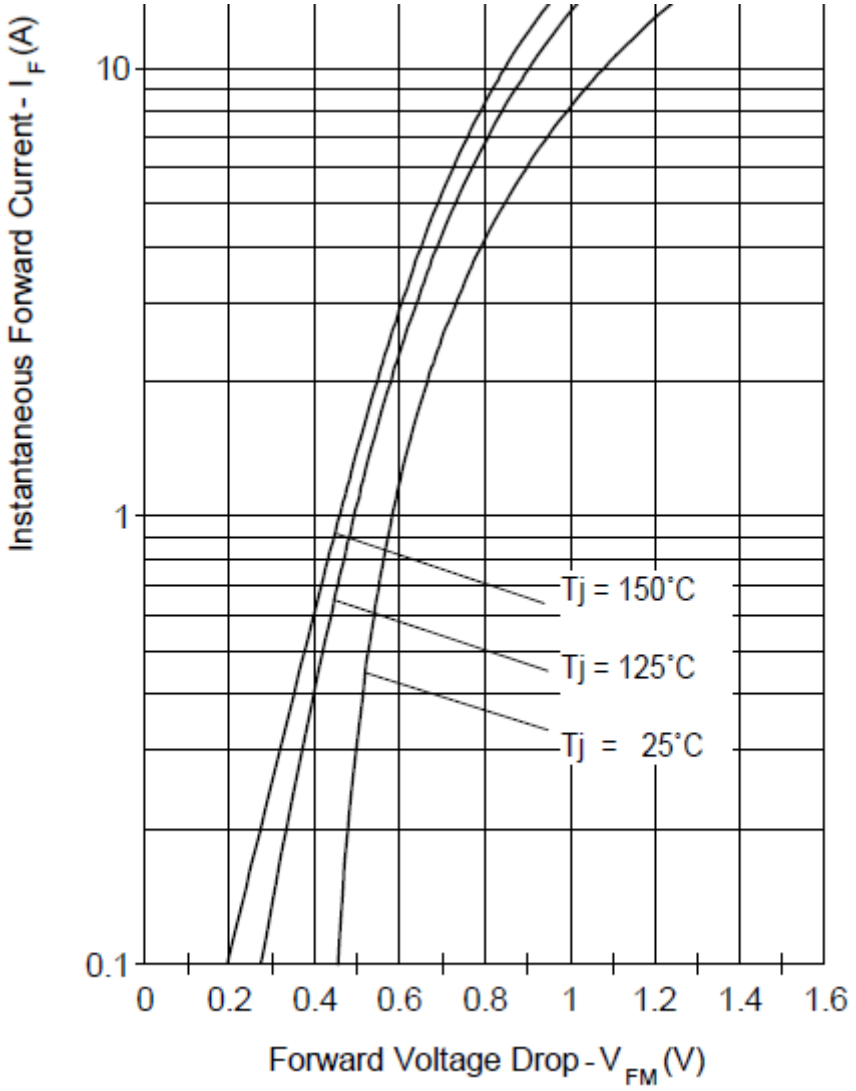
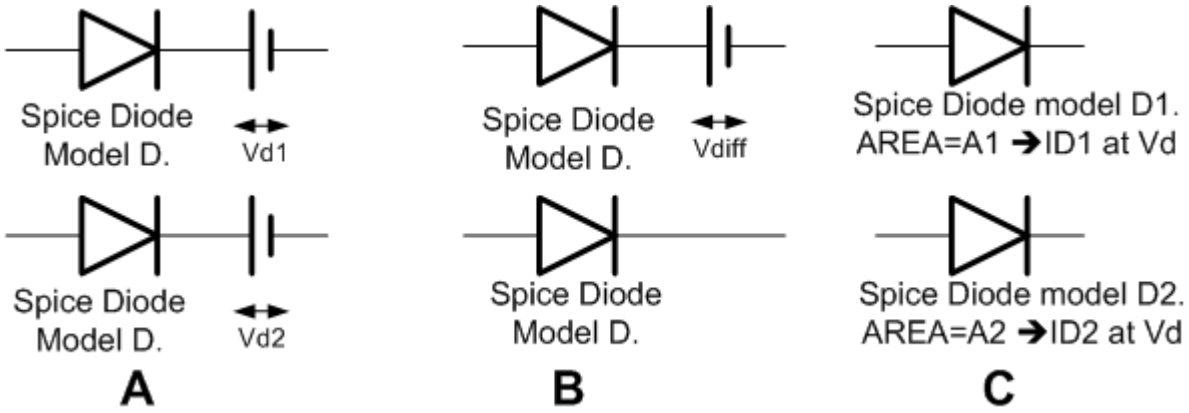


Fig. 1 - Max. Forward Voltage Drop Characteristics

Annex A3: Existing PD diode Model used in the system model per ADHOC database slides

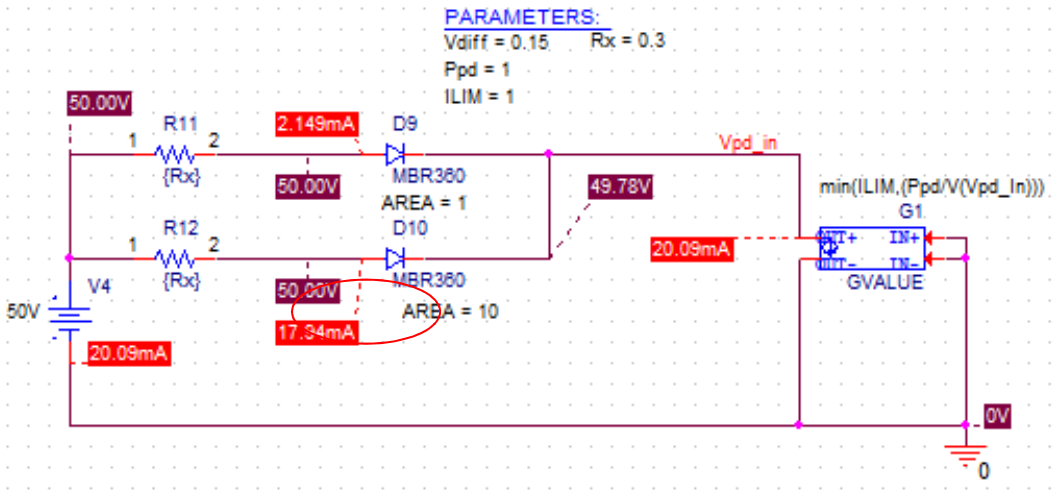
- The best currently used model for low and high current is A.
- B and C are equivalent to A.



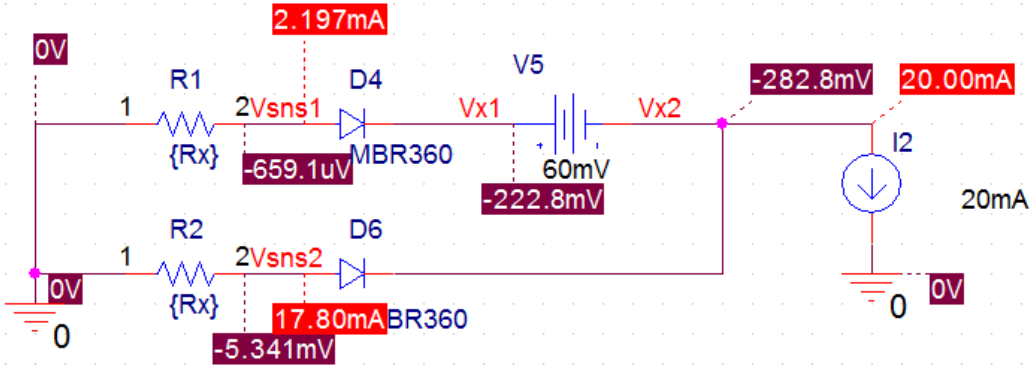
- See more details in Annex F. This is how P2P current unbalance results were obtained.

Annex A4: Equivalent Models for generating Vdiff

- **1st Model**
- Short Channel: Rx 0.3Ω from PSE PI to PD PI.
- Creating diode area ratio=10
- Creates ID(10)/ID(9)=α=~9 ratio.
  - ~2mA and 18mA over each pair
  - E2EP2PRUNB=(18-2)/(18+2)=80%
    - Or |(α-1)|/(α+1)=(9-1)/(9+1)=80%



- **2nd Model**
- Using current source instead of constant power sink which is OK for low current due to the fact that Vpse=~Vpd.
- Replacing two different diodes area with two identical diodes and 60mV voltage source to create the same behavior of 1st model above which is mathematically and physically are equivalents. See annex B for details.



Annex A5: Properties of Existing Diode Model per ADHOC database slides

- The proposed model: Spice diode model + Vd to create Vdiff behaves as expected:

#	Features
1	Vd is increased when current is increased.
2	Vdiff is effect on E2ECP2PRUNB when current is increased • At high currents, the linear model is accurate.
3	No errors at low current (mA range) When PSE Vdiff>0
4	Temperature unbalance effect can be simulated as well.
5	The model is automatically adjust itself to low or high current. • Rd is automatically adjusted (Dynamic resistance =dVf/dId) • Rp is automatically adjusted (Rp=(Ploss-Vf*Id)/Id^2, Vd=Vf+Id*Rp) • Vf and Vd are automatically adjusted as function of the current

Annex A6 – Different Spice diode models

- MBR360 from PSPICE library

.model MBR360 D(Is=403.6n Rs=36.68m Ikf=.6653 N=1 Xti=0 Eg=1.11 Cjo=502.8p
+ M=.5778 Vj=.75 Fc=.5 Isr=718.2n Nr=2)

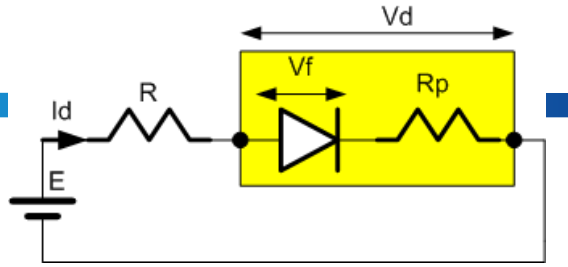
- Modifying MBR360 with STPS2H100A model numbers

.model MBR360 D(Is=3n Rs=30.287m Ikf=27.936E-3 N=1.0052 Xti=0 Eg=1.11 Cjo=502.8p
+ M=.5778 Vj=.55005 Fc=.5 Isr=1.4525n Nr=4.9769)

- STPS2H100A model contributed by Christian Beia / ST

.MODEL STPS2H100A D IS=3.0000E-9 N=1.0052 RS=30.287E-3 IKF=27.936E-3
+ EG=.69 XTI=2 CJO=264.50E-12 M=.49985 VJ=.55005 ISR=1.4525E-9
+ FC=0.5 NR=4.9769 TT=0

Annex B1: Mathematical analysis Part A: General Diode Equation.



- General Diode Equation:

$$Id = Is \cdot \left(\exp^{\frac{q \cdot Vf}{n \cdot k \cdot T}} - 1 \right) = Is \cdot \left(\exp^{\frac{q \cdot (Vd - Id \cdot Rp)}{n \cdot k \cdot T}} - 1 \right)$$

- Id is also equal to: $Id = \frac{E - Vd}{R}$
- Therefore Id is solved by:

$$\frac{E - Vd}{R} = Id = Is \cdot \left(\exp^{\frac{q \cdot (Vd - Id \cdot Rp)}{n \cdot k \cdot T}} - 1 \right)$$

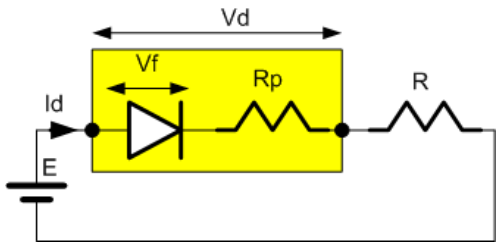
- There is no simple algebraic solution for it. There are iterative techniques or complex solutions by form of normalization and transformation to solve it.
- To simplify the solution and conclusions derivation, the analysis will be done with low R value (which will be used later to investigate short channel length i.e. lowest resistance between PSE and PD e.g. 0.3Ω to 1Ω range) and for:
  - Low load current
  - High load current.
- At high current and long channel we will get much lower system unbalance. See details in next slides.

- R=Load Resistance
- Vd=The voltage across the diode terminals
- Vf=Forward voltage . In general Vf=Vd-Id*Rp which will be addressed in the diode modeling discussion. Rp=parasitic resistance which is i*gnored at low current analysis.*
- Id=Diode current
- Is=Saturation dark (reverse) current. (Typical numbers: 10^-11A to 10^-12A for PN diode, 10^-6 to 10^-9 for Schottkey Diode).
- n= ideality factor, a number between 1 and 2 which typically increases as the current decreases.
- T=Temperature [°K]. Converting to Celsius: C=K-273.15.
- q=Electron Charge=1.602176*10^-19 Coulomb
- K=Boltzmann constant=1.380648*10^-23 J/T [°K]
- Is and n are not independent and they affect each other however presented here as independent variables for simplicity.

Annex B2: Mathematical analysis
Part B: Diode Equation at low current and short channel.

- At low current Id*(R+Rp)<<Vf, as a result R and Rp can be ignored and Vd=Vf.
- The general model can be simplified from:

$$\frac{E-Vd}{R}=Id=Is\cdot\left(\exp^{\frac{q\cdot(Vd-Id\cdot Rp)}{n\cdot k\cdot T}}-1\right)$$



- To: $Id=Is\cdot\left(\exp^{\frac{q\cdot Vd}{n\cdot k\cdot T}}-1\right)$

- As a result, Id is controlled by Vd which is =Vf only.
- Vf is the actual parameter that we are interested
  - E2ECP2PRUNB resistance and unbalance elements has negligible effect on E2ECP2PRUNB at low current and short channel.

Annex B3: Mathematical analysis
Part B: Diode Equation at low current and short channel.

At low current and short channel. **Id*(R+Rp)<<Vf.**

Finding Vf, Vd from Id equation.

$$Id = Is \cdot \left(\exp^{\frac{q \cdot Vf}{n \cdot k \cdot T}} - 1 \right) = Is \cdot \left(\exp^{\frac{q \cdot (Vd - Id \cdot Rp)}{n \cdot k \cdot T}} - 1 \right)$$

$$for \;\; Id \cdot Rp << Vd$$

$$Id = Is \cdot \left(\exp^{\frac{q \cdot Vd}{n \cdot k \cdot T}} - 1 \right)$$

$$1 + \frac{Id}{Is} = \exp^{\frac{q \cdot Vd}{n \cdot k \cdot T}}$$

$$LN\left(1 + \frac{Id}{Is}\right) = LN\left(\exp^{\frac{q \cdot Vd}{n \cdot k \cdot T}}\right) = \frac{q \cdot Vd}{n \cdot k \cdot T}$$

$$Vd = \frac{n \cdot k \cdot T}{q} \cdot LN\left(1 + \frac{Id}{Is}\right)$$

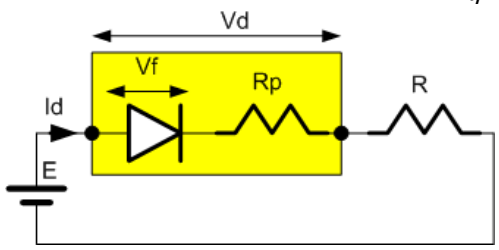
Diode Equations

Id/Is>>1 , therefore we can simplify to:

$$Vd \cong Vf = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Id}{Is}\right)$$

$$Id = Is \cdot \left(\exp^{\frac{q \cdot Vd}{n \cdot k \cdot T}} - 1 \right)$$

$$\frac{k \cdot T}{q} = 0.02585V \;\; @300°K$$



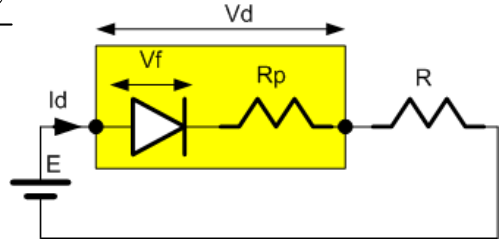
Annex B4: Mathematical analysis

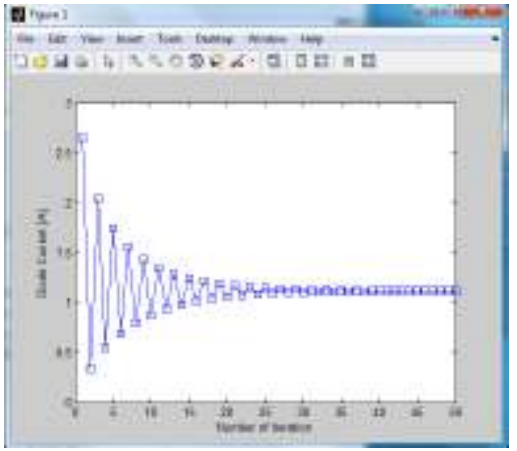
Part C: Diode Equation at high current **and short and long channel.**

- At high current vf=Vd - Rp*Id. (Rp+R)*Id can not be neglected.
- Id appears at both sides of the equation
- Can be solved with iterative solution.
- When Id increased. Vf is decreased causing Id to decreased until steady state solution is reached for Id.

$$Is \cdot \left(\exp^{\frac{q \cdot (Vd - Id \cdot Rp)}{n \cdot k \cdot T}} - 1 \right) = Id = \frac{E - Vd}{R}$$

$$Vd = \frac{n \cdot k \cdot T}{q} \cdot LN\left(1 + \frac{Id}{Is}\right) + Rp \cdot Id$$



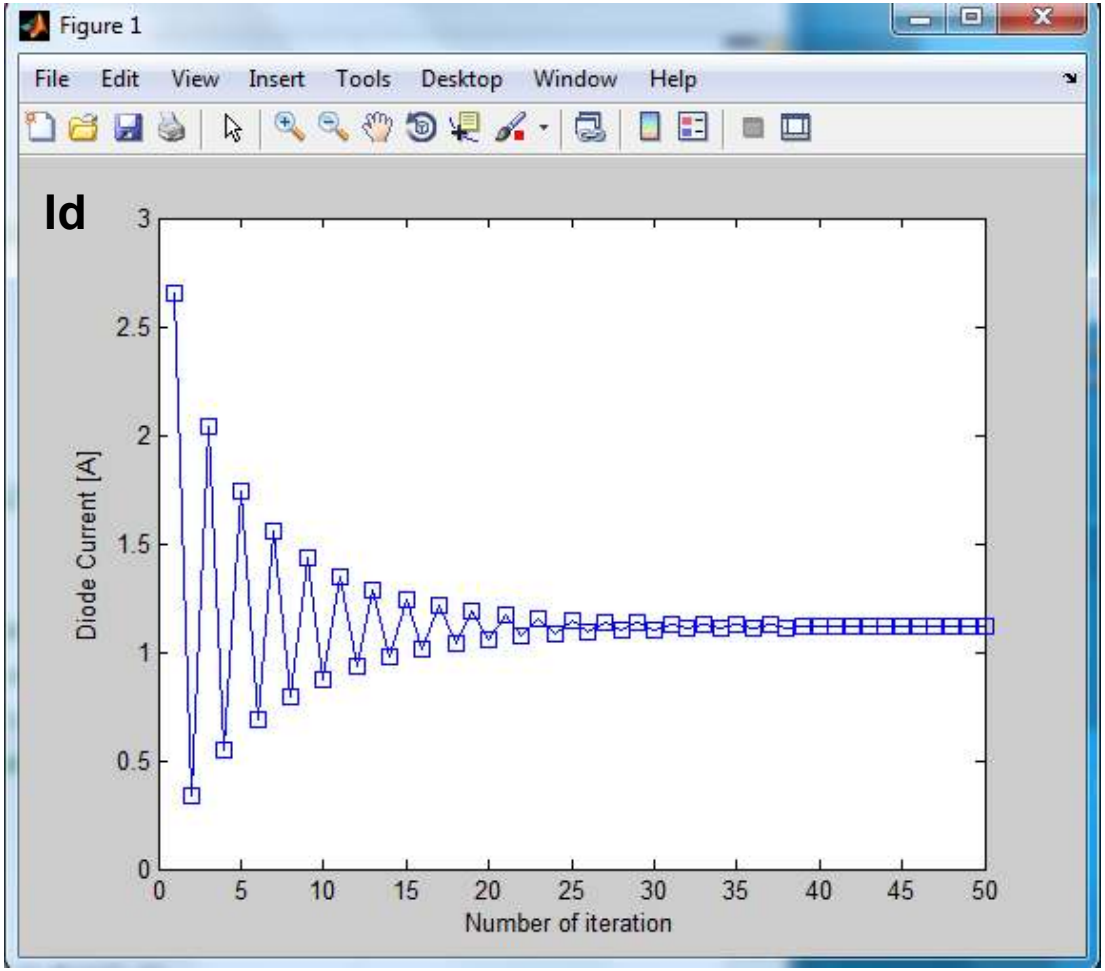


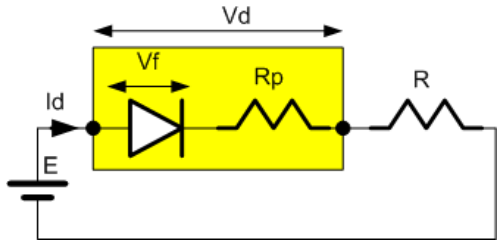
- **<u>As a result:</u>**
- Voltage drop Vd on the diode is increased when current increase ➔ Vf is decreased
- Rp is helping balancing the current Id. It means if current is splitted between two diodes the Vf difference between them and as a result the Idiff between them will decreased compared to lower current.
  - **At high current system unbalance is better than at low current.**
    - **We can see this effect in next slides with more details.**

Annex B5: Mathematical analysis

Part C: Diode Equation at high current and short channel.

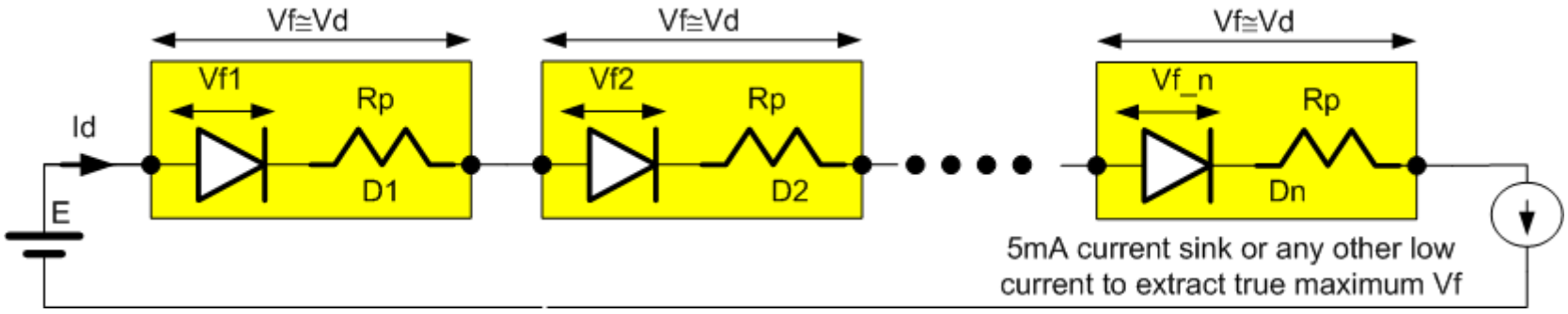
- Iterative diode equation solution for Id: $\frac{E - Vf}{R} = Id = Is \cdot \left(\exp^{\frac{q \cdot (Vd - Id \cdot Rp)}{n \cdot k \cdot T}} - 1 \right)$





Annex B6: Mathematical analysis
Part D: Characterization of diode Vf and Vdiff at low current.

- We need to find the **true Vf** generated by the diode silicon parameters without the effect of Rp*Id. The **true Vf** is the **Vf_max at the tested Id** operating point.
- The way to do it is to test Vf at low current (few mA range).
- All diodes driven with the same current to eliminate Vf differences due to current variations between diodes.
- We can't connect diodes in parallel for calculating Vdiff due to the fact that the diode with lower Vf will shunt the diode with the higher Vf. We will see later that when diodes are connected in parallel, the current distribution between them will be a direct function of the **true Vf differences.**



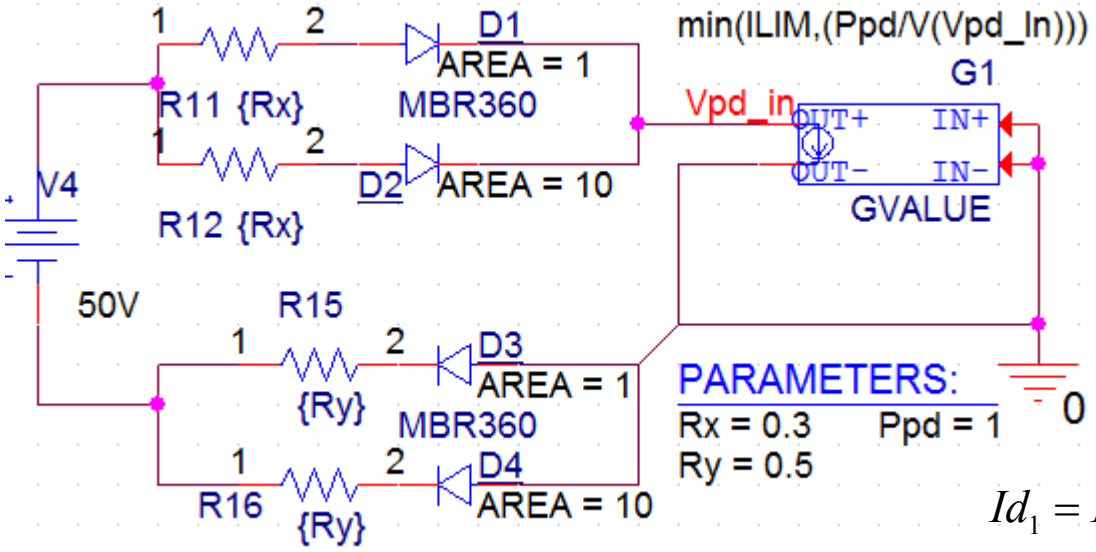
- $Vdiff=Vd_n-Vd_m$, for any $m \neq n$. We are interested in Vdiff_max.

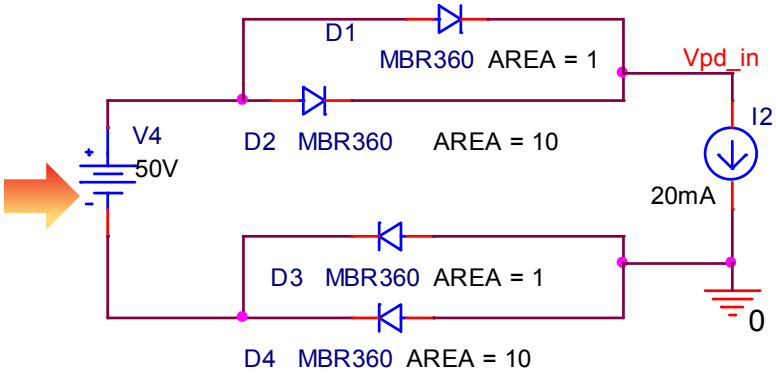
Annex B7: Mathematical analysis
Part D: Characterization of Vdiff at low current.

- **Finding Voltage difference between two diodes on pairs with the same voltage polarity**
  - Diode voltage can vary due to process variations determined by n, Is and Temperature.
    - The junction temperature of all diodes is assume to be the same at low current due to the fact that diode power loss is negligible at **low current** resulting with Tj≅Ta.
    - Is can vary significantly since it is process dependent and proportional to diode cross conduction area. Is also highly dependent on temperature.
    - n can vary between 1 (typical) to 2 (at low Vf and low current) and is dependent on Is.
    - Id/Is>>1
    - Id1=Id2=Id as per the characterization test shown in previous slides. **Note: Don't confuse between the fact that in our 4P PoE system, Id1 and Id2 will not be the same. They are not the same due to the fact that the true Vf at low current of D1 and D2 are not the same. In our 4P system when D1 and D2 are appear to be in parallel when (R+Rp)*Id<<Vf, it is the "shunt" effect that force the same voltage on both diodes in a pair of the same polarity that cause the current unbalance i.e. the diode with the lowest Vf will have the highest current and its Vf will be forced on the 2nd diode with higher Vf resulting with lower current through the 2nd diode due to the fact that that diode needs higher Vf to produce the same current that the diode with the lower Vf.**
      - **See next electrical drawing that explains the two diodes in parallel case.**

Annex B8: Mathematical analysis
Part D: Characterization of Vdiff at low current.

- Current will be higher through the diode with lower voltage across it and vice versa.
- At low current and short channel the same voltage Vd ,is forced on the diodes. Also Vd=Vf.
- Voltage drop on the end to end channel pair resistance is very small.
  - I(Rx)*Rx<<Vf. (E.g: 10mA*(Rx=0.5Ω)=5mV. Vf=0.2V to 0.7V.)
- At low current PD diode Vdiff affects DC disconnect pair current.
- Vpse=~Vpd ➔ No need to use constant power sink ➔ Current sink/source can be used.
- As a result, Vf1=~Vf2=Vf_min *(If Rch➔ 0 then Vd1=Vd2)*
- If Is2/Is1=10 ➔ Id2 > Id1 resulting with P2P_Iunb=(Id2-Id1/(Id2+Id1)
- Same procedure apply to the negative pairs where current is measured.
- PD diode Vdiff value before inserted to the circuit below, affects system P2P current

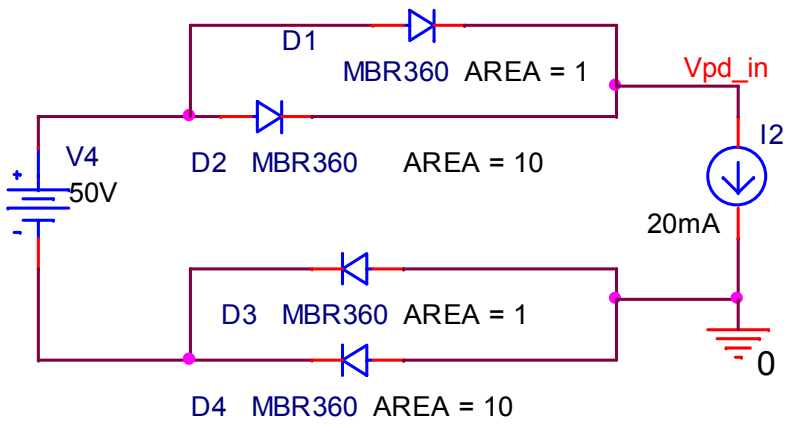




$$Id_1 = Is_1 \cdot \left(\exp^{\frac{q \cdot Vf_1}{n_1 \cdot k \cdot T}} - 1 \right), \quad Id_2 = Is_2 \cdot \left(\exp^{\frac{q \cdot Vf_2}{n2 \cdot k \cdot T}} - 1 \right)$$

Annex B9: Mathematical analysis
Part D: Characterization of Vdiff at low current.

- The simplified zero channel length at low current will look like the following drawing (example shown on positive pairs):
  - Id1*Rch<<Vf1, Id2*Rch<<Vf2
  - Vf2 is lower than Vf1 (See example in Slide 9: Diode Characterization Curve)
  - Vf2 is forced on Vf1 so Vf1=~Vf2=Vf_min
  - As a result: D2 will have maximum pair current af Vf2.
  - D1 will have minimum current at Vf2 while it needs Vf1>Vf2 to allow same current.
  - If Rch is increased, Vf1≠Vf2 and reach Vdiff_max initial value.



$$Id_1 = Is_1 \cdot \left(\exp^{\frac{q \cdot Vf}{n_1 \cdot k \cdot T}} - 1 \right)$$

$$Id_2 = Is_2 \cdot \left(\exp^{\frac{q \cdot Vf}{n2 \cdot k \cdot T}} - 1 \right)$$

$$Id_1 + Id_2 = I2$$

Annex B10: Mathematical analysis
Part D: Characterization of Vdiff at low current.

$$Vd_1 = \frac{n_1 \cdot k \cdot T_1}{q} \cdot LN\left(\frac{Id_1}{Is_1}\right) + Id_1 \cdot Rp_1$$

$$Vd_2 = \frac{n_2 \cdot k \cdot T_2}{q} \cdot LN\left(\frac{Id_2}{Is_2}\right) + Id_2 \cdot Rp_2$$

$$Vdiff = Vd_1 - Vd_2 = \frac{n_1 \cdot k \cdot T_1}{q} \cdot LN\left(\frac{Id_1}{Is_1}\right) - \frac{n_2 \cdot k \cdot T_2}{q} \cdot LN\left(\frac{Id_2}{Is_2}\right) + Id_1 \cdot Rp_1 - Id_2 \cdot Rp_2$$

- For: Id1=Id2=Id (to find **true maximum Vf** at low current as explained previously).
- Id1*Rp1<<Vf1, Id2*Rp<<Vf2
- T1=T2 (at low current Tj≅Ta)
- N1=n2=n at the same Id current and at low current is a very high probability assumption i.e. negligible probability that two diodes of the same part number and manufacture will have n=1 and n=2. Most of the will be with similar n value in the range of 1 to 2.

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right)$$

Annex B11: Mathematical analysis
Part D: Characterization of Vdiff at low current.

- Typical diodes will be with n1=n2≅1, Is2/Is1=10 (assumed process accuracy) at T=300°K (~27 °C) we will get:

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 59.5mV$$

- Vdiff_max is found by using n=2 and Is2/Is1=10 at the same time.

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 119mV$$

- Or Significant number of parts will have Is2/Is1=100 with n≅1:

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 119mV$$

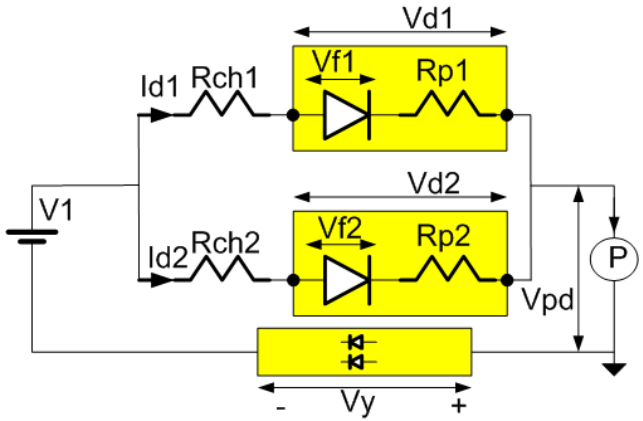
- Conclusion: Realistic calculated worst case Vdiff of currently used diodes is 119mV ➔ 120mV.

Annex B12: Mathematical analysis
Part E: Vdiff effect on P2P_Iunb at high current.

- **The general case with high current and any channel length.**
- E=V1-Vpd-Vy. It will simplify showing the behavior of e.g. positive pairs
- Vdiff at high current: Voltage drop on Rp and R is not <<Vf1.
  - Actually Vf1=Vd1-Id1*Rp1, Vf2=Vd2-Id2*Rp2 and Id1*Rch1 and Id2*Rch2 help to reduce the differences between Id1 and Id2 by acting as ballast resistors.
- In this case the current Id1 and Id2 can be find by solving the following two complex equations:

$$\frac{E - Vd_1}{R_{ch1}} = Id_1 = Is_1 \cdot \left(\exp^{\frac{q \cdot (Vd_1 - Id_1 \cdot Rp_1)}{n \cdot k \cdot T}} - 1 \right)$$

$$\frac{E - Vd_2}{R_{ch2}} = Id_2 = Is_2 \cdot \left(\exp^{\frac{q \cdot (Vd_2 - Id_2 \cdot Rp_2)}{n \cdot k \cdot T}} - 1 \right)$$



Example for positive pairs. Same applies for negative pairs.

- The above can easily found by using simulations.
- **The accurate visibility and understanding why diode Vdiff is reduced when current is increased can be seen by normalizing the above system to simpler version of it i.e. Just a voltage source E connected to two pairs as shown in next slides.**

Annex B13: Mathematical analysis
Part E: Vdiff effect on P2P_Iunb at high current.

-The following drawing describes the **steady state** condition of the positive pairs. Similar analysis can be done for the negative pairs.
-Vf1 and Vf2 are the steady state final (Iteration end value) value of diodes silicon portion of D1 and D2 (Vf=Vd-Rp*Id).
-R1 and R2 represents all resistive elements on the pair from end to end including PSE and PD and diodes resistive loses. E.g. R1=Rch1+Rp1.

1. $IL = \frac{Vx}{RL}$

2. $Id_1 = \frac{E - Vx - Vf_1}{R_1}$

3. $Id_2 = \frac{E - Vx - Vf_2}{R_2}$

4. $IL = Id_1 + Id_2$

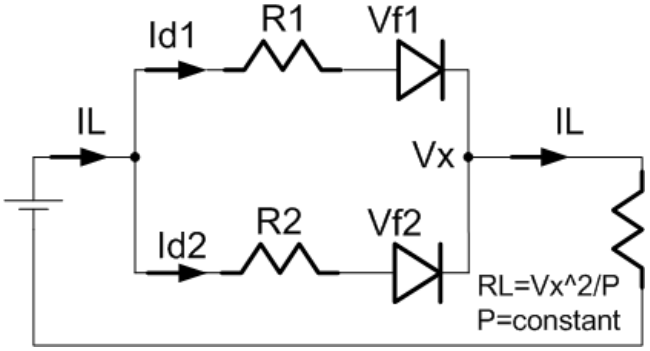
Solving $1+2+3+4$ *for* Vx:

5. $$Vx = \frac{E \cdot \left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{Vf_1}{R_1} - \frac{Vf_2}{R_2}}{\frac{1}{RL} + \frac{1}{R_1} + \frac{1}{R_2}}$$

From (5) $Id1$ *and* $Id2$ *can be found.*

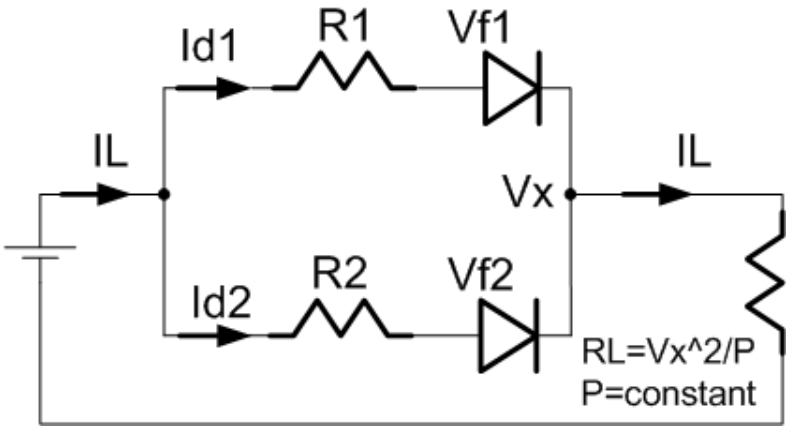
From (2) *and* (3) $P2P\_Iunb$ *can be found*:

6. $$Iunb = \frac{Id2 - Id1}{Id2 + Id1} = \frac{\left(\frac{E - Vx - Vf_2}{R_2}\right) - \left(\frac{E - Vx - Vf_1}{R_1}\right)}{\left(\frac{E - Vx - Vf_2}{R_2}\right) + \left(\frac{E - Vx - Vf_1}{R_1}\right)}$$



Annex B14: Mathematical analysis
Part E: Vdiff effect on P2P_Iunb at high current.

$$6.\ Iunb = \frac{Id2 - Id1}{Id2 + Id1} = \frac{\left(\frac{E - Vx - Vf_2}{R_2}\right) - \left(\frac{E - Vx - Vf_1}{R_1}\right)}{\left(\frac{E - Vx - Vf_2}{R_2}\right) + \left(\frac{E - Vx - Vf_1}{R_1}\right)}$$



- In order to show why Diode Vdiff weight is reduced when current and value of resistive elements in the pair are increased, R1=R2 will be set to eliminate the effect of resistive elements unbalance and show how Vdiff is affected:

$$R1 = R2 = Rch + Rp = R$$

$$V_{R2} = E - Vx - Vf_2$$

$$V_{R1} = E - Vx - Vf_1$$

$$Iunb = \frac{Id2 - Id1}{Id2 + Id1} = \frac{|Vdiff|}{V_{R1} + V_{R2}}$$

$$For\ V_{R1} > 0\ \ and\ \ V_{R2} > 0$$

- **Conclusion: P2P_Iunb is reduced for any Vdiff by a factor of 1/(VR1+VR2).**
- For low current, Id*(Rc+Rp)<<Vf, Vf1=Vf2=Vf_min is forced on the diodes so different equation is used for calculating Id1, Id2 and P2P_Iunb. See previous slides for information.

Annex B15: Mathematical analysis
Part F: Vdiff vs. Temperature.

- **The sensitivity of diode Vdiff to a temperature differences between the two diodes.**
  - Diodes have temperature difference of 5°K at the high current case.
  - n1=n2=1. Is2/Is1=10. Id1=Id2=600mA, T1=305°K, T2=300°K
  - T1>T2 for getting worst case results. T2>T1 will result with lower Vdiff.
  - Id1 and Id2 is a steady state solution for two diodes with the same current through it. (This is the way to compare Vf between diodes without other effects such resistors unbalance and resistor elements balancing effects).

$$Vdiff = Vd_1 - Vd_2 = \frac{n_1 \cdot k \cdot T1}{q} \cdot LN\left(\frac{Id_1}{Is_1}\right) - \frac{n_2 \cdot k \cdot T_2}{q} \cdot LN\left(\frac{Id_2}{Is_2}\right) =$$

$$Vdiff = Vd_1 - Vd_2 = 1 \cdot 0.02628 \cdot LN\left(\frac{0.6A}{40nA}\right) - 1 \cdot 0.02585 \cdot \cdot LN\left(\frac{0.6A}{400nA}\right) = 66.7mV$$

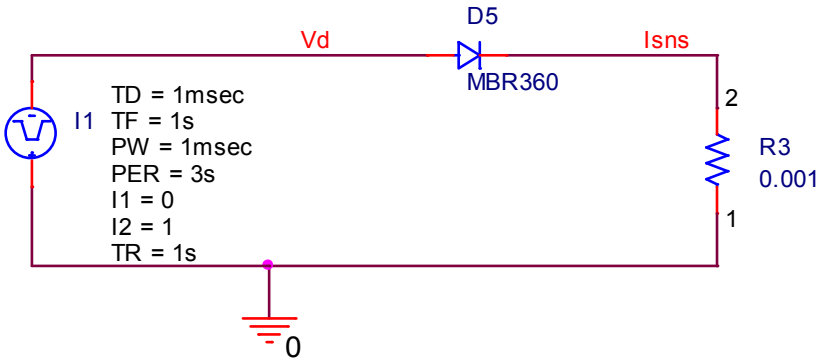
- Compared to a case where T1=T2.

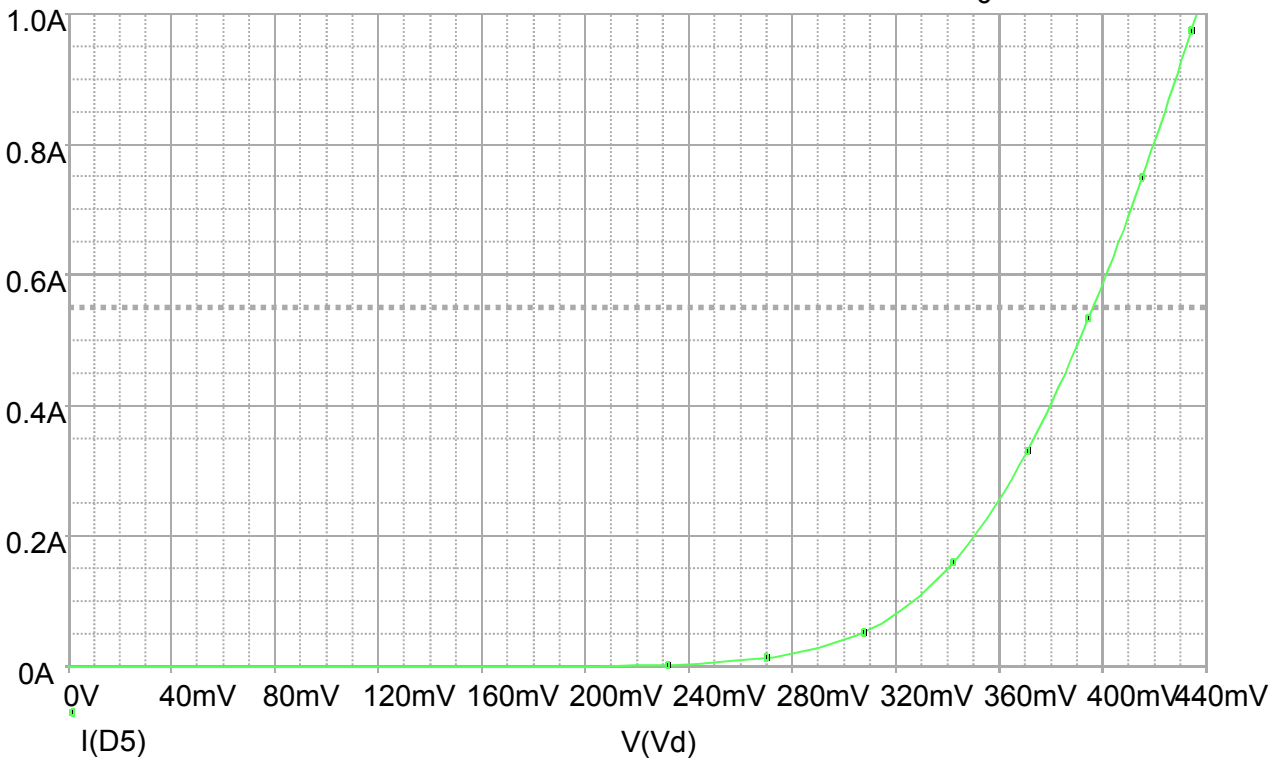
$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right) = 59.5mV$$

- 7.2mV higher for 5°K temperature difference between the diodes

Annex D1: Simulation results.
PD Diode I/V curve used in the following simulations.

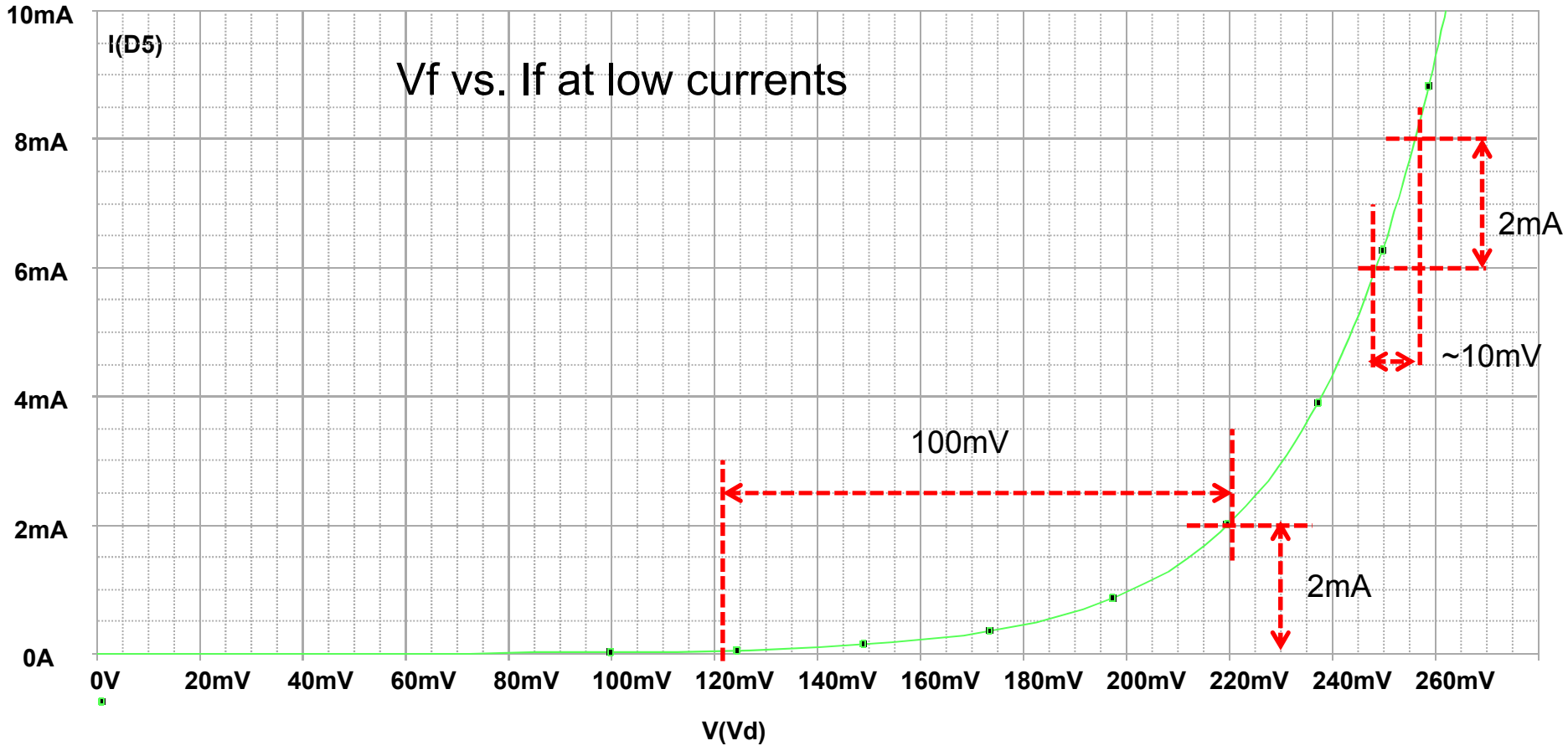
- Running at 1A.





Annex D2: Simulation results.
PD Diode I/V curve used in the following simulations.

- **Behavior at low current range.**
- Diode Rd=d(Vf)/d(Id) is decreased when If is increased.
- D1 to D2 Vdiff is ~constant as function of If as shown in mathematical analysis and lab tests

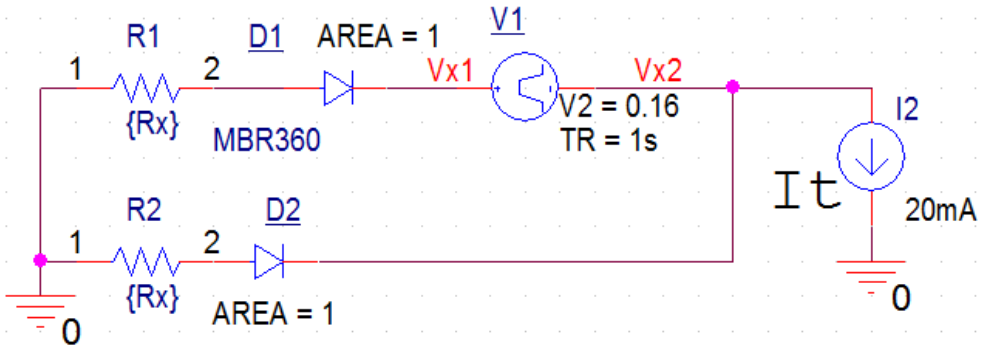


Annex D3: Simulation results of only the PD diodes effect on the system current unbalance.

- Checking End to End Channel Pair to Pair Channel Current Unbalance (E2ECP2PCUNB) PD diodes effect
- Checking **only** the PD diode effect on the system current unbalance.
  - Setting Rmax=Rmin=Rx for all elements.
  - Rx is the end to end resistance of the positive pair including PSE and PD PI elements.
  - Ry is the end to end resistance of the positive pair including PSE and PD PI elements.
- Analyzing unbalance at short channel to extract worst case unbalance effect at low and high current.
- Analyzing results at positive pairs and negative pairs were current is measured.
  - The effect on DC disconnect thresholds (Negative pairs where current is measured)
  - The effect on pair maximum current (positive pairs for worst case unbalance).
    - Worst case unbalance is the place where we have minimum end to end resistance
    - Negative pairs has better unbalance due to the contribution of RDSon and Rsense
    - If Rsense and RDSOn is out of the two pairs current path, the P2P_Iunb will be higher and equal to the positive pair unbalance
- Rx represents all components of PSE PI, PD PI and Cables and Connectors.
  - Rx=2*(Rconn+Rt+Rcable)/2=0.04Ω+0.125Ω+0.135Ω= **0.3Ω**
  - Ry=2*(Rconn+Rt+Rcable)/2+Rsense+Rdson=0.04Ω+0.125Ω+0.135Ω+0.1+0.1= **0.5Ω**

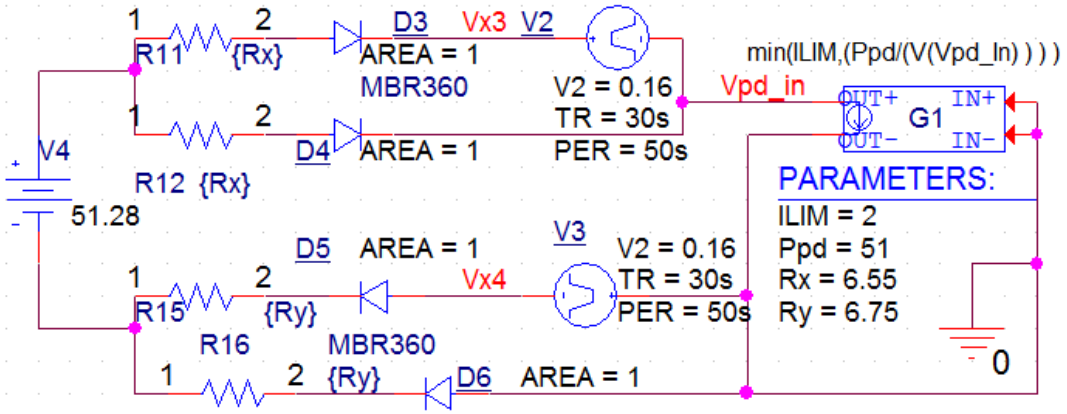
Annex D4: Simulation results of only the PD diodes effect on the system current unbalance.

- **Simulation model for low currents only.**
- Constant power sink can be replaced with current source.
- Positive pair shown for example. At low currents, positive pairs and negative pairs at short channels will results with the same behavior.



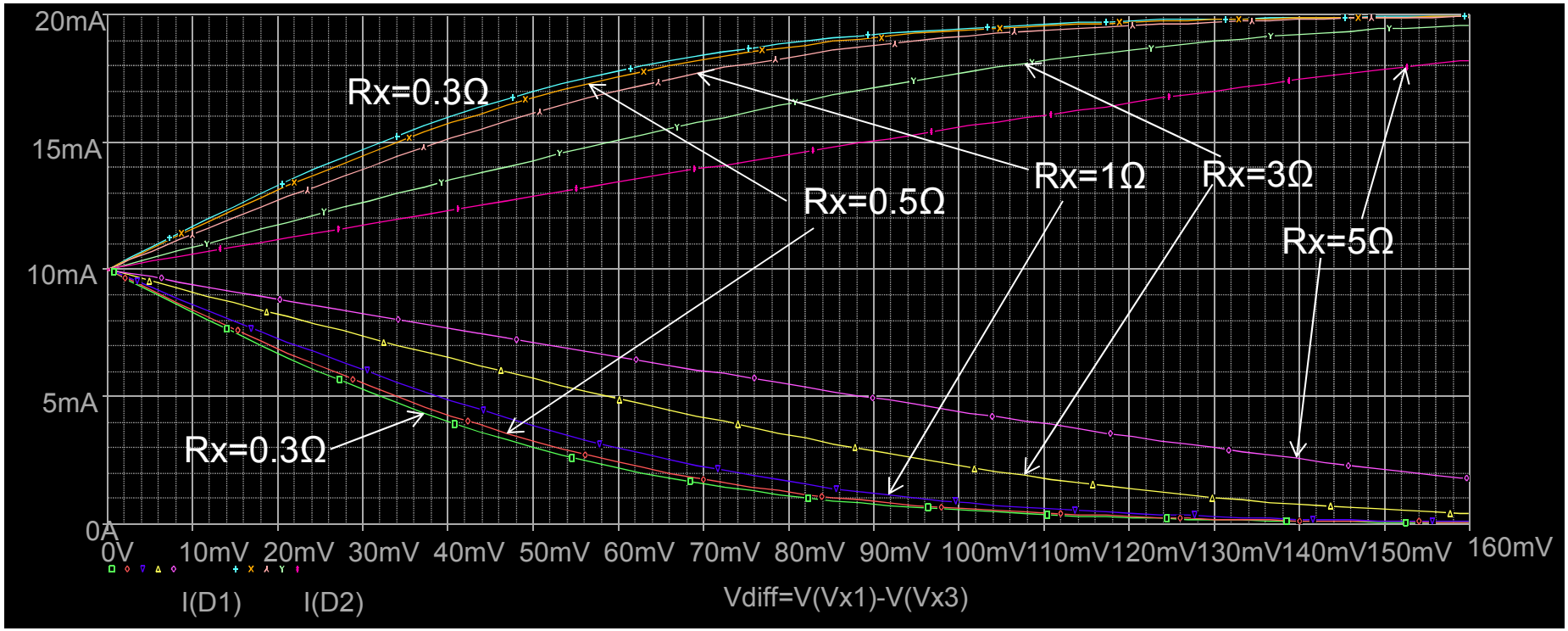
Model #1

- **Simulation model for high currents and low currents**



Model #2

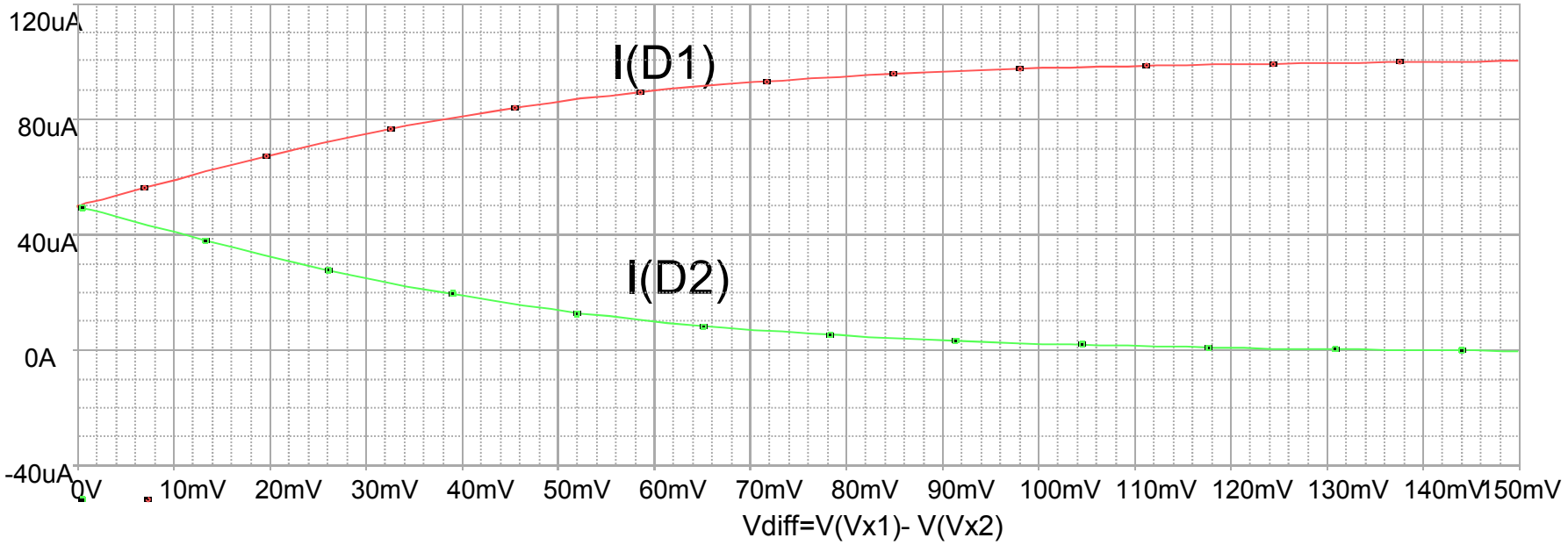
Annex D5: Simulation results of the PD diodes effect only on the system current unbalance.



- Model #1 setup.
- Id1 and Id2 vs. Vdiff and Rch. Rch=Rx=0.3,0.5,1,3 and 6Ω
- Total load current=20mA.
- Lab results confirms ID1_min=1.25mA and Ia_max=8.75mA at 10mA load, p2p_Iunb=75% as worst case minimum (very big samples) at very short channels (very low channel resistance, Rx=0.3Ω on positive pairs and 0.6Ω).

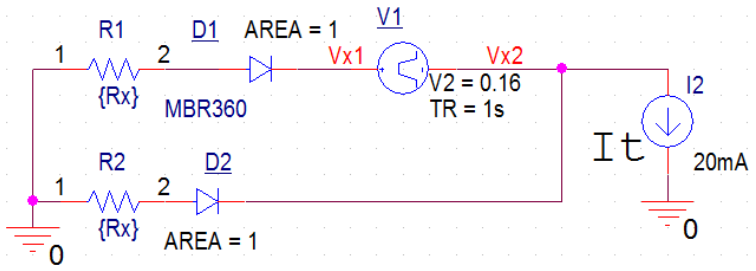
Annex D6: P2P current distribution at **low** current due to PD diodes Vdiff. Simulation results.

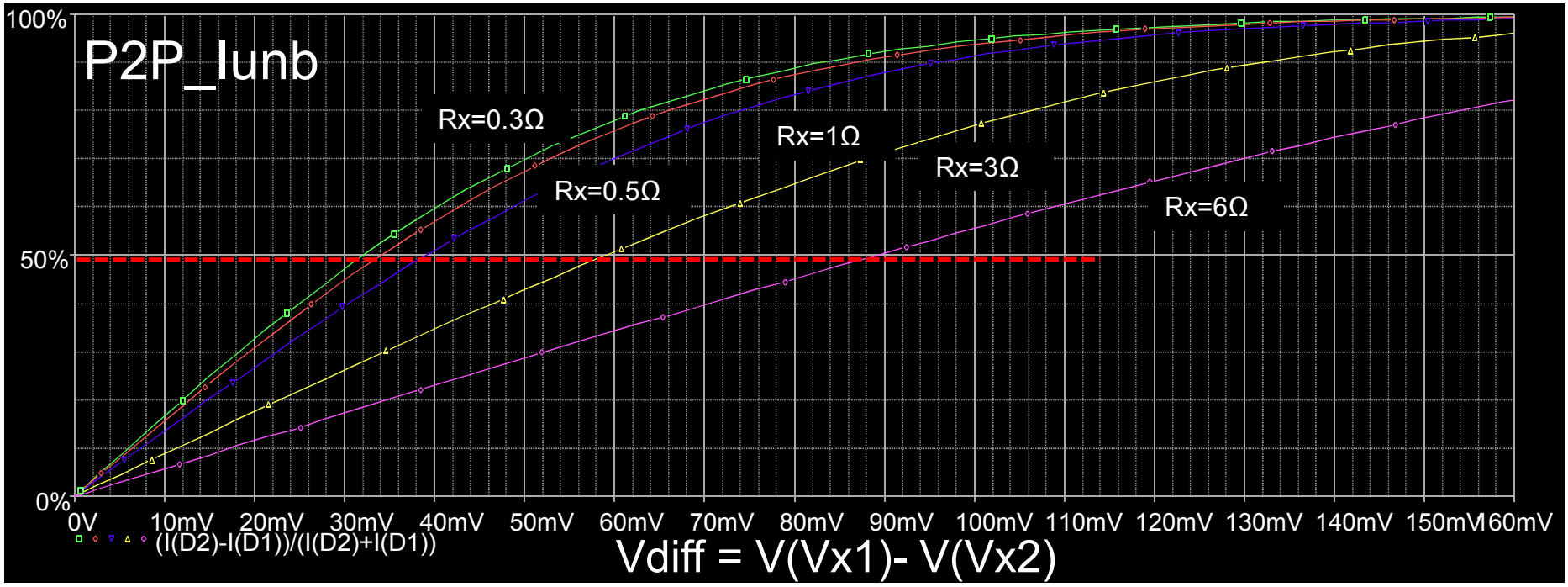
- Load current 100uA. Model #1 setup.
- Short Channel.
- Positive pairs are shown at Rx=0.3Ω.
- Negative pairs will have the same results at Rx=0.5Ω
- Current distribution at very low load as function of PD diode Vdiff.
  - Pair current will be ~ZERO at Vdiff ≥100mV and ~10uA at Vdiff=60mV.
  - Confirmed by lab results.



Annex D7: Simulation results of only PD diodes effect at low current on the system P2P_Iun.

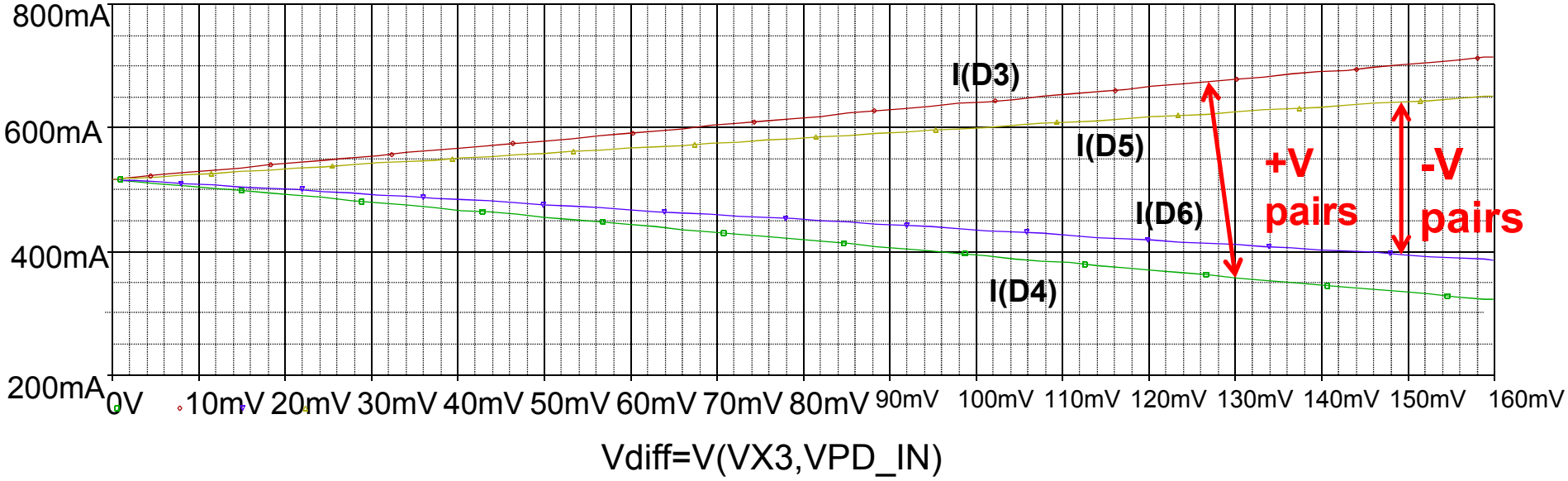
- Pair to pair system unbalance at low load current=20mA. Model #1 setup.
- Behavior of positive pair and negative pair is almost the same at low current.
- See Rx=0.3Ω and Rx=0.6Ω.showing this fact.
- Similar results at 10mA load.
- Results for Rx=0.3, 0.5, 1, 3 and 6Ω





Annex D8: P2P current distribution at **High** current due to PD diodes Vdiff effect only. Simulation results.

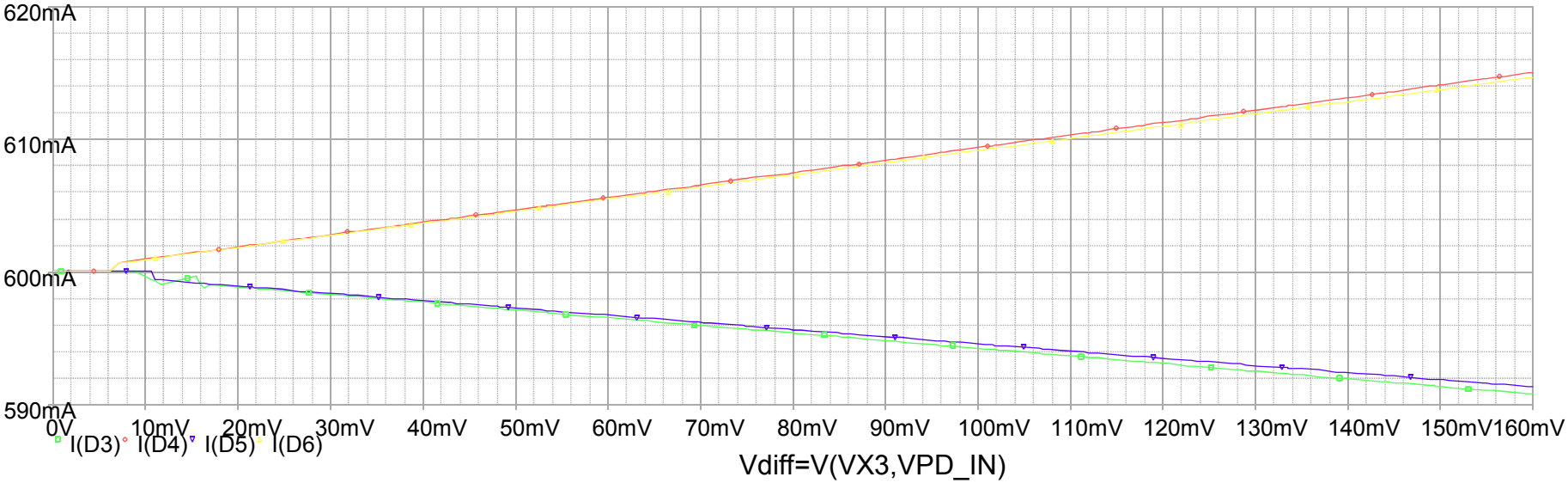
- Iload=1.035A (Ppd≅51W). Rx=0.3Ω. Model #2 setup.
  - In full system model including components unbalance, we will get ~5% higher current. In this simulation, the objective was to find only the diode effect on P2P_Iunb by setting the other components P2P_Iunb to ZERO.



- P2P_Iunb is improved when load current is increased due to the voltage drop across Rx. (Rx>Rp. Rp<0.1Ω).
- Good P2P_Iunb even with PD diode Vdiff=160mV with SHORT channel.
  - Mathematically confirmed. Confirmed by lab results.

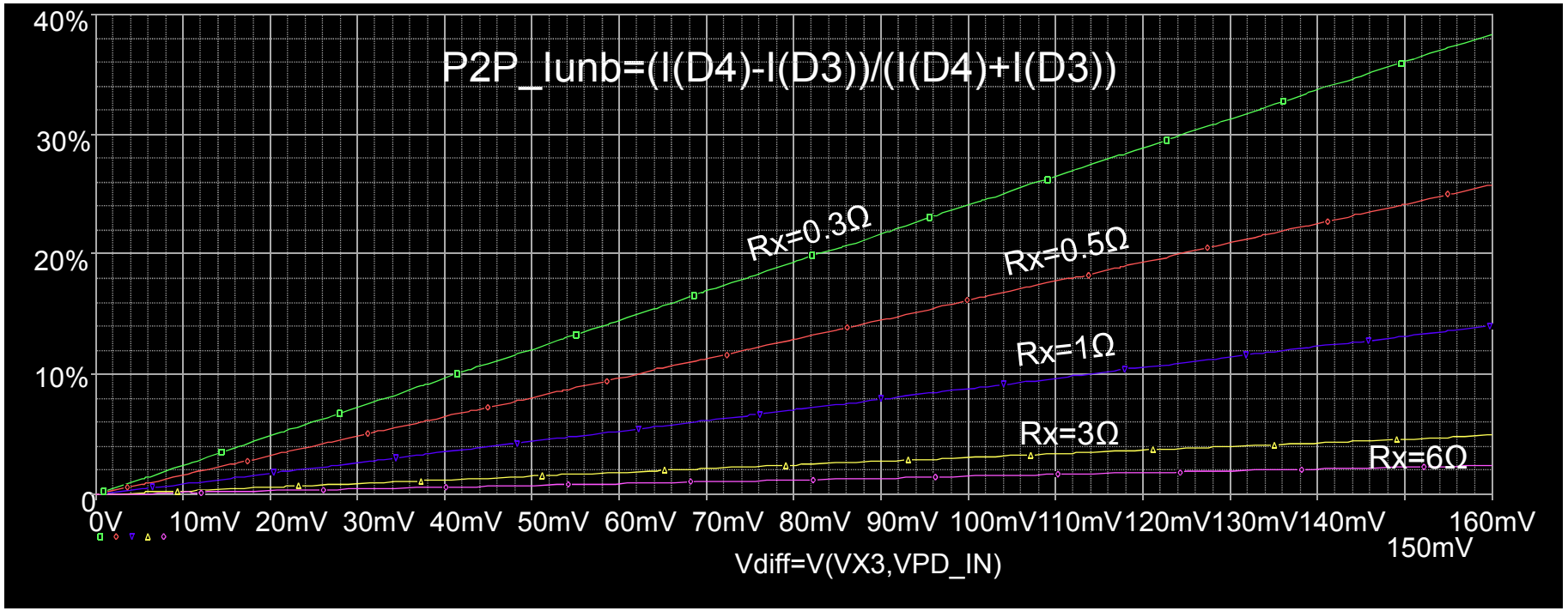
Annex D9: P2P current distribution at **High** current due to PD diodes Vdiff effect only. Simulation results.

- Iload=1.2A (Ppd≅51W). Model #2 setup.
- Rx=6.25Ω +0.3Ω=6.55Ω.
- Ry=6.25Ω +0.5Ω=6.75Ω.



- Very good P2P_Iunb even with PD diode Vdiff=160mV with **long channel.**
  - Mathematically confirmed
  - Lab results confirmed.

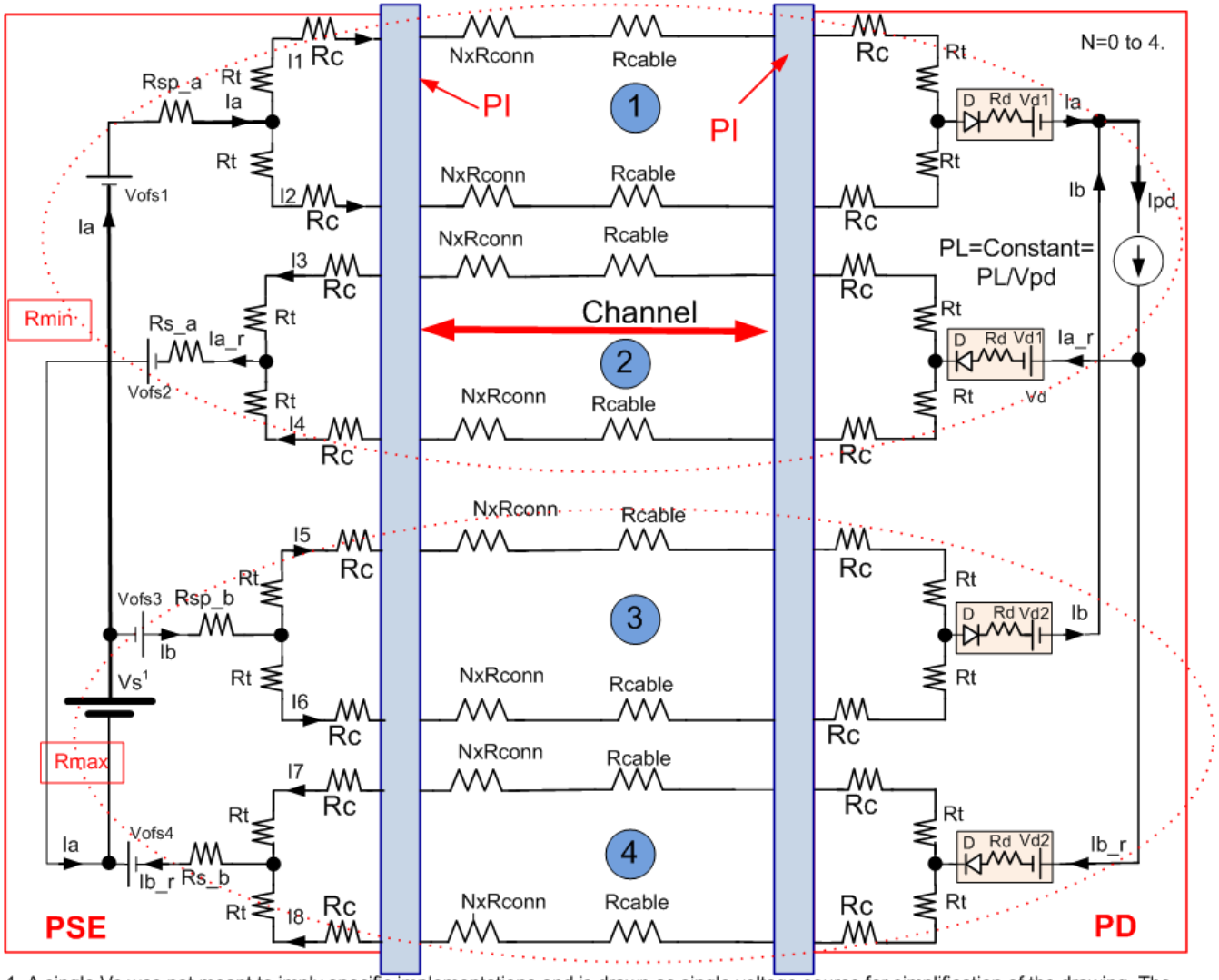
Annex D10: P2P current distribution at **High** current due to PD diodes Vdiff effect only. Simulation results.



- Model #2 setup.
- P2P_Iunb as function of PD Vdiff and different Rch=Rx values.
- Rx=End to End **pair** resistance.

Annex F – Model updates to be review by adhoc.

Adhoc to review and approve updates in summarized in the red text. Adhoc response: OK, No comments, good enough to our needs. August 2014.



1. A single Vs was not meant to imply specific implementations and is drawn as single voltage source for simplification of the drawing. The important parameter is the pair to pair voltage difference.

- Notes for the general Model:

1. Total end to end channel connectors is 6 max.
2. The formal channel definition is marked in red arrow and is with up to 4 connectors.
3. Number of connectors can varies between 0 to 4 as function of channel use cases A,B,C and D per annex G1
4. The internal application component resistance are addressed as well.
5. In simulations, pairs 1 and 2 components were set to minimum resistance and pairs 3 and 4 were set to maximum resistance values.
6. Vofs1/2/3 and 4 was added. Per adhoc consensus.
7. When Spice model Diode is used (instead of linear model) for investigating behavior at low and high currents, set Rd=0.

Annex G1: Existing adhoc worst case data base

#	Parameter	Data set 1	Data set 2
1	Cordage resistivity[1]	0.14Ω/m	
		0.09262Ω/m for AWG#24 for worst case analysis	
2	Horizontal cable resistivity option 1[2]	11.7Ω/100m=(12.5Ω - 4*0.2Ω) / 100m which is the maximum resistance when tested with maximum Iport.	7.4Ω/100m (CAT6A, AWG23) This is to give us maximum P2PRunb
3	option 2[3]	0.098Ω/m. Maximum value per TIA etc. Can't be used for worst case analysis.	
4	Unbalance parameters	• Cable Pair resistance unbalance: 2%. Channel pair resistance unbalance: 3% • Cable P2P Resistance Unbalance: 5%. • Channel P2P Resistance Unbalance: 0.1Ω/7.5% max which ever is greater	
5	Channel use cases to check. See figure 1 for what is a channel.	A. 6 inch (0.15 m) of cordage, no connectors. B. 4 m channel with 1 m of cordage, 3 m of cable, 2 connectors C. 23 m channel with 8 m of cordage, 15 m of cable, 4 connectors D. 100m channel with 10 m of cordage, 90 m of cable, 4 connectors	
6	End to End Channel[6]	The Channel per figure 1 + the PSE and PD PIs.	
7	Transformer winding resistance	120mOhm min, 130mOhm max	
8	Connector resistance[8]	40mOhm min, 60mOhm max	30mOhm min, 50mOhm max
9	Diode bridge[9] (Discreet Diodes)	0.39V+0.25Ω*Id min; 0.53V+0.25Ω*id max. (TBD)	
10	PSE output resistance [10]	Rsense=0.25 RDSON_min=0.1 Ω RDSON_min=0.7*RDSON_max	Rsense=0.25 RDSON_min=0.05 Ω RDSON_min=0.7*RDSON_max

Annex G2: Worst case data base- Notes. -2

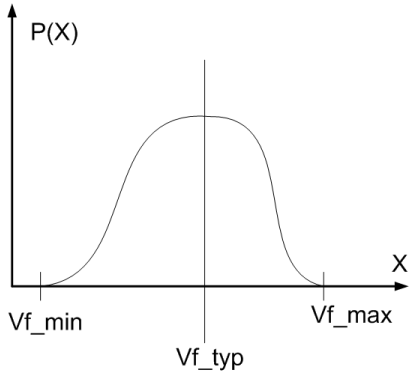
1	Per standard. It is maximum value for solid and stranded wire. The maximum value is close to AWG#26 wire resistance/meter including twist rate effects. **See annex E1.** Due to the fact that patch cords may use AWG#24 cables with stranded (for mechanical flexibility) or solid wire (for improved performance), we will use the AWG#24A for worst case analysis as well. Cordage with AWG#24 wire has 0.0842Ω/m for solid wire and with 10% twist rate it will be 0.09262 Ω/m.
2	We need both data sets (data set 1 and data set 2) to find where is the worst condition for maximum current unbalance. **See Annex B curve and data** showing that at short channel we get maximum P2PRUNB but it may has less concern to us since the current is lower. We need to do all use cases calculation to see where is the maximum current over the pair; at short channel or long channel. The CAT6A cable with AWG#23 has 0.066 Ω/m. Including 12% increase on cable length due to twist rate, the effective cable resistance per meter will be 1.12*6.6 Ω/100m= 0.074 Ω/m. (with 20% twist rate it will be 0.0792 Ω/m)
3	Standard definition per Annex E1 for maximum resistance. We will check how results will be differ when AWG#23 is used for worst case results (lower resistance than standard definition for horizontal cable which is a maximum value.
4	
5	
6	PSE PI and PD PI includes: connector, transformer, resistors. PD PI includes diode bridge.
7	
8	Connector resistance was changed since the difference (60-30) milliohm is not representing Rdiff, it is representing maximum and minimum results of connector resistance of different connectors. To correct it, we change the numbers according to inputs from connector vendors and measured data. See Annex E1-E6 for confirmation.
9	Vf and Rd are worst case numbers of discrete diode which there is no control on Vf and Rd. It needs more investigation to verify that we are not over specify. (Christian is checking it). Normally match components (e.g. matched two diode bridges) are used for 4P operation. Any how ,PD PI spec. will eventually set the requirement.
10	PSE output resistance e.g. Rs_a/b=Rsense+Rdson in addition to winding resistance. See model I Annex F for reference.

Adhoc response, June 24, 2014. Adhoc accept this table

Source: Yair Darshan and Christian Beia

Annex J1: Worst case system level probability analysis

- The characterization data are based on 6 sigma process controlled concept.
- The probability that for the same part number and vendor we will get:
  - Vf_min and Vf_max AND
  - They will be over the same pair AND
  - The same pair of the same polarity is very very small!
- Probability of <(3.4*10^-6)^2=~10^-11
- As a result the realistic Vdiff range (area below the normal curve around the mean value) will be much smaller than the area occupide from Vf_min to Vf_max.
- The above was confirmed by testing very large samples of system P2P_Iun on negative pairs at very short channel and at low current where ONLY PD diode Vdiff are the affecting parameters. The maximum P2P_Iunb (75%) was equivalent to Vdiff=60mV max.
- As a result the worst case realistic Vdiff on pairs of the same polarity will be 60mV and not 110 to 150mV range.



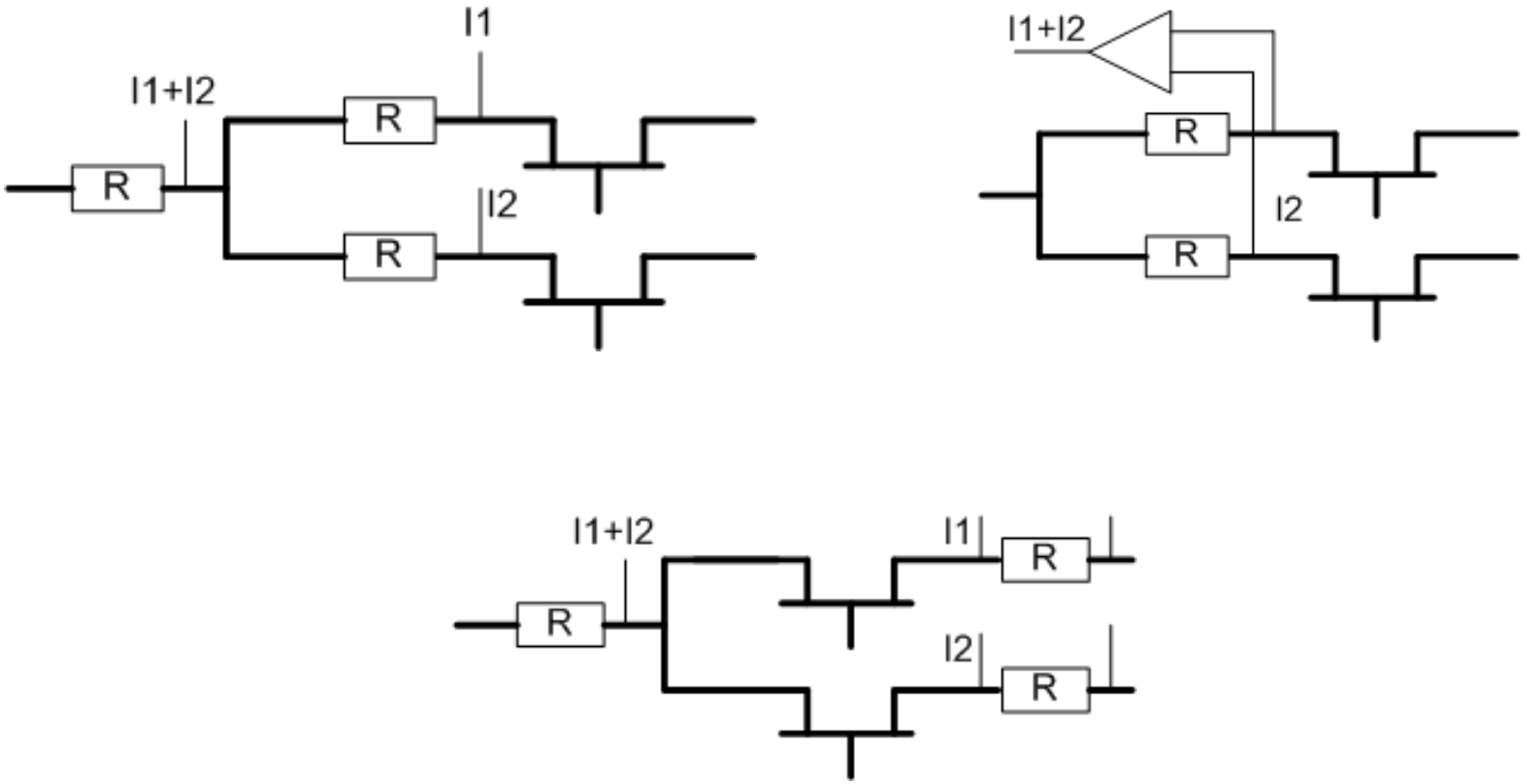
Annex J2: Worst case diode level Vdiff probability analysis

$$Vdiff = Vd_1 - Vd_2 = \frac{n \cdot k \cdot T}{q} \cdot LN\left(\frac{Is_2}{Is_1}\right)$$

- Is2/Is1=10 is possible to happen.
- Is2/Is1=100 has much lower probability to happen.
- n=1 to 1.05 is the highest probability to happen.
- n=2 may happen at very low Vf values and it is not a typical case.
- As a result, the probability to have Vdiff>60mV is significantly reduced
- As a result the probability to have Vdiff between 60mV to 110mV is very small.
- At system level, to have Vf_min and Vf_max on the same pair of the same polarity at the same port at the same time is close to zero.
- Combining both effects leads to the conclusions that realistic Vdiff max will be limited by statistics to <60mV.
- Small samples (120) indicated that the above makes sense.
  - Larger samples are under work and expected to be ready for March 2015.

Annex K – Summing both pairs current

- Possible solutions



Annex L1: Diode Unbalance Vd/Id behavior

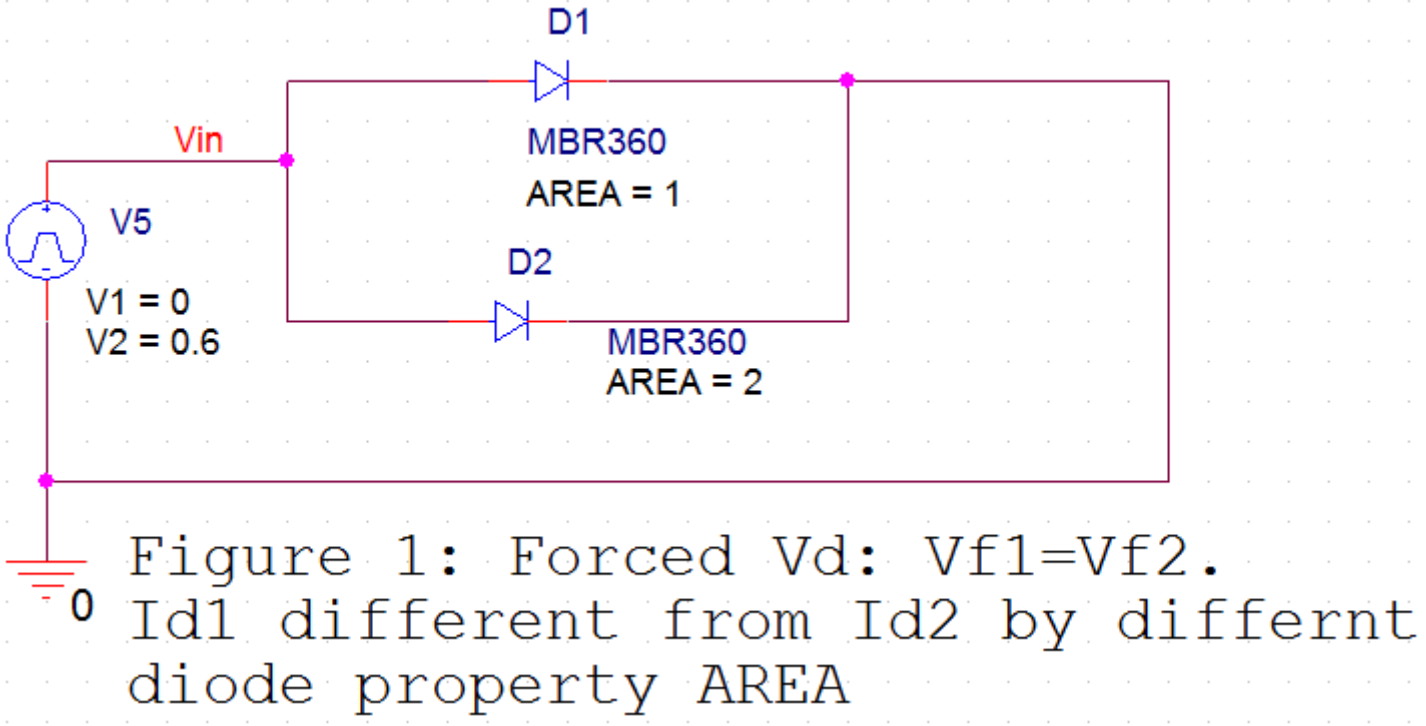
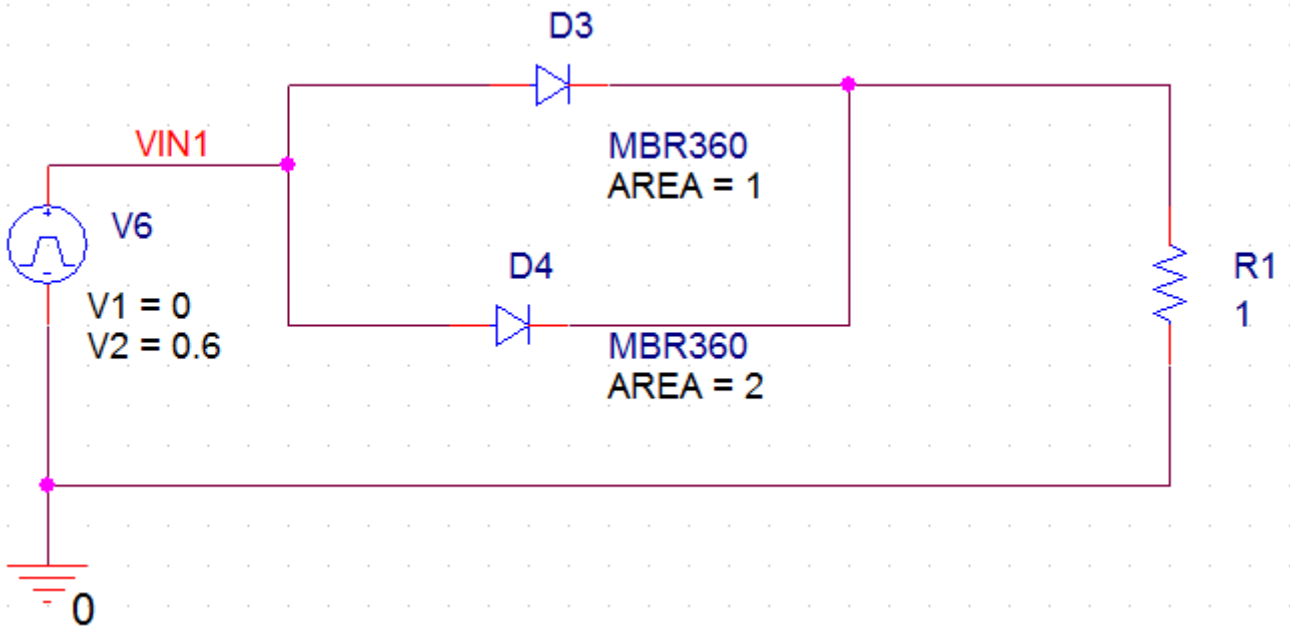


Figure 1: Forced Vd: Vf1=Vf2. Id1 different from Id2 by differnt diode property AREA

- Diode voltage drop is identical =Vin=Vd.
- At high current, Vf=Vd-Id*Rp. Rp is diode internal resistive loss
- ID(2)>ID(1) by factor of 2.

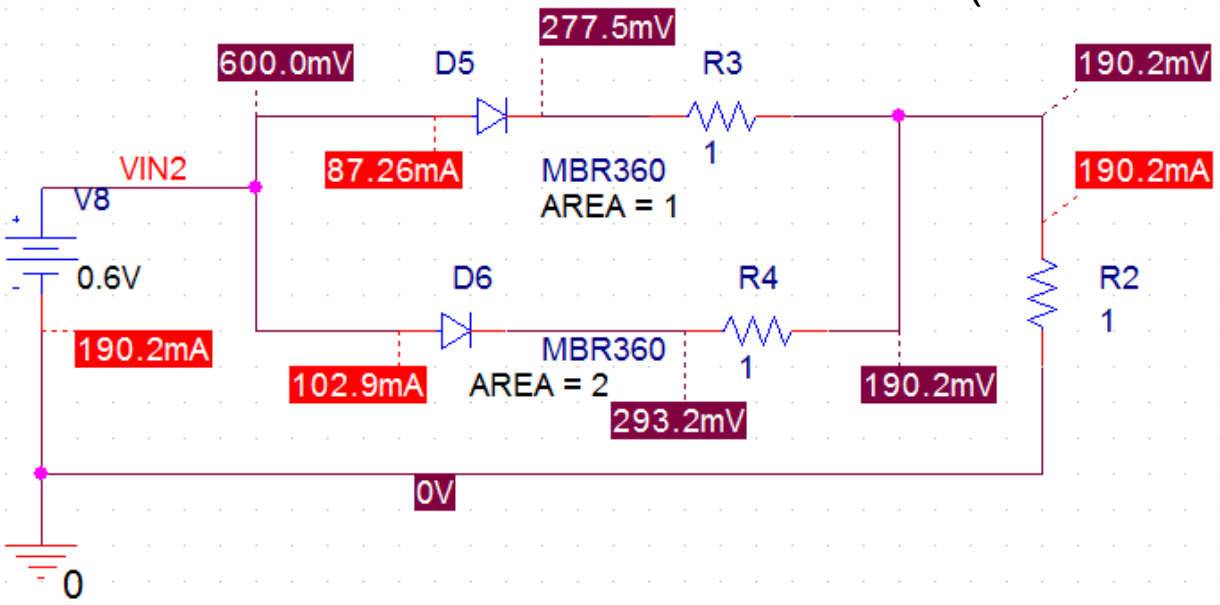
Annex L2: Diode Unbalance Vd/Id behavior



- Figure 2: Forced Vd: Vf1=Vf2.
- Load that limits the current is common to the two diodes.
- Id1 different from Id2 by different diode property AREA.
- Same unbalance ratio will be obtained compared to Figure 1.

Annex L3: Diode Unbalance Vd/Id behavior

Id=(Vin2-VD-Vx)/R3=Is*(exp(Vd/nVt)-1)



- 2. Id will be lower at the diode that has higher voltage drop due too the fact that:

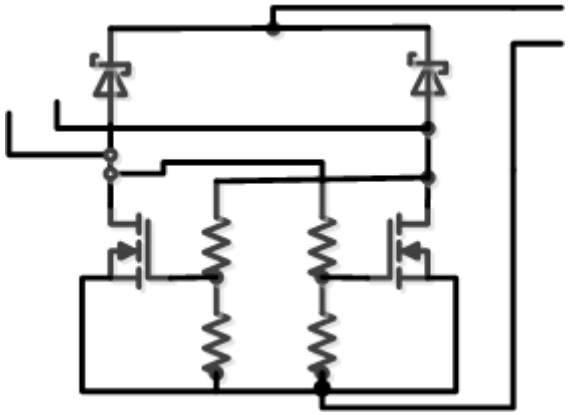
$$Id_5 = \left(\frac{Vin2 - Vd_5 - Vx}{R_3}\right) = Is_5 \cdot \left(\exp^{\frac{Vd_5}{n \cdot Vt}} - 1\right), \quad Id_6 = \left(\frac{Vin2 - Vd_5 - Vx}{R_4}\right) = Is_6 \cdot \left(\exp^{\frac{Vd_6}{n \cdot Vt}} - 1\right)$$

- Due to the fact that D6 has AREA=2 it will have higher current at lower VF than D5.
- Load that limits the current is common to the two diodes.
- Unbalance ratio will be decreased when current is increased when Vin is increased or load resistance is decreased.

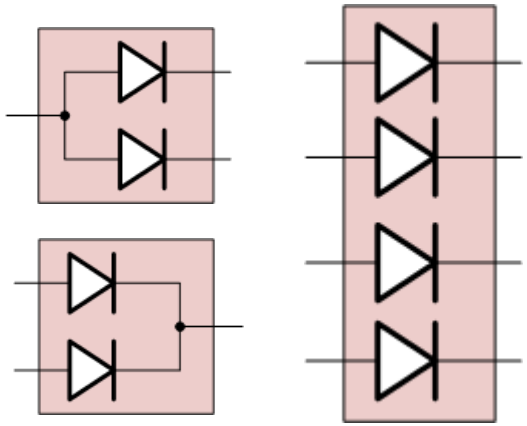
Annex M1: Possible solutions for tight Vdiff or P2P_Iunb in a PD

- **Using two MOSFETs at the low side guarantee** excellent P2P_Iunb at the negative pairs when current is measured at the PSE side)with discrete components due to the fact that the RDSON_DIFF effect on Iunb is much smaller than the effect of discrete two diodes with different Vf.
- In addition, adding resistance in the current path, reduces P2P_Iunb.
- Less power loss than 4 diodes.

(Source: Jean Picard / TI.)



- Improved version of this example is using active diode bridge (4 MOSFETS). Results with excellent P2P_Iunb on both pairs and superior efficiency.



- **Two diodes or 4 diodes in the same package.**
- Vf_max-Vf_min=Vdiff will be significantly lower than discrete two diodes. (sensing the current could be on positive pairs (single port) or negative pairs (single and multi-port systems)

- **Discrete diodes forming diode bridge** (as is the popular way done so far) with limited Vdiff to meet our requirements is possible and exists in the market.
  - We need to ask vendors that this parameter will be specified in their data sheets.

References

1. End to End Channel Pair to Pair resistance unbalance adhoc slides.
   See: http://www.ieee802.org/3/bt/public/Jan15/darshan_xx_0115.pdf
2. http://www.bentongue.com/xtalset/16MeaDio/16MeaDio.html
3. http://pveducation.org/pvcdrom/characterisation/measurement-of-ideality-factor