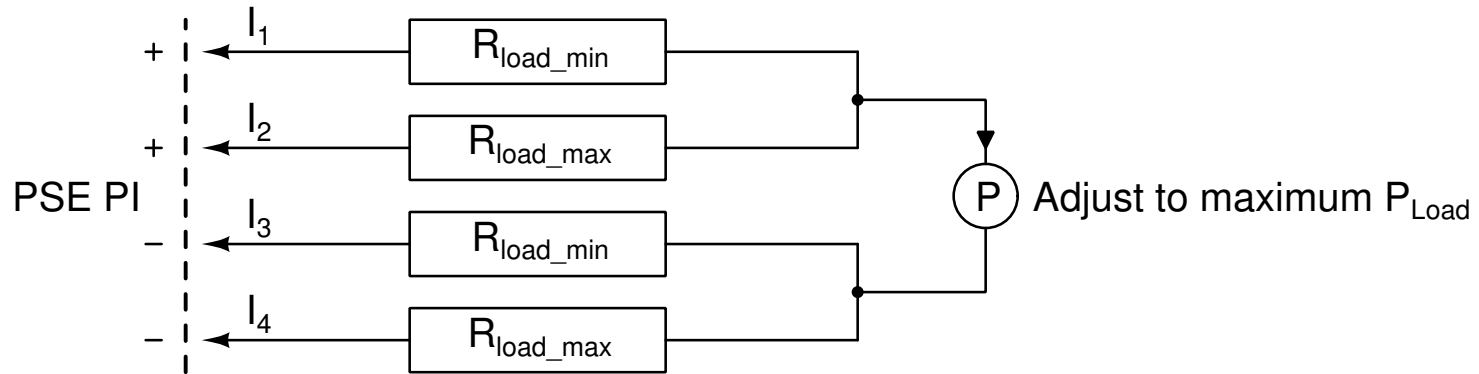


Combined load (PD and channel)



**Figure 33B-4--Current unbalance test circuit**