IEEE802.3 4P Study Group

Classification Current Width Modulation

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Goal of this Presentation

- Continue on the topic of 3-Event classification and address the concerns on the slides in Norfolk

- Propose the Classification Current Width Modulation (CCWM) Table for Type3/Type4 PoE.

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Glossaries

- Type3: Output power between 0W~60W at PSE;

- Type4: Output power between 0W~97.5W (TBD) at PSE;

- Class5: 40mA classification current with 3-Event;

- Class6 :40mA classification current with 4-Event.

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CCWM

• After successful detection, Type3 PSE checks if Classification Current is 40mA;

 •If YES, Initiates 3-Event;

 •If NO, probes 1-Event;

•The first-two-Event is the same as 3at;

•The 3rd Mark Event Timing TME3 is the same as TME1/TME2;

•The 3rd Class Event Timing TCLE3

 •TCLE3 =2xTCLE* → 60W (PSE);

•PSE Checks the Classification Current Width Ratio (CCWR) of the 3rd Event

*TCLE=TCLE1=TCLE2
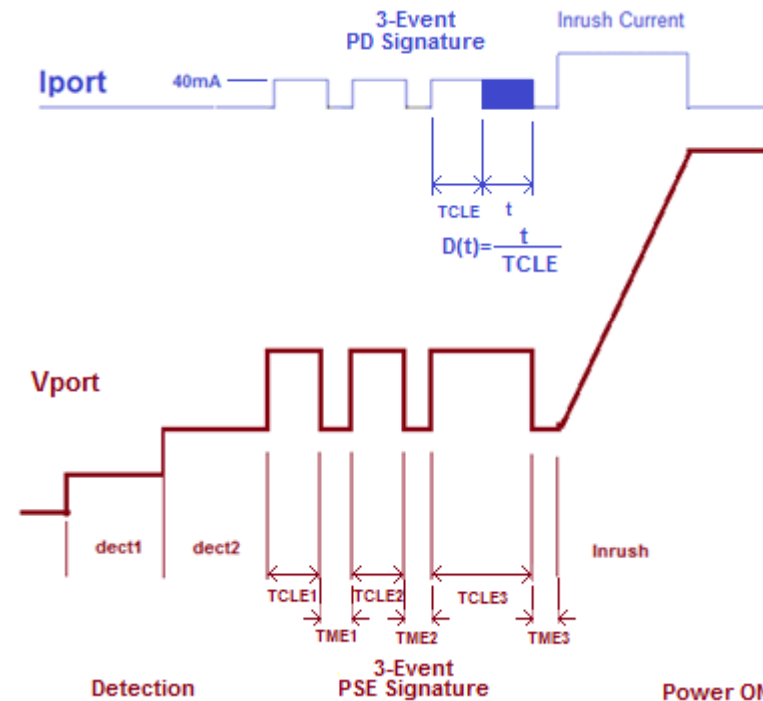
PD Classification Current Width Ratio (CCWR)

- In the 3rd Event, the Type3 PD responds to PSE with D(t);
  - $D(t)=t/TCLE$

    Here, t is the time when the PD provides classification current in the 2nd TCLE of TCLE3.
  - t is based on how PD is configured.

- The D(t) specifies/supports the followings of PD
  - Max Input Power
  - Green MPS
  - Auto Power Class

- For Type4 PoE, the CCWM will be implemented in 4th Event, the 3rd will be identical as the 1st and 2nd event.

V CLASS

3rd Event

1st TCLE | 2nd TCLE

TCEL3=2*TCLE

I CLASS

TCLE   t

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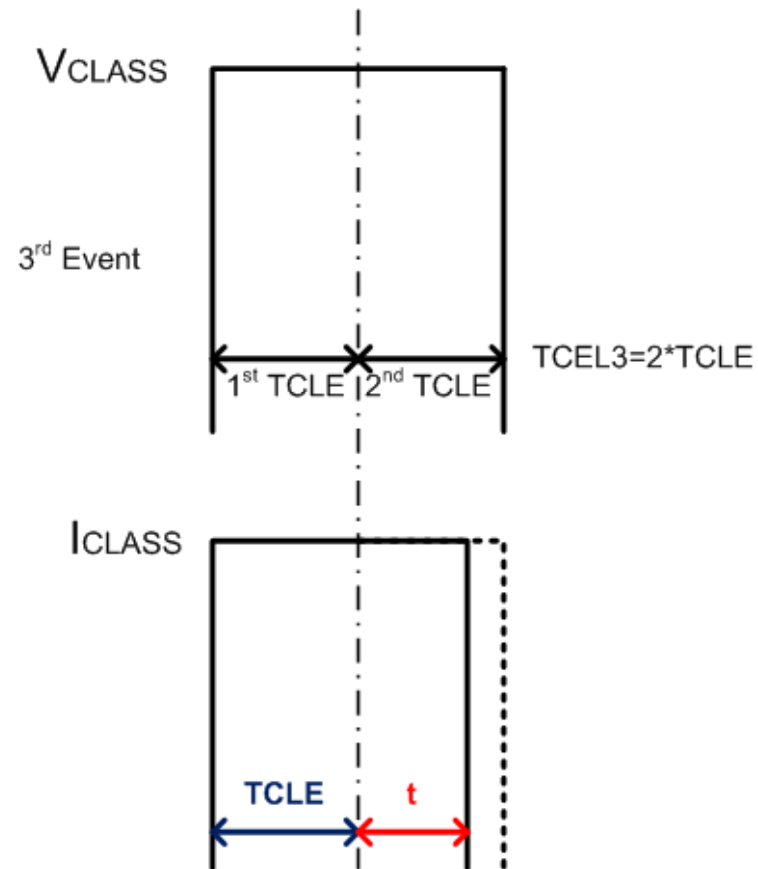
Type3 Classifications (TBR)

D(%)@PD	PD Type	Class	Power (W)
96~100	2	4	30
86~95	3	51	30
76~85	3	51 or 52	
66~75	3	52	37.5
56~65	3	52 or 53	
46~55	3	53	45
36~45	3	53 or 54	
26~35	3	54	52.5
16~25	3	54 or 55	
6~15	3	55	60
0~5	3	56	AUTO

Type4 Classifications (TBR)

D(%)@PD	PD Type	Class	Power (W)
96~100	2	4	30
86~95	4	61	60
76~85	4	62 or 62	
66~75	4	62	75
56~65	4	62 or 63	
46~55	4	63	82.5
36~45	4	63 or 64	
26~35	4	64	90
16~25	4	64 or 65	
6~15	4	65	97.5
0~5	4	66	AUTO

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Benefits

- Provide Type3/4 Signature for both PSE and PD

- Backwards compatible with Type1 and Type2 PoE

- Reliable on CCWR Check

- Capable of providing more options for Mutual-Identification

- Easily to be extended to Type4 PD with D(t) by adding one more event

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Appendix

Power Channel RC Impact on Current Width Detection
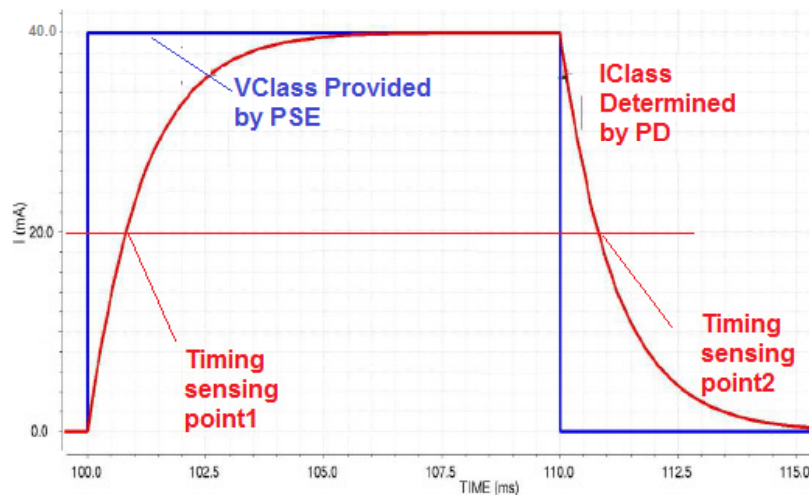
- The capacitor at PD is 0.15uF as max and its impact is very minimum

- Cable is 2x10Ohm assuming the same cable as in Tpye2

- TCLE range of 6~30ms

Challenges to Silicon Vendors

Circuits Needed at PD

- Oscillator-existing if PWM controller or MPS integrated

- Counter--existing if PWM controller or MPS integrated

- Logic circuit- to add

- 1-2% of the die size –total added area of the classification circuit

PSE

- Width Ratio detection on Iclass

- TCLE inconsistence between three classification events due to Temperature change

  > Take the 2nd TCLE as baseline for Ratio measurement;

  > Counter and power area are not sitting at the same area.

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Classification Table

Measured I_{Class}	Classification (Type2)	Classification (Type3)	Classification (Type4)
0 mA to 5.00 mA	Class 0	Class 0	Class 0
> 5.00 mA and < 8.00 mA	May be Class 0 or 1	May be Class 0 or 1	May be Class 0 or 1
8.00 mA to 13.0 mA	Class 1	Class 1	Class 1
> 13.0 mA and < 16.0 mA	Either Class 1 or 2	Either Class 1 or 2	Either Class 1 or 2
16.0 mA to 21.0 mA	Class 2	Class 2	Class 2
> 21.0 mA and < 25.0 mA	Either Class 2 or 3	Either Class 2 or 3	Either Class 2 or 3
25.0 mA to 31.0 mA	Class 3	Class 3	Class 3
> 31.0 mA and < 35.0 mA	Either Class 3 or 4	Either Class 3 or 4	Either Class 3 or 4
35.0 mA to 45.0 mA	Class 4	Class 5	Class 6
> 45.0 mA and < 51.0 mA	Either Class 4 or invalid	Either Class 4 or invalid class	Either Class 4 or invalid class

NOTE—A Type 1 PSE may ignore I_{Class} and report Class 0.