33.2.8 Power supply output

Info (not part of baseline)

The DC MPS text can be clarified by using $I_{Hold-2P}$ for all currents that deal with a pairset, and I_{Hold} for currents that deal with 4P current. The old table also does not really say what the requirements are for Type 3/4 PSEs operating in 2P mode. A new row is added for this.

Remove footnote 3 and footnote 4.
Split Table 33–17 item 20 into two items as follows:

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
20	DC MPS current to be met on at least one pairset, as function of the assigned Class						
		$I_{Hold-2P}$	A	0.005	0.010	1, 2	See 33.2.10.1.2
	Single-signature PD, Class 0 to 4, 2-pair			0.004	0.009	3, 4	
	Single-signature PD, Class 0 to 4, 4-pair			0.002	0.005	3, 4	
	Single-signature PD, Class 5 to 8			0.002	0.007	3, 4	
	DC MPS current to be met on each pairset						
	Dual-signature PD	$I_{Hold-2P}$	A	0.002	0.007	3, 4	
21	DC MPS total current to be met when the sum of both pairs with the same polarity is measured, as function of the assigned Class						
	Single-signature PD, Class 0 to 4	I_{Hold}	A	0.004	0.009	3, 4	See 33.2.10.1.2.
	Single-signature PD, Class 5 to 8			0.004	0.014	3, 4	

33.2.10.1.2 PSE DC MPS component requirements

Info (not part of baseline)

Changes:

- The paragraphs on Type 1 and Type 2 used both $I_{Port-2P}$ and I_{Port}. Changed to I_{Port}.
- The first line indicates that the Table contains conditions on which values to use in which circumstances. I've removed "the applicable" from the rest of the text as it is redundant.

~~All Types of~~ A PSE, depending on the connected Type of PD, shall use the applicable I_{Hold} min, I_{Hold} max, T_{MPS} and T_{MPDO} values as defined in Table 33–17. The specification for T_{MPS} in Table 33–17 applies only to the DC MPS component.

A Type 1 and Type 2 PSE shall consider the DC MPS component to be present if ~~$I_{Port-2P}$~~ I_{Port} is greater than or equal to the applicable ~~I_{Hold} max~~ $I_{Hold-2P}$ max continuously for a minimum of T_{MPS}. A Type 1 and Type 2 PSE shall consider the DC MPS component to be absent if ~~$I_{Port-2P}$~~ I_{Port} is less than or equal to the applicable ~~I_{Hold} min~~ $I_{Hold-2P}$ min. A Type 1 and Type 2 PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of the applicable ~~I_{Hold}~~ $I_{Hold-2P}$.

A Type 1 and Type 2 PSE shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 1 and Type 2 PSE shall not remove power from the ~~port~~ PI when I_{Port} is greater than or equal to ~~I_{Hold} max~~ $I_{Hold\text{-}2P}$ max continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–17. This allows a PD to minimize its power consumption.

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ of the pairset with the highest current is greater than or equal to $I_{Hold\text{-}2P}$ max or the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity is greater than or equal to ~~the applicable~~ I_{Hold} max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ of the pairset with the highest current is less than or equal to $I_{Hold\text{-}2P}$ min or the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity ~~are~~ is less than or equal to ~~the applicable~~ I_{Hold} min. A Type 3 or Type 4 PSE, when connected to a single-signature PD, may consider the DC MPS component to be either present or absent if $I_{Port\text{-}2P}$ of the pairset with the highest current is within the range of $I_{Hold\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity is within the range of ~~the applicable~~ I_{Hold}.

A Type 3 and Type 4 PSE, when connected to a single-signature PD, shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}. A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall not remove power from the PI when DC MPS has been present within the T_{MPS} + T_{MPDO} window. This allows a PD to minimize its power consumption.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present or absent on ~~a~~ each pairset independently ~~from the other pairset~~. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present on a pairset if $I_{Port\text{-}2P}$ is greater than or equal to ~~the applicable~~ $I_{Hold\text{-}2P}$ max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be absent on a pairset if $I_{Port\text{-}2P}$ is less than or equal to ~~the applicable~~ $I_{Hold\text{-}2P}$ min. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may consider the DC MPS component on a pairset to be either present or absent if $I_{Port\text{-}2P}$ is within the range of ~~the applicable~~ $I_{Hold\text{-}2P}$.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall not remove power from a pairset when DC MPS has been present on both pairsets every T_{MPS} + T_{MPDO}. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may maintain power on a pairset if DC MPS has been present on that pairset every T_{MPS} + T_{MPDO}. This allows a PD to minimize its power consumption.

33.3.8 PD Maintain Power Signature

A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI. A PD that does not maintain the MPS components mentioned above may have its power removed within the limits of T_{MPDO} as specified in Table 33–17.

~~The MPS shall consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}.~~
For a single-signature PD the MPS shall consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}. I_{Port_MPS} is the total current drawn by the PD at the PI.

For a dual-signature PD the MPS shall consist of current draw equal to or above $I_{Port\_MPS\text{-}2P}$ on each powered pairset independently for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}. $I_{Port\_MPS\text{-}2P}$ is the current drawn by the PD on a pairset.

The values of I_{Port_MPS}, $I_{Port\_MPS\text{-}2P}$, T_{MPS_PD}, and T_{MPDO_PD} are shown in Table 33–30. A Type 1 or Type 2 PD, or a PD connected to a Type 1 or Type 2 PSE, shall in addition show the input impedance with resistive and capacitive components defined in Table 33–29.

Replace Table 33–30 item 1 by the two items that follow:

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Condition
1	Total input current as function of assigned Class to a single-signature PD						
	Class 0 to 4	I_{Port_MPS}	A	0.010		All	
	Class 5 to 8			0.016		3, 4	
2	Input current on each powered pairset of a dual-signature PD						
	Class 1 to 5	I_{Port_MPS-2P}	A	0.008		3, 4	