Guiding Principles (not part of baseline)

4-pair operation

Top-level state diagram:

1) 3 Functions shall be performed, in any order:
- do_detect_pri
- do_detect_sec
- do_cxn_chk

2) Functions may be started at any time: staggered, “quasi-simultaneous”, or simultaneous

3) Time between functions must be no greater than 400ms (i.e., tcc2det, tdet2det)

4) “do_detect_*” functions must be no longer than 500ms (i.e., tdet)

“SISM” state diagrams:

1) When “sism = true” PRI/SEC may exit “ENTRY_*” state at any time: staggered, “quasi-simultaneous”, or simultaneous

2) PRI/SEC tpon timers dictate when PRI/SEC may transition from “ENTRY_*” to class on that pairset, re-perform detection on that pairset, or exit to “WAIT_*” state for connection check/detection to be re-performed at top-level

2-pair operation

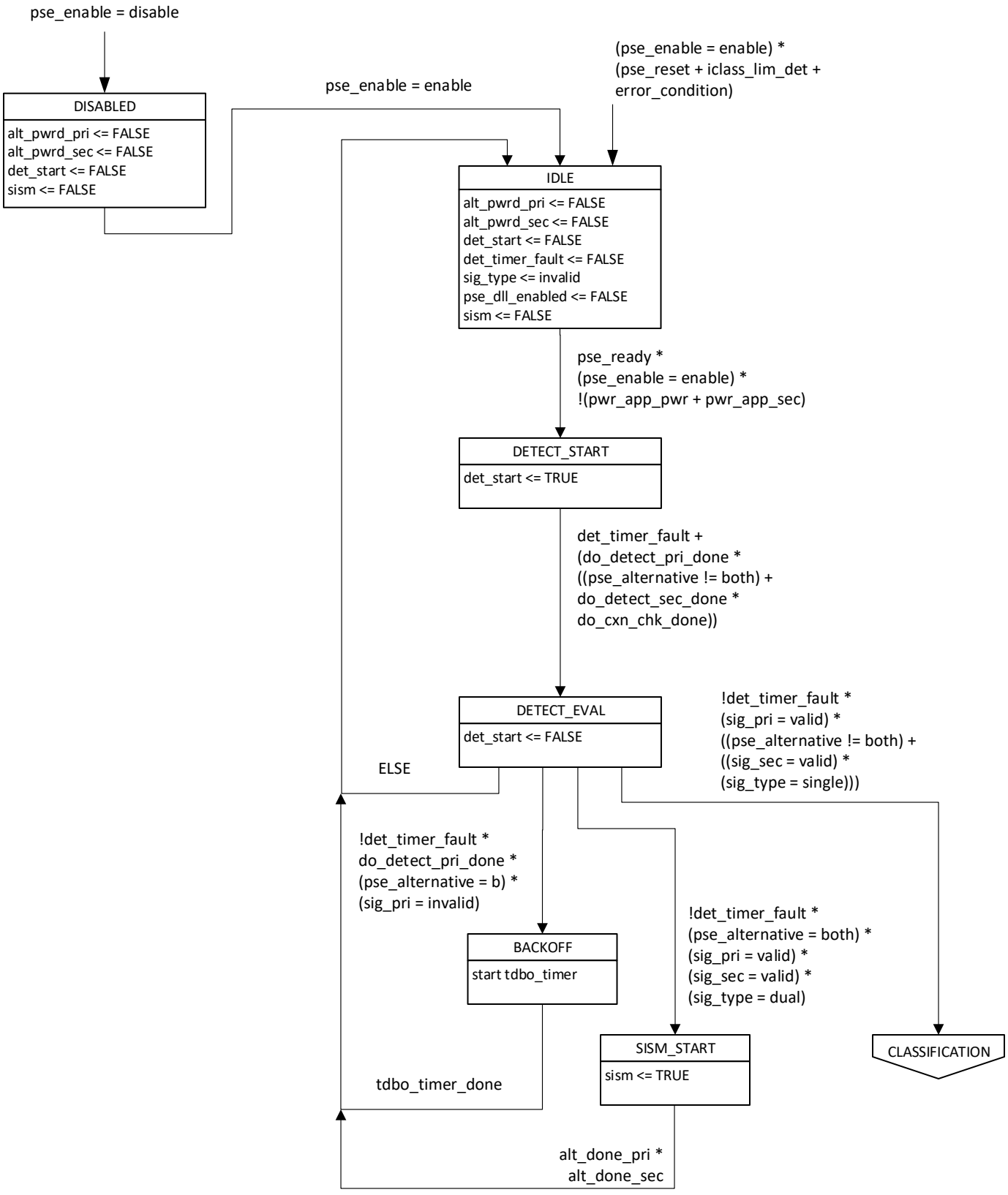
Top-level state diagram:

1) 1 Function shall be performed
- do_detect_pri

2) “do_detect_pri” must be no longer than 500ms (i.e., tdet)

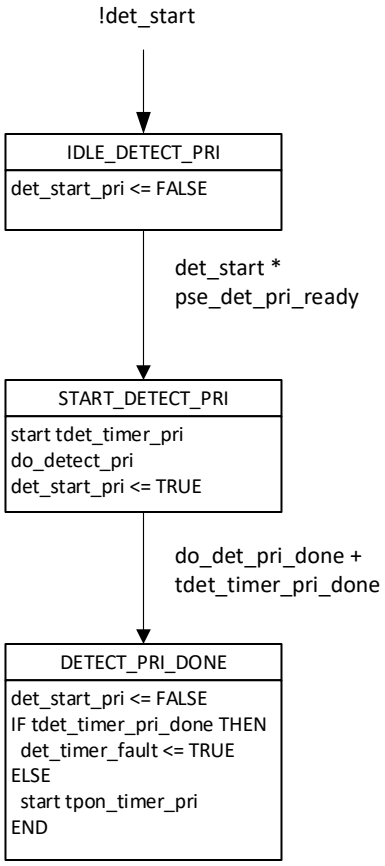
3) Midspan backoff may be observed as described in text (pse_alternative = b, sig_pri = invalid)

Replace Pages 117, 119 (top level PSE state diagram) as follows:

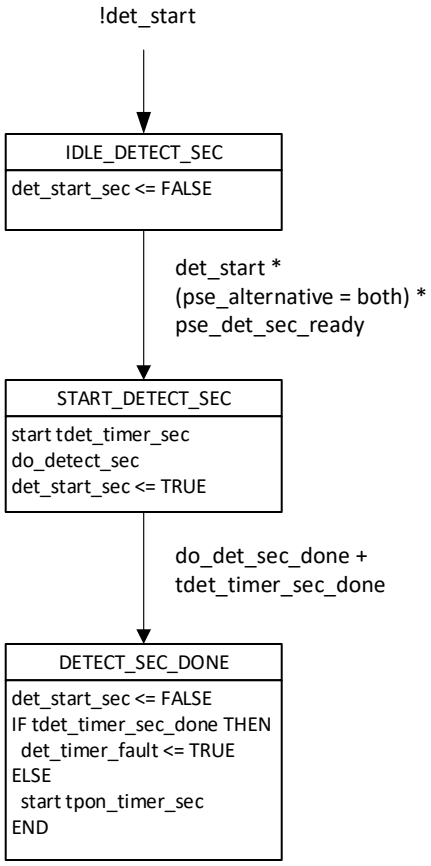


INFO (not part of baseline): "ELSE" is valid and defined per 21.5.3(e), which is currently referenced by Clause 145 PSE SD

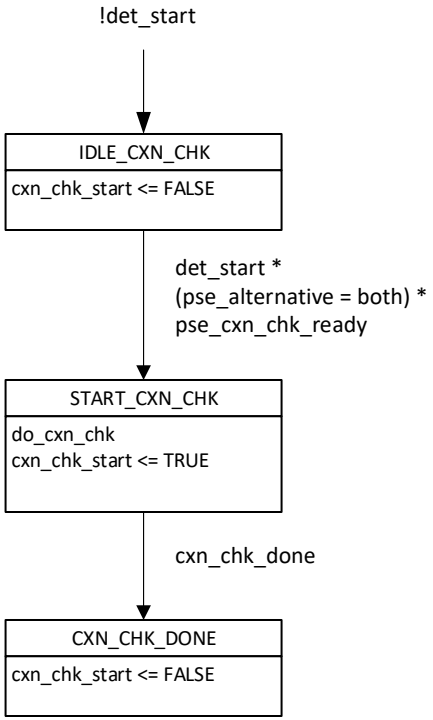
Add the following to PSE state diagram:



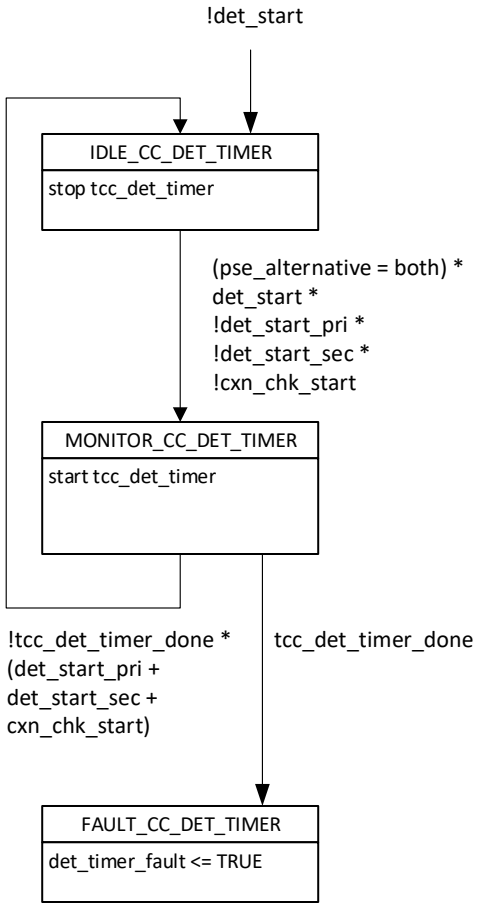
Detection Sub-SD:
Primary Alternative



Detection Sub-SD:
Secondary Alternative

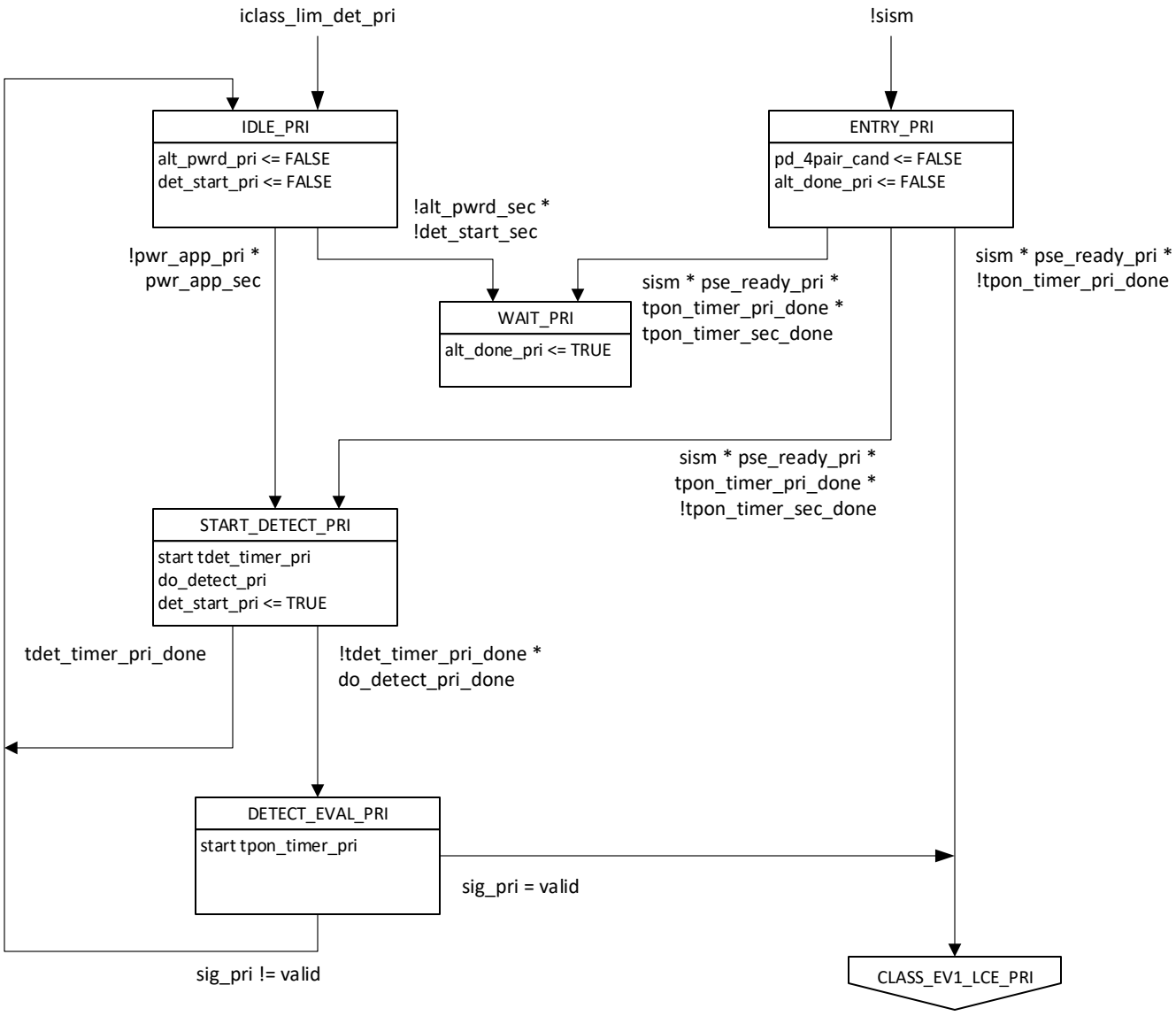


Connection Check Sub-SD

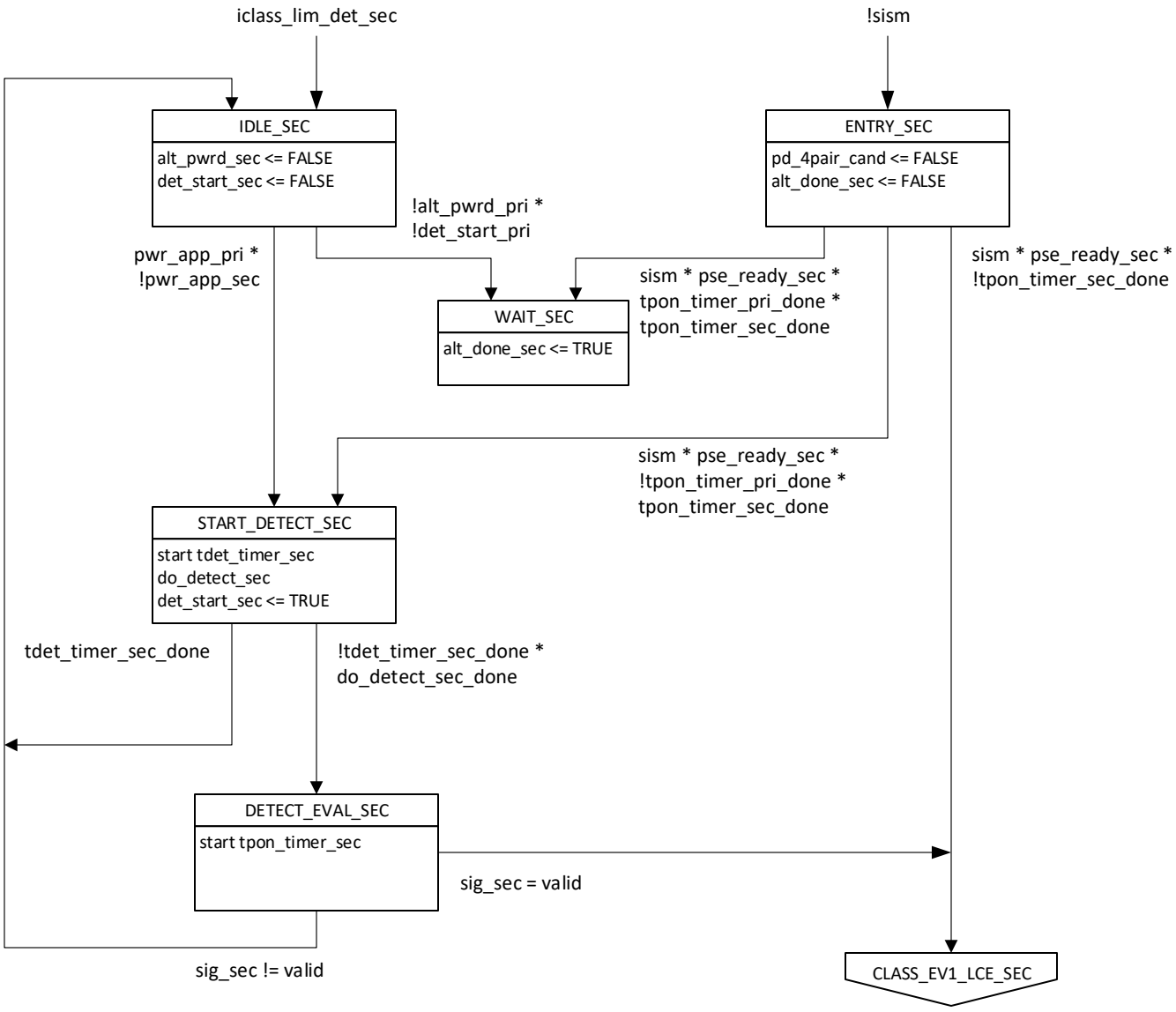


Detection/CxnChk Watchdog

Replace Page 124 (SISM, Primary Alternative) as follows:



Replace Page 126 (SISM, Secondary Alternative) as follows:



Modifications to variables and text:

1) Modify 145.2.5.4:
Modify the following variable:
pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3). The value of this variable may be modified in an implementation-specific manner in the IDLE state.

Values:

a: The PSE uses PSE pinout Alternative A.

b: The PSE uses PSE pinout Alternative B.

both: The PSE uses both Alternative A and Alternative B.

Add the following variables:

det_start

A variable used by the top level state diagram to control the connection check and detection state diagrams.

Values:

FALSE: PSE has disabled connection check and detection by the top level state diagram.

TRUE: PSE has enabled connection check and detection by the top level state diagram.

det_timer_fault

A variable used by the connection check and detection state diagrams to indicate a timer fault has occurred during the Connection Check/Detection sequence.

Values:

FALSE: A timer fault has not occurred during the Connection Check/Detection sequence.

TRUE: A timer fault has occurred during the Connection Check/Detection sequence.

cxn_chk_start

A variable used by the connection check state diagram to indicate connection check is being performed.

Values:

FALSE: PSE is not performing connection check.

TRUE: PSE is performing connection check.

pse_det_ready_pri

A variable that is asserted in an implementation-dependent manner to initiate detection on the Primary Alternative during the Connection Check/Detection sequence. PSEs are subject to timing constraints limiting the duration of detection, intra-function delay, and power turn on time; See T_{cc_det} in Table 145-7, T_{det} and T_{pon} in Table 145-16.

Values:

FALSE: PSE is not ready to perform detection on the Primary Alternative during the Connection Check/Detection sequence.

TRUE: PSE is ready to perform detection on the Primary Alternative during the Connection Check/Detection sequence.

pse_det_ready_sec

A variable that is asserted in an implementation-dependent manner to initiate detection on the Secondary Alternative during the Connection Check/Detection sequence. PSEs are subject to timing constraints limiting the duration of detection, intra-function delay, and power turn on time; See T_{cc_det} in Table 145-7, T_{det} and T_{pon} in Table 145-16.

Values:

FALSE: PSE is not ready to perform detection on the Secondary Alternative during the Connection Check/Detection sequence.

TRUE: PSE is ready to perform detection on the Secondary Alternative during the Connection Check/Detection sequence.

pse_cxn_chk_ready

A variable that is asserted in an implementation-dependent manner to initiate connection check during the Connection Check/Detection sequence. PSEs are subject to timing constraints limiting the duration of detection, intra-function delay, and power turn on time; See T_{cc_det} in Table 145-7, T_{det} and T_{pon} in Table 145-16.

Values:

FALSE: PSE is not ready to perform connection check during the Connection Check/Detection sequence.

TRUE: PSE is ready to perform connection check during the Connection Check/Detection sequence.

pse_ready_pri

A variable that is asserted in an implementation-dependent manner to probe the Primary Alternative in the semi-independent dual-signature state diagram. PSEs are subject to timing constraints limiting the duration of detection and power turn on time; See T_{det}, T_{pon} in Table 145-16.

Values:

FALSE: PSE is not ready to perform detection on the Primary Alternative in the semi-independent dual-signature state diagram.

TRUE: PSE is ready to perform detection on the Primary Alternative in the semi-independent dual-signature state diagram.

pse_ready_sec

A variable that is asserted in an implementation-dependent manner to probe the Secondary Alternative in the semi-independent dual-signature state diagram. PSEs are subject to timing constraints limiting the duration of detection and power turn on time; See T_{det}, T_{pon} in Table 145-16.

Values:

FALSE: PSE is not ready to perform detection on the Secondary Alternative in the semi-independent dual-signature state diagram.

TRUE: PSE is ready to perform detection on the Secondary Alternative in the semi-independent dual-signature state diagram.

2) Modify 145.2.5.5:

Add the following timer:

tcc_det_timer

A timer used during the Connection Check/Detection sequence to limit the time between the completion of any function and the beginning of any other function; See T_{cc_det} in Table 145-7.

Remove the following timers:

~~tcc2det_timer~~

~~tdet2det_timer~~

3) Modify 145.2.6.1, paragraph 1 as follows:

PSEs that will deliver power on both pairsets shall complete a connection check prior to the classification of a PD as specified in 145.2.7 to determine if both pairsets are connected to a single-signature PD configuration~~,~~ or a dual-signature PD configuration~~, or both pairsets are invalid~~.

4) Remove 145.2.6.1, paragraphs 4 and 5:

~~The specification of T_{cc2det}, defined in Table 145–7, applies to the time between the end of connection check and the beginning of detection on at least one pairset. If the connection check takes place after the beginning of detection, this specification does not apply.~~

~~The specification of $T_{det2det}$, defined in Table 145–7, applies to the time between the end of detection on the first pairset to the beginning of detection on the other pairset when the second detection occurs before power up on the first pairset.~~

5) Add the following to 145.2.6.1, beneath "NOTE—":

The specification of T_{cc_det}, defined in Table 145–7, applies to the time between the end of any function and beginning of any other function during the Connection Check/Detection sequence.

6) Replace Table 145-7 with the following:

Item	Parameter	Symbol	Unit	Min	Max	Additional Information
1	Connection Check/Detection inter-function time	T_{cc_det}	s		0.4	