



AHEAD OF WHAT'S POSSIBLE™

Unbalance

Rev. 3

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- ▶ A new variable “ $I_{\text{Unbalance-2p}}$ ” was introduced in Draft 3.1 and is used in place of $I_{\text{Con-2p-unb}}$ in some areas
- ▶ In Draft 3.1, $I_{\text{Con-2p-unb}}$ has the same value as $I_{\text{Unbalance-2p}}$
- ▶ Unbalance interoperability has been compromised
 - $I_{\text{Con-2p-unb}}$ limits were increased in Draft 3.1 in such a way that both the PSE and PD may now be more unbalanced and *interoperability is not guaranteed*
 - **Fix $I_{\text{Con-2p-unb}}$ limits**

- ▶ $I_{\text{Unbalance-2p}}$ (550mA) based on worst case cable/connection/diode model delivering 40W
- ▶ System Unbalance system models are calibrated with:
 - Diode area mismatch of 10
 - $R_{\text{PSE_alpha}} = 2.182$ ($R_{\text{PSE_alpha}}$ is the gain factor in Eqn. 145-13)
 - $I_{\text{Con-2p,max}}$ was measured as 550mA and this was used as the $I_{\text{Con-2p-unb}}$ limit until Draft 3.1

$$0 < R_{\text{PSE_max}} \leq \left\{ \begin{array}{ll} 2.182 \times R_{\text{PSE_min}} - 0.04 & \text{for Class 5} \\ 1.999 \times R_{\text{PSE_min}} - 0.04 & \text{for Class 6} \\ 1.904 \times R_{\text{PSE_min}} - 0.03 & \text{for Class 7} \\ 1.832 \times R_{\text{PSE_min}} - 0.03 & \text{for Class 8} \end{array} \right\}_{\Omega} \quad (145-13)$$

where

$R_{\text{PSE_max}}$ is, given $R_{\text{PSE_min}}$, the highest allowable common mode effective resistance in the powered pairs of the same polarity

$R_{\text{PSE_min}}$ is the lower PSE common mode effective resistance in the powered pairs of the same polarity

Class 5 Case Study

- ▶ Draft 3.1 $I_{\text{Unbalance-2p}}$ was changed to 560mA to provide margin.
 - Now, using the PSE test from table 145-18, $R_{\text{PSE_alpha}}$ can be changed to 2.67 and pass the compliance test
 - That is the PSE can be more unbalanced and pass the hardware compliance test

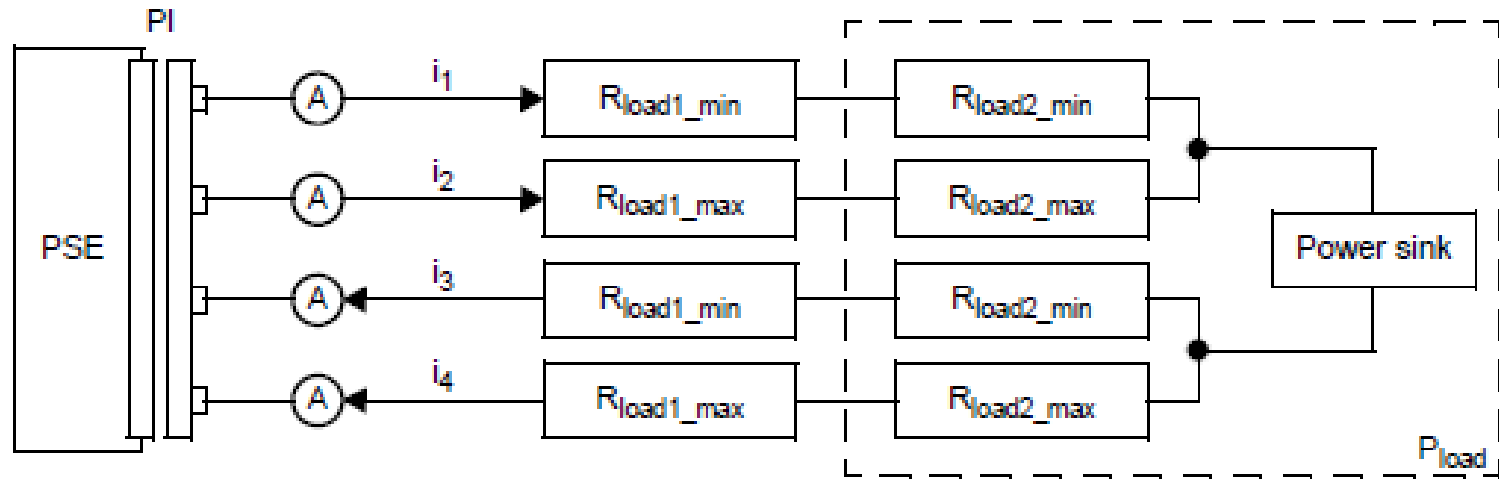
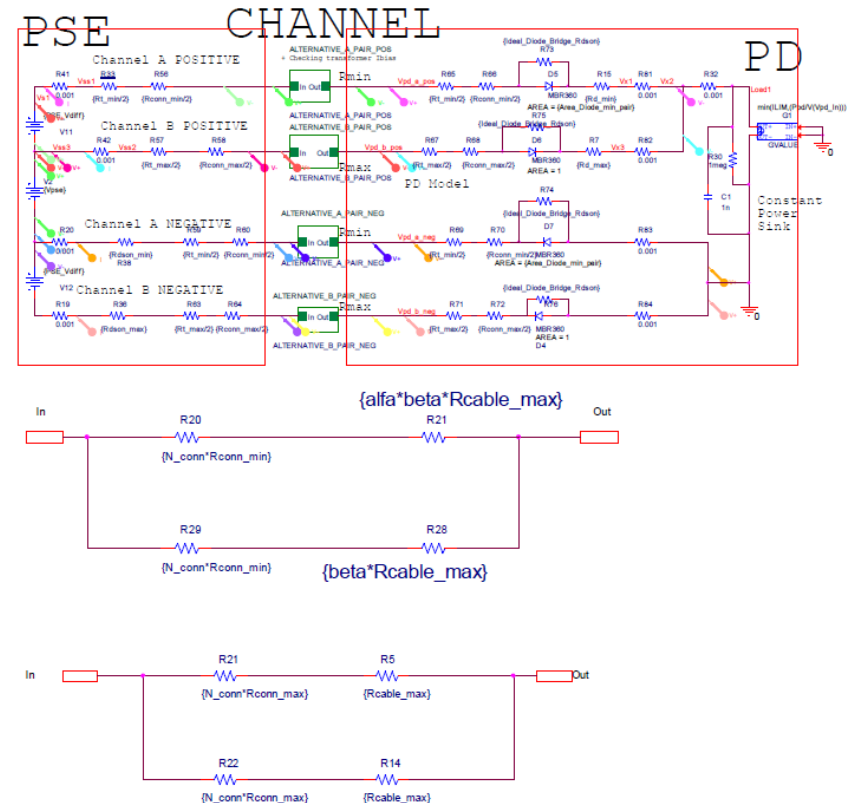


Figure 145-22—PSE PI unbalance specification and system resistance unbalance

- ▶ Plugging $R_{\text{PSE_alpha}} = 2.67$ back into the System Unbalance model gives $I_{\text{Unbalance-2p,max}} = 571\text{mA}$
- ▶ This PSE passes the compliance test but may fail to interoperate



Credit: darshan_01_0317

How do we add margin?

- ▶ We need two unbalance numbers
 - $I_{\text{Unbalance-2p}}$ for the hardware unbalance test (component unbalance contribution)
 - $I_{\text{Con-2p-unb}}$ for the system at runtime (software-controlled current threshold)
 - The hardware test limit must be less than the runtime unbalance limit to ensure margin
- ▶ $I_{\text{Unbalance-2p}}$ is the hardware unbalance test
 - PSEs and PDs should not exceed $I_{\text{Unbalance-2p}}$ when connected to the test load/source
 - $I_{\text{Unbalance-2p}}$ should use the $I_{\text{Con-2p-unb}}$ numbers from Draft 3.0
 - Draft 3.0 $I_{\text{Con-2p-unb}}$ numbers define system performance given PSE, cable and PD unbalance allocations
- ▶ $I_{\text{Con-2p-unb}}$ is the runtime test
 - A PSE should not remove power from a PD until at least $I_{\text{Con-2p-unb}}$ is drawn from a pairset
 - $I_{\text{Con-2p-unb}}$ should maintain the numbers specified in Draft 3.1