New PD Classification Scheme Proposal for PoDL

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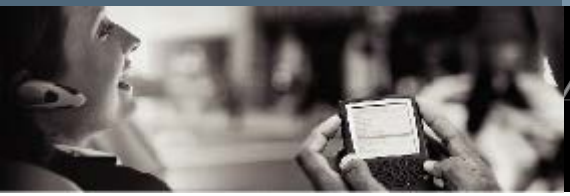

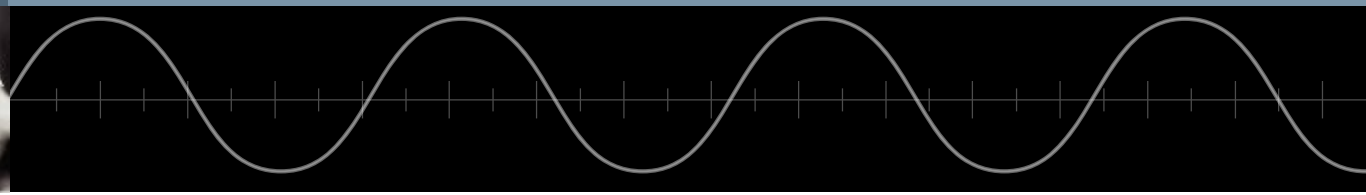

PoDL Power Classification Scheme Goals

- The standard should only constrain parameters required to ensure interoperability.
- Maximum PI current for a PD power/voltage class should be constrained by the standard.
  - This ensures interoperability of the coupling networks.
- The standard should not attempt to constrain the power reserve budget for link segment loss.
  - Maximum allowed link segment resistance is intentionally not addressed by the standard.

New PD Class Table Paradigm

- State Required PD Class Power and Voltage.
- Classes are referenced by Power/Voltage, e.g. 5W/12V class or 2W/5V class.
- Constrain Maximum PI Current:
  - A PD shall not consume any more current and power than is allowed by its class.
  - PD V_{PI} shall be greater than $0.8*V_{class}$.
    - Somewhat arbitrary - voltage tolerance may need to vary by class.
  - A PSE must be able to source enough power and voltage in order to deliver the required power and voltage to the PD while compensating for voltage drop in the link segment.

Proposed PoDL PD Class Table Format

	2W	5W	10W	25W	60W	Open Power Class
5V (-20%)	0.50A	N/A	N/A	N/A	N/A	-
12V (-20%)	0.21A	0.52A	1.04A	N/A	N/A	-
48V (-20%)	0.05A	0.13A	0.26A	0.65A	1.56A	-
Open Voltage Class	-	-	-	-	-	-

Table 200-1 – Maximum PI Current vs. PD Power and Voltage

Link Segment Resistance Scenarios

- AWG 26, 15m link segment:
  - Loop resistance at 20°C is 4.2Ω
  - A 5W/12V constant power PD with V_{PI}>9.6V will require a PSE V_{PI}>11.78V with <1.14W of resulting link segment loss.
- AWG 22, 40m link segment:
  - Loop resistance at 20°C is 4.43Ω
  - A 10W/12V constant power PD with V_{PI}>9.6V will require a PSE V_{PI}>14.2V with <4.8W of resulting link segment loss.
- Link segment resistance data taken from mueller_3bu_01_0114.pdf.
- Wire resistance varies as 3900 ppm/°C.

Other Considerations

- The PSE shall determine if it can power a PD given its own source resistance and the link segment resistance.
  - Engineered systems address this by design.
  - Plug-and-play systems must be able to determine link segment resistance and adjust V_{PSE} as needed in order to deliver the required power and voltage to the PD.
- What should the min/max limits be for PD class voltage?
  - The minimum limit drives the maximum required PI current.

Questions?