0.0.0.1 Link Segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	DC loop resistance	104.2	M	Yes [ ]	Less than 6.0Ω for 12V unregulated system power classes and less than 6.5Ω for all other system power classes.

0.0.0.2 Power sourcing equipment (PSE)

Item	Feature	Subclause	Status	Support	Value/Comment
PSE1	Voltage and power requirements	104.3.2	M	Yes [ ]	As defined in Table 104-1 for each relevant system class
PSE2	PSE behavior	104.3.3	M	Yes [ ]	In accordance with state diagram shown in Figure 104-4
PSE3	PSE probing	104.3.4	M	Yes [ ]	Probe the PI in order to detect a valid PD signature
PSE4	Complete detection of PD signature	104.3.4	M	Yes [ ]	Within T_{det} as specified in Table 104-2
PSE5	Unsuccessful detection	104.3.4	M	Yes [ ]	Wait at least $T_{restart}$ before reattempting detection
PSE6	Detection currents	104.3.4.1	M	Yes [ ]	Within I_{valid} current range specified in Table 104-2 with a valid PD detection signature as specified in Table 104-4
PSE7	Accept valid PD signature	104.3.4.2	M	Yes[ ]	From link segment with a voltage in the range of V_{good_PSE} for at least T_{sig_hold} in response to a probing current in the range of I_{valid} as specified in Table 104-2
PSE8	Reject invalid PD signature	104.3.4.3	M	Yes [ ]	From link segment that exhibits the following characteristics outlined in Table 104-2 and Table 104-5: a) Voltage less than or equal to $V_{bad_lo_PSE}$max b) Voltage greater than or equal to $V_{bad_hi_PSE}$min
PSE9	Applying full operating voltage at the PI with SCCP enabled	104.3.5	M	Yes [ ]	Only after detection and complete classification in a time less than T_{Class} as specified in Table 104-3
PSE10	T_{Class} timer expired before complete classification	104.3.5	M	Yes [ ]	Complete a new detection cycle before applying any subsequent full operating voltage
PSE11	Providing power to the PSE PI	104.3.6	M	Yes [ ]	To conform to electrical limits in Table 104-3
PSE12	Present invalid PD signature	104.3.6	M	Yes [ ]	As specified in Table 104-5 under all conditions

PSE13	PI SLEEP voltage while in SLEEP state	104.3.6.1	M	Yes [ ]	Within V_{Sleep} range outlined in Table 104-3
PSE14	SLEEEP_SETTLE state	104.3.6.1	M	Yes [ ]	Discharge the PSE PI to the range of V_{Sleep} within a time less than T_{Off}max
PSE15	Enter SLEEEP_SETTLE state	104.3.6.2	M	Yes [ ]	If a valid MFVS is not present at the PI while operating in the POWER_ON state
PSE16	PI discharge while in SLEEP_SETTLE state	104.3.6.2	M	Yes [ ]	To the range of V_{sleep} with a current greater than $I_{discharge}$
PSE17	POWER_UP and POWER_ON state operation	104.3.6.2.1	M	Yes [ ]	Limit the current of I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104-3
PSE18	PSE enabled while not in POWER_ON state	104.3.6.2.1	M	Yes [ ]	Limit I_{Port} to less than I_{SC} as specified in Table 104-2 for a duration of up to T_{LIM}
PSE19	Begin power removal from the PI within T_{LIM}	104.3.6.2.1	M	Yes [ ]	When limiting current in the POWER_UP state, POWER_ON state, or any state when V_{Sleep} is applied at the PI
PSE20	Measuring I_{Port} during short circuit	104.3.6.2.1	M	Yes [ ]	To be made 1ms after the initial transient to allow for settling
PSE21	PD wakeup request valid while in SLEEP state	104.3.6.2.2	M	Yes [ ]	If I_{port} is in the valid range of I_{wakeup} for a minimum of T_{wakeup}
PSE22	PD wakeup request invalid while in SLEEP state	104.3.6.2.2	M	Yes [ ]	If I_{port} is greater than $I_{wakeup\_bad\_hi}$ or less than $I_{wakeup\_bad\_lo}$
PSE23	Enter POWER_ON state	104.3.6.4	M	Yes [ ]	If full operating voltage is applied within T_{inrush}min
PSE24	Full operating voltage not applied within T_{inrush}max	104.3.6.4	M	Yes [ ]	New detection cycle initiated after a delay of $T_{restart}$ before any subsequent application of full operating voltage
PSE25	V_{PSE} to V_{Sleep} discharge time while in POWER_ON state	104.3.6.5	M	Yes [ ]	Defined as T_{Off} in Table 104-3
PSE26	P_{Class}	104.3.6.6	M	Yes [ ]	As defined in Table 104-1
PSE27	Measurement of P_{Class}	104.3.6.6	M	Yes [ ]	Averaged from uniform sliding window of 1 second wide
PSE28	Normal Operating voltage removal while in POWER_ON state	104.3.7	M	Yes [ ]	In absence of PD Maintain Full Voltage Signature
PSE29	MFVS present	104.3.7.1	M	Yes [ ]	If I_{Port} is greater than or equal to I_{Hold} max for a minimum of T_{MFVS}
PSE30	MFVS absent	104.3.7.1	M	Yes [ ]	If I_{Port} is less than or equal to I_{Hold} min
PSE31	MFVS absent for duration greater than TMFVDO	104.3.7.1	M	Yes [ ]	Reduce voltage at the PI to the range of V_{Sleep}

0.0.0.3 Powered Device (PD)

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Voltage and power requirements	104.4.2	M	Yes [ ]	As defined in Table 104-1 for each relevant system class
PD2	PD behavior	104.4.3	M	Yes [ ]	In accordance with state diagram shown in Figure 104-6
PD3	Present valid detection signature	104.4.4	M	Yes [ ]	When V_{PD} drops below V_{sig_enable}
PD4	Removal of current draw of detection signature	104.4.4	M	Yes [ ]	When V_{PD} rises through $V_{sig\_disable}$
PD5	PD detection signature	104.4.4	M	Yes [ ]	To consist of a current limited, constant voltage as specified in Table 104-4 when measured by the PSE
PD6	Valid detection signature	104.4.4	M	Yes [ ]	In accordance with the characteristics shown in Table 104-4
PD7	Non-valid detection signature	104.4.4	M	Yes [ ]	In accordance with at least one of the characteristics shown in Table 104-5
PD8	PD power	104.4.6	M	Yes [ ]	In accordance with the characteristics shown in Table 104-6
PD9	Turn on voltage	104.4.6.1	M	Yes [ ]	In the range of V_{On} after a delay greater than t_{power_dly} as specified in Table 104-6
PD10	Turn off voltage	104.4.6.1	M	Yes [ ]	Greater than or equal to V_{Off} as specified in Table 104-6
PD11	PD turn on or off	104.4.6.1	M	Yes [ ]	Without startup oscillation and within the first trial when fed by V_{Port_PSE}min to V_{Port_PSE}max with a series resistance within the range of valid channel resistance
PD12	PD_SLEEP state input voltage	104.4.6.1	M	Yes [ ]	Greater than V_{Sleep_PD} min as specified in Table 104-6
PD13	Input current while in DISCONNECT and PD_SLEEP states	104.4.6.2	M	Yes [ ]	Current drawn is not in excess of I_{Sleep_PD} as specified in Table 104-6
PD14	PD requiring detection and power-up	104.4.6.2	M	Yes [ ]	Draw current within range of I_{Wakeup_PD} for at least T_{Wakeup_PD} when V_{sleep_PD} min < V_{pd} < V_{sleep} max as specified in Tables 104-4 and Table 104-6
PD15	PD ripple and transients	104.4.6.3	M	Yes [ ]	In accordance with specifications shown in Table 104-6 for all operating voltages in the range of V_{Port_PD} and over the range of input power of the device

PD16	PSE ripple and transients	104.4.6.3	M	Yes [ ]	Operate in accordance to the levels specified in Table 104-3 in the presence of PSE ripple and transient voltages appearing at the PD PI
PD17	PD stability	104.4.6.5	M	Yes [ ]	When PD is fed voltage between V_{Port_PSE}min and V_{Port_PSE}max with R_{Loop_max} in series, P_{Port_PD} is defined by equation 104-1
PD18	PD Maintain Full Voltage	104.4.7	M	Yes [ ]	Provide valid Maintain Full Voltage Signature (MFVS) at the PI
PD19	PD MFVS current draw	104.4.7	M	Yes [ ]	Equal to or greater than I_{Hold_PD} for a minimum duration of T_{MFVS_PD} measured at the PD PI followed by an optional MFVS dropout for no longer than T_{MFVDO} min
PD20	No longer require full input operating voltage	104.4.7	M	Yes [ ]	Remove current draw of the MFVS from the PI

0.0.0.4 Common Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
COMEL1	PI output conductor pair fault tolerance	104.5.2	M	Yes [ ]	Meet the requirements of the appropriate specifying clause (See Clauses 96 and 97)
COMEL2	100BASE-T1 PoDL system MDI return loss	104.5.3.1	M	Yes [ ]	Meet or exceed Equation 104-2
COMEL3	1000BASE-TI PoDL system MDI return loss	104.5.3.1	M	Yes [ ]	Meet or exceed Equation 104-3

0.0.0.5 PSE Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
PSEEL1	PSE PI	104.5.2	M	Yes [ ]	Withstand the application of short circuits between the wires within the cable for an indefinite period of time without damage
PSEEL2	Short circuit current magnitude	104.5.2	M	Yes [ ]	Not to exceed I_{LIM}max as defined in Table 104-3 given an indefinite short circuit

0.0.0.6 PD Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
PDEL1	DC isolation	104.5.1	M	Yes [ ]	Provided between all accessible external conductors, including frame ground (if any), and all MDI leads

0.0.0.7 SCCP

Item	Feature	Subclause	Status	Support	Value/Comment
SCCP1	SCCP master	104.6.1	M	Yes [ ]	Source a pull-up current in order to drive the bus voltage high and meet the required electrical specifications for SCCP
SCCP2	SCCP communication	104.6.3.1	M	Yes [ ]	Begins with an initialization sequence consisting of a result pulse from the master followed by a presence pulse from the slave. See Figure 104-9
SCCP3	Initialization sequence	104.6.3.1	M	Yes [ ]	Master transmits a reset pulse by first pulling the PI port voltage low and then pull-up within t_{RSTL} before going into receive mode (RX)

SCCP4	Slave presence pulse Double check this	104.6.3.1	M	Yes [ ]	Transmitted after detecting rising edge at PD PI and waiting t_{PDHI}
SCCP5	Sample subsequent voltage	104.6.3.1	M	Yes [ ]	Within t_{MSP} from the completion of the preceding rising-edge at its PI
SCCP6	Master write time slots	104.6.3.2	M	Yes [ ]	Write 1 time slot to transmit logic 1 to slave and write 0 time slot to transmit logic 0 to slave
SCCP7	Write time slot duration	104.6.3.2	M	Yes [ ]	Defined as t_{SLOT} shown in Table 104-10
SCCP8	Write time slot initiation	104.6.3.2	M	Yes [ ]	Initiated by pulling PI port voltage low
SCCP9	Write 1 time slot generation	104.6.3.2	M	Yes [ ]	Write by pulling PI port voltage low then release and pull up its PI port voltage within t_{W1L}
SCCP10	Write 0 time slot generation	104.6.3.2	M	Yes [ ]	Write by pulling PI port voltage low then hold and then pull up its PI port voltage within t_{W0L}
SCCP11	Read time slot generation	104.6.3.3	M	Yes [ ]	Generated by the master immediately after issuing a function command which requires data from the slave
SCCP12	Read time slot duration	104.6.3.3	M	Yes [ ]	Defined as t_{SLOT} shown in Table 104-7
SCCP13	Read time slot initiation	104.6.3.3	M	Yes [ ]	Initiate by pulling PI port voltage low and then pulling up the PI port voltage within t_{W1L}
SCCP14	Slave transmit	104.6.3.3	M	Yes [ ]	Transmit a 1 or 0 at the slave PI after master initiates read time slot
SCCP15	Slave transmit 1	104.6.3.3	M	Yes [ ]	Leave PI port voltage high
SCCP16	Slave transmit 0	104.6.3.3	M	Yes [ ]	Pull PI port voltage low
SCCP17	Slave transmit 0 duration	104.6.3.3	M	Yes [ ]	While transmitting 0, hold the PI low , and then release its PI within t_{R0L}
SCCP18	Read time slot sample	104.6.3.3	M	Yes [ ]	Master releases PI and then samples subsequent voltage within t_{MSR} from the start of the read time slot
SCCP19	SCCP data and commands	104.6.4	M	Yes [ ]	Transmitted least significant bit first
SCCP20	Communication with slave	104.6.4.2	M	Yes [ ]	Begins with the initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the slave

SCCP21	SCCP-capable slaves	104.6.4.3	M	Yes [ ]	Support the Broadcast Address command
SCCP22	Issuing function command	104.6.4.3	M	Yes [ ]	Only after issuing an appropriate address command
SCCP23	Broadcast address command use	104.6.4.3.1	M	Yes [ ]	By the master to address a slave device on the bus without sending out unique address code information
SCCP24	8-bit Read Scratchpad command	104.6.4.4	M	Yes [ ]	Supported by all SCCP-enabled slaves
SCCP25	Reception of Read Scratchpad function command	104.6.4.4	M	Yes [ ]	Slave shall respond with a 16-bit CLASS_TYPE_INFO read payload followed by an 8-bit CRC8 field
SCCP26	CRC8 calculation	104.6.4.5	M	Yes [ ]	Produces the same result as the serial implementation shown in Figure 104-13
SCCP27	Shift register	104.6.4.5	M	Yes [ ]	Initialized to the value 0x00 before CRC8 calculation begins