PoDL Detection and Classification Presentation

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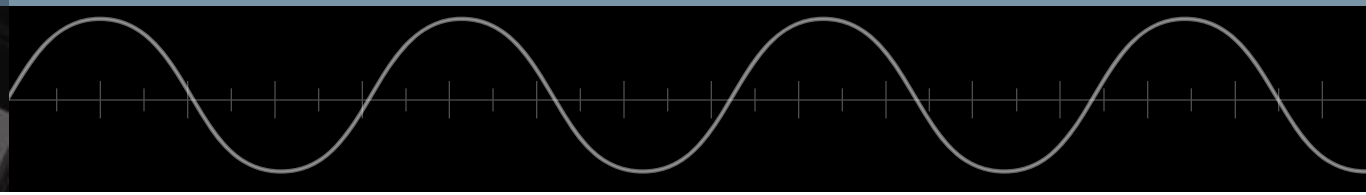


LINEAR TECHNOLOGY

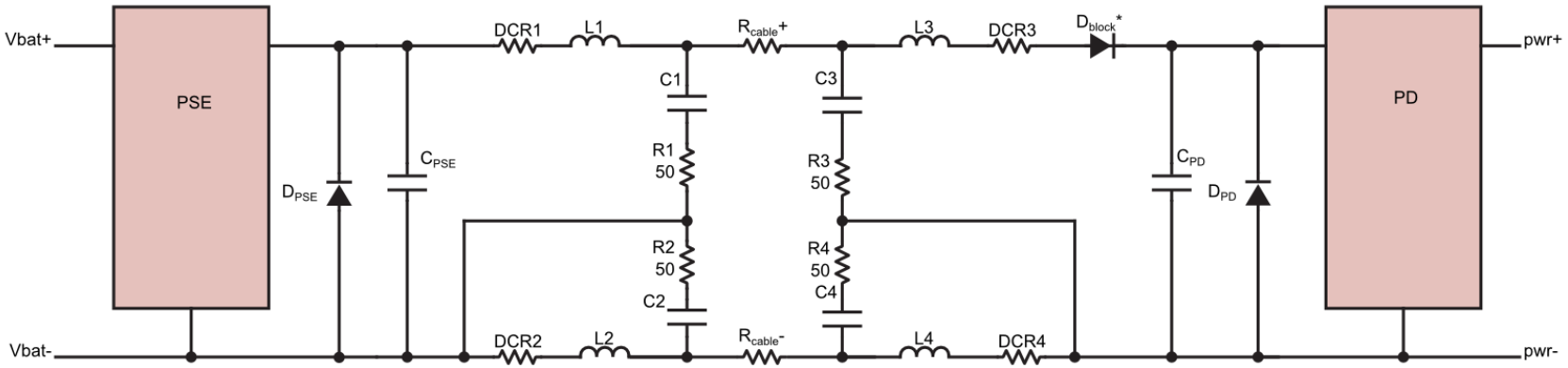
Presentation Objectives

- Review the requirements for PoDL detection and classification.
- Review the detection and classification scheme for PoE.
- Propose a new detection and classification scheme for PoDL.
- Propose a scheme for measuring parasitic resistance between the PSE and PD during detection.

Detection and Classification Considerations for PoDL

- Both PD voltage and current information need to be encoded in the class info, e.g.
  - V_{PD} = {5V, 12V, 48V} and I_{PD} = {0.5A, 1A, 2A, 5A, 10 A} have been proposed.
- A means for detecting parasitic resistance between the PSE and PD during detection may also be required/desired.
- The detection and classification scheme should be easily extendable and straight forward to implement.
- Start-up latency requirement may present a significant time constraint.
  - An abbreviated detection scheme that just checks for open and short circuit conditions may be required.
  - Classification may be performed once or on demand with the subsequent PD info being stored in system NVM.

PoDL Network from PSE/PD Perspective



* - Optional reverse polarity blocking diode

- Decoupling network inductors L1-L4 value is a function of the PHY T_{droop} specification:

$$L \geq \frac{-50ohms \times t_{droop}}{\ln\left(1 - \frac{v_{droop}}{v_{peak}}\right)}$$

- PHY DC blocking capacitors C1-C4 are chosen to yield an adequately damped response:

$$C \geq -\zeta^2 \frac{4 \times t_{droop}}{50ohms \times \ln\left(1 - \frac{v_{droop}}{v_{peak}}\right)} \quad where\ \zeta\ is\ the\ desired\ damping\ ratio$$

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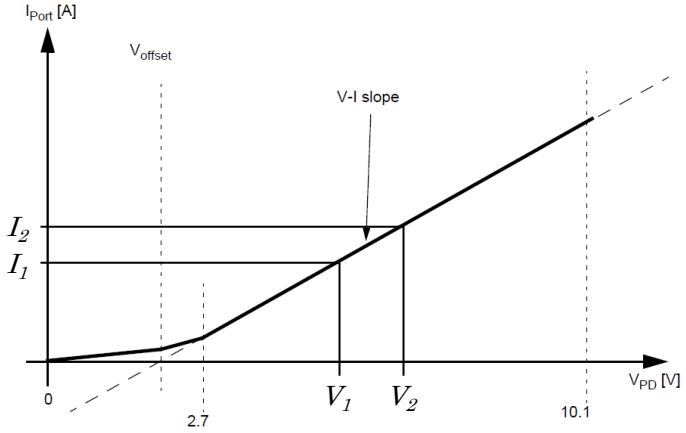
PoE Detection and Classification Scheme Recap

- The POE detection scheme looks for ~25kΩ signature resistance over a PD voltage chord > 1V in the range of 2.7V to 10.1V.



$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega}$$

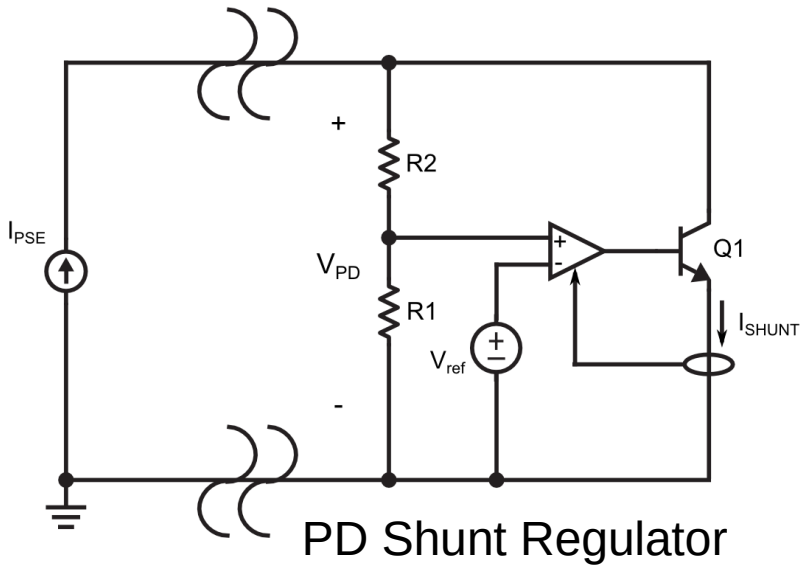
- The subsequent classification scheme entails the PSE forcing a voltage between 14.5V and 20.5V while detecting the resulting current one or more times in order to determine the PD power requirement.

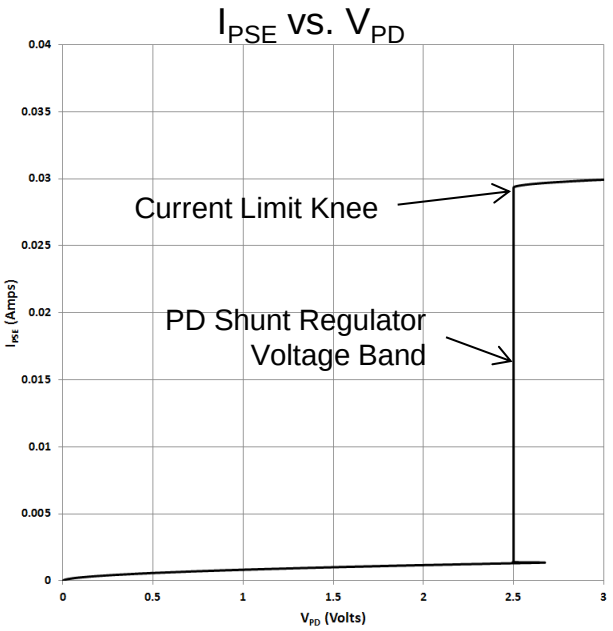
New Constraints on PoDL Detection and Class Scheme

- PoDL Detection and Class has significantly less voltage headroom to work with (<5V?) .
- Detect and Class may need to complete in <10ms for some applications.
- Parasitic resistance between the PSE and PD may need to be measured during detection prior to powering the PD load.

A New Approach to Detection and Classification for PoDL?

- The PSE may force current and sense one or more current limited voltages being shunt regulated by PD during detection and classification.
- Signature and class information may be encoded by PD shunt regulator voltage(s) (as opposed to PD current).





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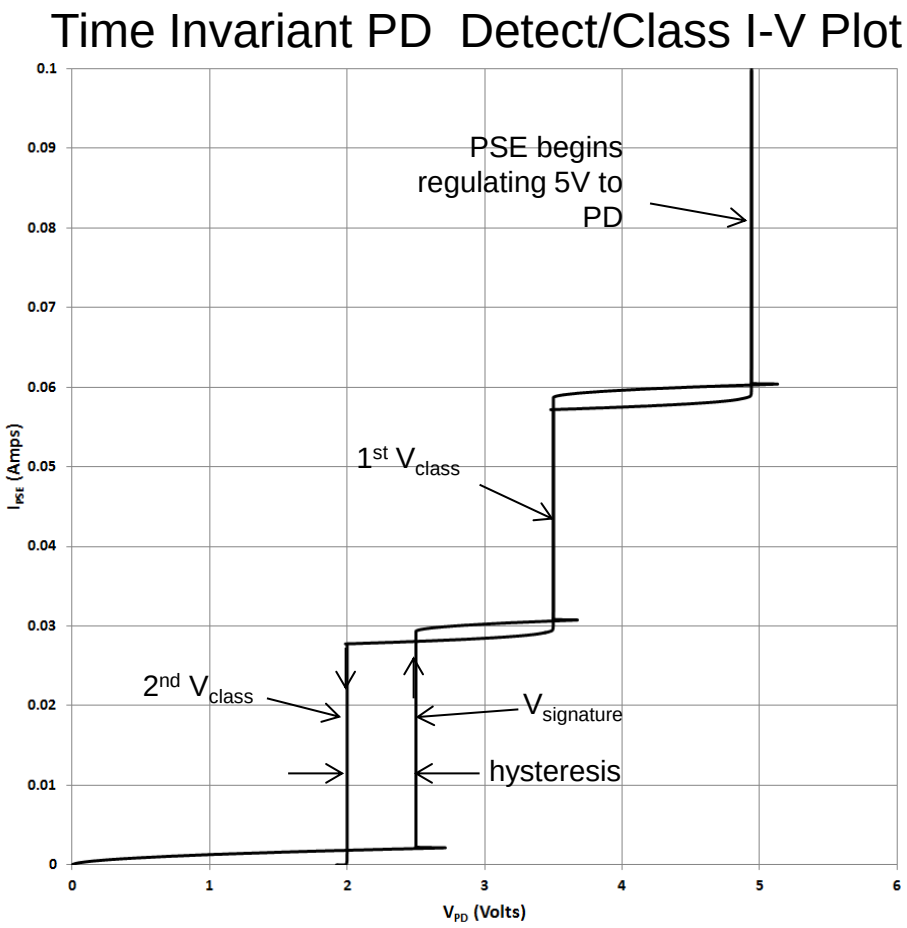
Time Invariant PoDL Detection and Classification Scenario

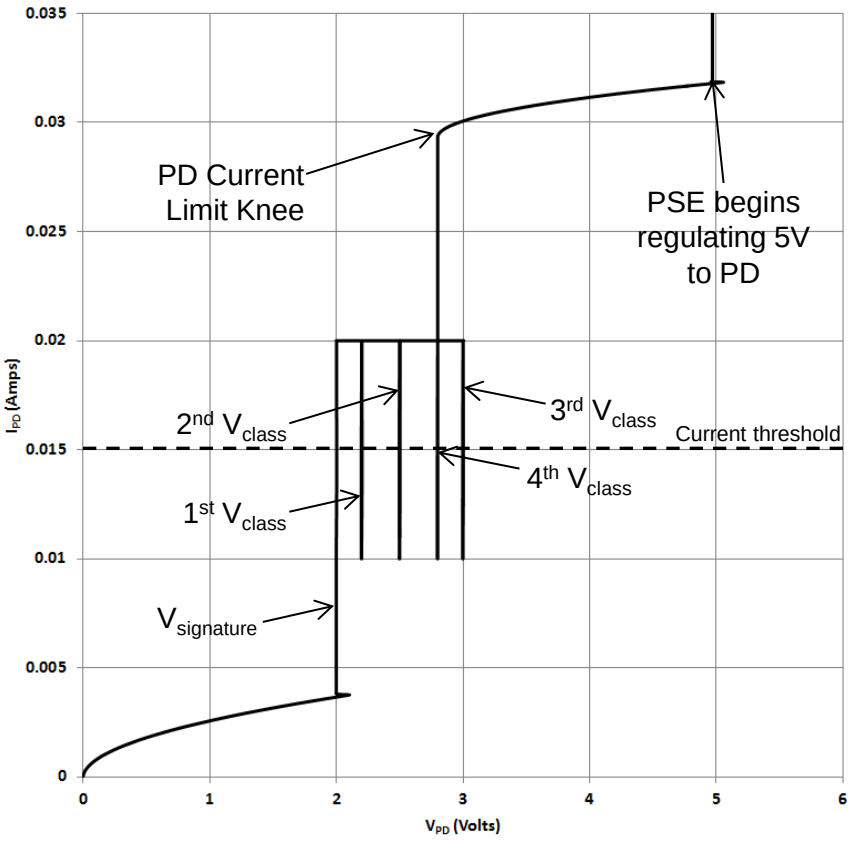
- A time-invariant PD always yields the same I-V plot on a curve tracer in response to an alternating I_{PSE} sweep.
  - The PD may exhibit hysteresis.
- The first or lowest voltage may encode the PD signature.
- Additional higher regulator voltages may be used to encode class information.
  - Voltage deltas may also be used to encode class information.
- Hysteresis may be used to encode additional information for the same PSE current.



Time Variant PoDL Detection and Classification Scenario

- The PD's shunt regulated voltage may change in a non-repetitive way in response to an alternating PSE current about a predetermined threshold.
- The first voltage may encode the PD signature.
- Subsequent PD voltages may be used to encode class information.
  - Voltage deltas may also encode class information.
- The sequence may stop after a predetermined number of cycles, or the PSE may overdrive the PD in order to end the sequence.

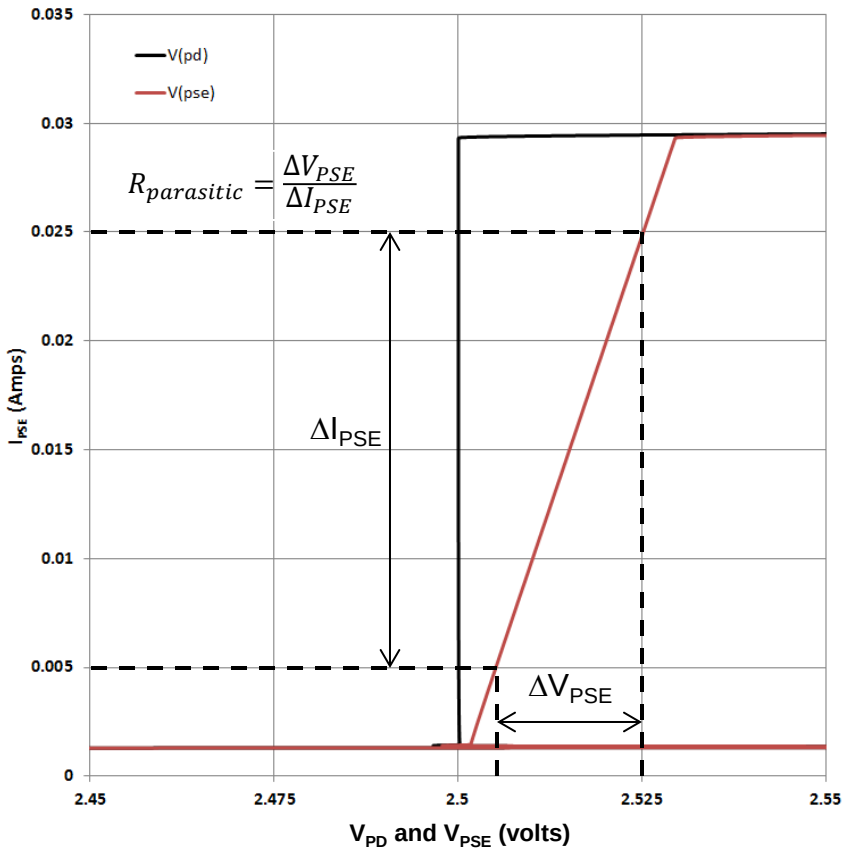
Time Variant PD Detect/Class I-V Plot



Sensing Parasitic Resistance Between the PSE and PD

- Parasitic resistance between the PSE and PD may be sensed by varying the PSE current within a regulated voltage band and sensing the resulting change in V_{PSE}.
- The parasitic resistance information may be used to compensate the PSE voltage for cable drop as a function of the PD load current.

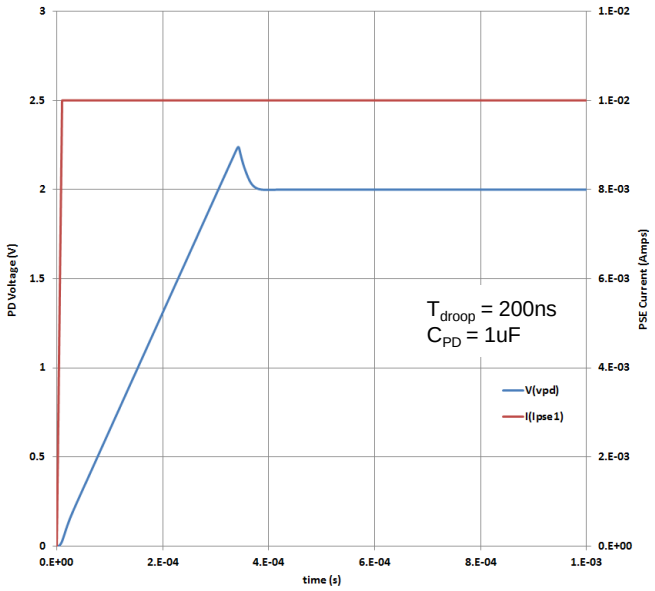
I_{PSE} vs. V_{PD} and V_{PSE}



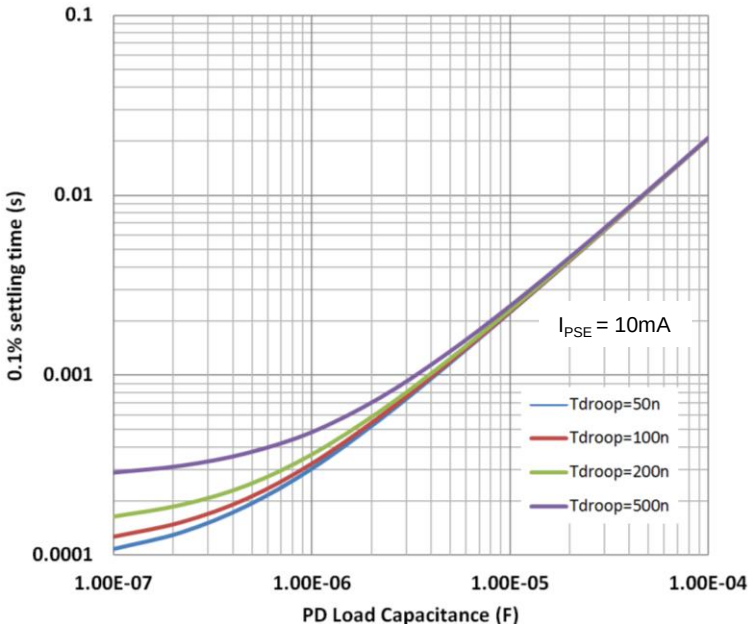
Settling Time Considerations

- PD regulator settling time is a function of capacitance downstream of the PSE and T_{droop}.
- Isolating large PD load capacitance from the PoDL network during detection and classification may be necessary for fast detection and classification.

PD Shunt Regulator Step Response



Settling Time into 2V PD Shunt vs. C_{PD}



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Summary

- Both voltage and current information need to be encoded in the PD signature for PoDL.
- A new detection and classification scheme for PoDL was presented.
- PD load capacitance may need to be isolated from the PoDL network during detection and classification in order to minimize settling times.