Sleep and Wakeup Proposal for PoDL

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Presentation Objectives

- Justify the need for a PoDL sleep and wakeup scheme.
- State requirements for sleep and wakeup.
- Describe a scheme for sleep and wakeup.
- Propose baseline text for sleep and wakeup.



Why Do We Need a Sleep and Wakeup Scheme for PoDL?

- When a link is sleeping, potential candidate Energy Efficient Ethernet (
 EEE) -T1 PHYs may only consume tens of micro-amps while retaining the capability to receive wakeup symbols from a link partner.
- PoDL PSE and PD quiescent currents should be comparable to the PHY quiescent current during sleep in order to be compatible.
- Implementing a MPS scheme compatible with micro-power EEE links may not be feasible without a sleep and wakeup scheme.
- Specifying a sleep and wakeup scheme may enable micropower sleep functionality for PoDL links even if the PHYs themselves do not support EEE!



Requirement for a Sleep and Wakeup Scheme

- Define states that will allow the PSE and PD to operate with very low quiescent current while the application is asleep.
- Define a MPS scheme that will reliably differentiate between a sleeping micro-power PD and a PD that no longer requires power.
- Define the conditions required for detecting sleep and wakeup events.
- Define a method for forwarding a wakeup request through the PSE.



PD Initiated Sleep and Wakeup Transitions

- When a PD enters sleep, the quiescent current transitions to a very low level.
 - I_{PD} drops below DC threshold current I_{Sleep} which marks the PD's transition to the SLEEP_PENDING state.
 - The PSE responds by transitioning to its SLEEP state and reducing V_{PI} to the range of V_{Sleep} where V_{Sleep} max is less than V_{Off}.
 - > When the PD detects $V_{PD} < V_{Off}$ it enters the SLEEP state.
- For wakeup the PD draws an elevated current in order to notify the PSE that it requires full power at the PI.
 - \succ I_{PD} increases current to the range of I_{Wakeup}.
 - The PSE detects I_{Wakeup} for greater than t_{Wakeup} and ramps-up the voltage at the PI to the full level.
 - The PD detects V_{PD}>V_{On} for greater than t_{powerdly} and goes to its fully powered state.



PD Initiated Sleep and Wakeup Transition Waveforms





Wakeup Forwarding and PSE Initiated Wakeup

- One example of wakeup forwarding occurs when the application needs to wakeup a link through the PSE.
- The PSE can wakeup a PD by simply exiting the SLEEP state and transitioning to the POWER_UP state.
 - When a sleeping PD detects $V_{PD} > V_{On}$, it waits $t_{powerdly}$ and powers-up.



PSE Wakeup Forwarding Waveforms





Existing & Proposed PSE State Diagrams



Existing & Proposed PD State Diagrams



Proposed (see Annex B for variables and timers)



MPS and the Sleep State

- In order to make MPS practical for micro-power applications, leverage the proposed SLEEP state:
 - > MPS monitoring is only required to be enabled during sleep.
 - PSE implementations will benefit from the restricted range of I_{Port} and ample voltage headroom between PSE input and output during sleep.



Existing and Proposed MPS State Diagrams

- The vsleep_valid variable indicates when the PSE is applying V_{Sleep} at the PI.
- MPS is not required to be active when the PSE applies full voltage at the PI.





Existing

Proposed



Proposed PSE Baseline Text for Sleep and Wakeup

104.3.6.1 Output voltage

The PSE shall apply a voltage at the PI in the V_{Sleep} range while operating in the SLEEP state (see Table 104-3).

A PSE operating in the SETTLE_SLEEP state shall discharge the PSE PI to the range of $\rm V_{\rm Sleep}.$

104.3.6.4 Output current

A PSE operating in the POWER_ON state shall consider a PD sleep request valid if I_{Port} averaged over a sliding window t_{Sleep} wide is less than or equal to I_{Sleep} min.

A PSE operating in the SLEEP state shall consider a PD wakeup request valid if I_{Port} is greater than I_{Wakeup} min for a minimum of t_{Wakeup} (see Table 104-3).



Proposed PD Baseline Text for Sleep and Wakeup

104.4.6.1 Input voltage

The PD shall operate in the SLEEP and WAKEUP states with an input voltage in the range of $V_{\text{Sleep PD}}$ as specified in Table 104-4.

104.4.6.5 Input current

During operation in the SLEEP_PENDING and SLEEP states, the PD shall draw current averaged over a sliding window t_{Sleep} seconds wide in the range of $I_{Sleep_{PD}}$ as specified in Table 104-6.

During operation in the WAKEUP state, the PD shall draw current in the range of $I_{Wakeup_{PD}}$ as specified in Table 104-6.



Proposed MPS Baseline Text for PSE

104.3.7 PSE power removal

Power shall be removed from the PSE PI in the absence of the PD Maintain Power Signature while the PSE is operating in the SLEEP state.

104.3.7.1 PSE Maintain Power Signature Requirements

A PSE shall consider the MPS to be present if I_{Port} averaged over a sliding window T_{MPS} wide is greater than or equal to I_{Hold} max. A PSE may consider the MPS to be either present or absent if I_{Port} averaged over a sliding window T_{MPS} wide is in the range of I_{Hold} .

A PSE shall consider MPS to be absent if I_{Port} averaged over a sliding window T_{MPS} wide is less than or equal to I_{Hold} min. Power shall be removed from the PI when the MPS has been absent for a duration greater than T_{MPDO} .



Proposed MPS Baseline Text for PD

104.4.7 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall draw current averaged over a sliding window T_{MPS} wide equal to or above $I_{Hold_PD(min)}$. A PD that does not maintain the MPS may have its power removed within the limits of T_{MPDO} as specified in Table 104–3. PDs that no longer require power shall remove the current draw of the MPS



Proposed PSE Output Requirements for Table 104-3

ltem	Parameter	Symbol	Unit	Min	Max	Class	Туре	Additional Information	
1a	DC output voltage during	V_{Sleep}	V	4	V _{off(max)}	(12V CC)		See 104.3.6.1	
1b				4	V _{off(max)}	(12V)			
1c				4	V _{off(max)}	(24V)			
1d				4	V _{off(max)}	(48V)			
ł		1	ł	ł	ł		ł		
13	PD MPS dropout time limit	T _{MPDO}	S	0.3	0.4			See 104.3.7.1	
14	PD Maintain Power Signature time for Validity	T _{MPS}	ms	90	110			See 104.3.7.1	
15	MPS current	I _{Hold}	μA	5	15			See 104.3.7.1	
16	Sleep current threshold	I _{Sleep}	mA	TBD				See 104.3.6.4	
17	Sleep current threshold sliding window	t _{Sleep}	ms	90	110			See 104.3.6.4	
18	Wakeup current threshold	I _{Wakeup}	mA		TBD			See 104.3.6.5	
19	Wakeup current hold time for validity	t _{Wakeup}	ms	1				See 104.3.6.5	



Proposed PD Power Supply Requirements for Table 104-6

ltem	Parameter	Symbol	Unit	Min	Мах	Class	Туре	Additional Information	
8a	Power supply voltage during SLEEP state	ver supply V _{Sleep_PD} age during EP state	V	3.9	V _{off(max)}	(12V CC)		See 104.4.6.1	
				3.9	V _{off(max)}	(12V)			
8b				3.9	V _{off(max)}	(24V)			
8c				3.9	V _{off(max)}	(48V)			
9	Sleep Current	I _{sleep_PD}	μA		100			See 104.4.6.5	
10	Wakeup Current	I _{wakeup_PD}	mA	3	10			See 104.4.6.5	



Conclusion

- Micro-power Energy Efficient Ethernet (EEE) applications need to be considered as part of the PoDL standard.
- Requirements for compatibility with micro-power EEE were reviewed.
- A sleep and wakeup scheme and a modified MPS scheme compatible with micro-power EEE were presented.
- Proposed changes to baseline text and tables for sleep, wakeup, and revised MPS are relatively minor; changes to the state diagrams are more extensive.



Questions?

LINEAR TECHNOLOGY

Annex A – PSE State Diagram Variables

Variable Name	Definition
do_classification_done	A Boolean variable indicating that the PSE has terminated serial communication after performing a read of the PD information byte and any additional implementation dependent read or write commands.
do_detection_done	This Boolean variable indicates the status of the current START_DETECTION state detection cycle. If true, the current START_DETECTION detection cycle has completed. If false, the current START_DETECTION state detection cycle has not completed.
fault_detected	A Boolean variable indicating the PSE output current has been in an overcurrent condition for at least T _{CUT} . If TRUE, the PSE has encountered an overcurrent condition. If FALSE, the PSE has not detected an overcurrent condition.
good_sig	A Boolean variable that indicates the state of mr_valid_signature when detection is done. If true, mr_valid_signature is true. If false, mr_valid_signature is false.
I _{Port}	PSE output current as measured at the PI.
mr_mps_valid	This Boolean variable indicates the presence or absence of a valid MPS.
mr_pse_enable	A Boolean control variable that enables or disables PSE operation.
mr_sccp_enabled	A Boolean variable indicating whether the Serial Communication Classification Protocol (SCCP) is supported by the PSE. If true, SCCP is supported. If false, SCCP is not supported.
mr_valid_signature	This Boolean variable indicates the PSE has detected a valid signature.
pi_discharge_enable	This Boolean variable indicates if the PSE is discharging the PI to VSleep. See 104.3.6.4
pi_powered	A Boolean variable that controls the circuitry the PSE uses to power the PD. If false, the PSE shall not apply power to the PI (default). If true, the PSE shall apply power to the PI.
pi_sleeping	A Boolean variable that controls the circuitry the PSE uses to power the PD. If false, the PSE is not applying Vsleep to the PI (default). If true, the PSE is applying Vsleep to the PI.
power_applied	A Boolean variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp of voltage, is not in a current limiting mode. If false, the PSE is either not applying power or has begun applying power but is still in POWER_UP. If true, the PSE has begun steady state operation.
power_not_available	A Boolean variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification. If false, the PSE is able to source power to the attached PD. If true, the PSE is no longer able to source power to the attached PD.
pse_ready	A Boolean variable that is asserted in an implementation-dependent manner to probe the link segment. If true, the PSE is ready to probe the link segment. If false, the PSE is not ready to probe the link segment.
sleep_detected	A Boolean variable indicating that the average value of I _{Port} is less than or equal to the I _{Sleep} threshold current and that the PSE shall transition to the SLEEP state. See 104.3.6.4.
valid_class	A Boolean variable indicating that a valid class information byte was obtained from the PD during SCCP. If true then valid. If false then invalid.
vsleep_valid	A Boolean variable indicating that the PI was discharged to the range of Vsleep before exiting the SETTLE_SLEEP state. If TRUE, VPI is in the range of Vsleep. If FALSE, VPI is greater than Vsleep max.
wakeup_detected	A Boolean variable indicating that the PD is requesting full power at the PI or an external wakeup request has been received by the PSE and that the PSE shall forward the request to the PD. See 104.3.6.4.



Annex A cont'd – PSE State Diagram Timers

Timer Name	Definition
tclass_watchdog_timer	A timer used to limit the time in the START_CLASSIFICATION state in the event serial
	communication between the PSE and PD is stalled before the do_classification_done variable has been asserted by the PSE.
tdet_timer	A timer used to limit an attempt to detect a PD.
ted_timer	A timer used to regulate a subsequent attempt to power a PD after a error condition that causes a fault.
tinrush_timer	A timer used to monitor the duration of the inrush event.
tmpdo_timer	A timer used to monitor the dropout of MPS.
tpon_timer	A timer used to limit the time for power turn-on.
trestart_timer	A timer used to regulate a subsequent attempt to power a PD after an error condition that does not result in a fault.



Annex B – PD State Diagram Variables

Variable Name	Definition
disconnect	Boolean variable that indicates if a PD no longer requires
	power from the PI.
fault_detected	
	Boolean variable that indicates if a PD no longer requires power as the result of an error condition.
pd_sccp_enabled	been detected and SCCP serial transaction is pending.
POR	Boolean variable that indicates if the PSE in in power-on reset.
present_det_sig	Boolean variable that controls presenting the detection signature by the PD. If FALSE, a non-valid signature shall be presented. If TRUE, a valid signature shall be presented.
present_mps	This Boolean variable controls the application of MPS by the PD. If TRUE, the PD shall present a valid MPS current. If false, the PD shall present an invalid MPS current.
sccp_reset_pulse	Boolean variable that indicates if a SCCP reset pulse has been received by the PD. See 104.6.
sleep	Boolean variable that indicates if a PD has received a command to enter the SLEEP state.
V _{PD}	Voltage at the PD PI.
wake	Boolean variable that indicates if a PD has received a command to enter the WAKEUP state and request full power at the PI.



Annex B cont'd – PD State Diagram Timers

Timer Name	Definition
tpowerdly_timer	A timer used to prevent a PD from drawing more than inrush current during the PSE's MDI_POWER_DELAY state.
sccp_watchdog_tmr	A timer used to limit the time in the DO_CLASSIFICATION state in the event serial communication between the PSE and PD is idle or stalled.



Annex C: Updated Table 104-1-System and class power requirements matrix for PSE, PI, and PD

System Class										
(P _{PSE} -P _{PD})/P _{PSE}	I	I	II	II	II	III	III	IV	V	VI
20%	(12V CC)	(12V)	(12V CC)	(12V)	(24V)	(24V)	(48V)	(48V)	(48V)	(Open)
V _{PSE(max)} (V) ¹	18	18	18	18	28	28	56	56	56	-
V _{PSE(min)} (V) ¹	6	9	6	9	18	18	36	36	36	-
$R_{PSE}\left(\Omega ight)$	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-
I _{PI(max)} (A)	0.42	0.28	1.04	0.69	0.35	0.69	0.35	0.87	2.08	-
$R_{Loop(max)}\left(\Omega ight)^2$	2.9	6.5	1.2	2.6	10.4	5.2	20.7	8.3	3.5	-
V _{PD(min)}	4.8	7.2	4.8	7.2	14.4	14.4	28.8	28.8	28.8	-
P _{PSE} (W) ³	2.5	2.5	6.25	6.25	6.25	12.5	12.5	31.25	75	-
$P_{PD}\left(W\right)^4$	2	2	5	5	5	10	10	25	60	-

 $^{1}V_{PSE}$ is the no-load voltage measured at the PSE PI.

 ${}^{2}R_{Loop}$ is the round trip link segment resistance.

³P_{PSE} is the maximum power the PSE is required to source at the PI.

 ${}^{4}P_{PD}$ is the power available at the PD PI.



Straw Poll: I would support a motion to add a sleep and wakeup scheme into Clause 104

- Y:
- N:
- A:

