Power Classes for PoDL

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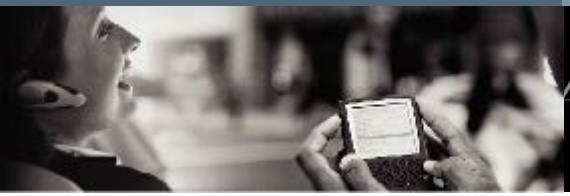
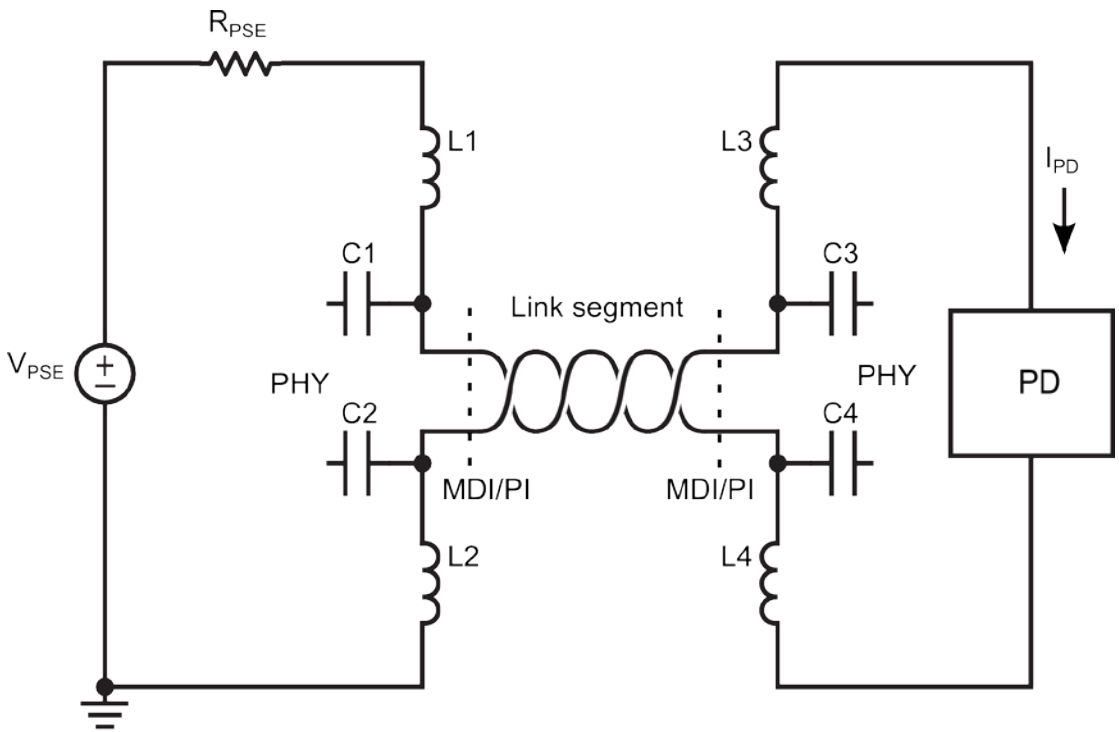


Presentation Objectives

- Review the underlying constraints regarding the delivery of power to a PD through a series resistance.
- Propose workable voltage and current limits for PoDL power classes.

Basic PoDL Circuit Architecture

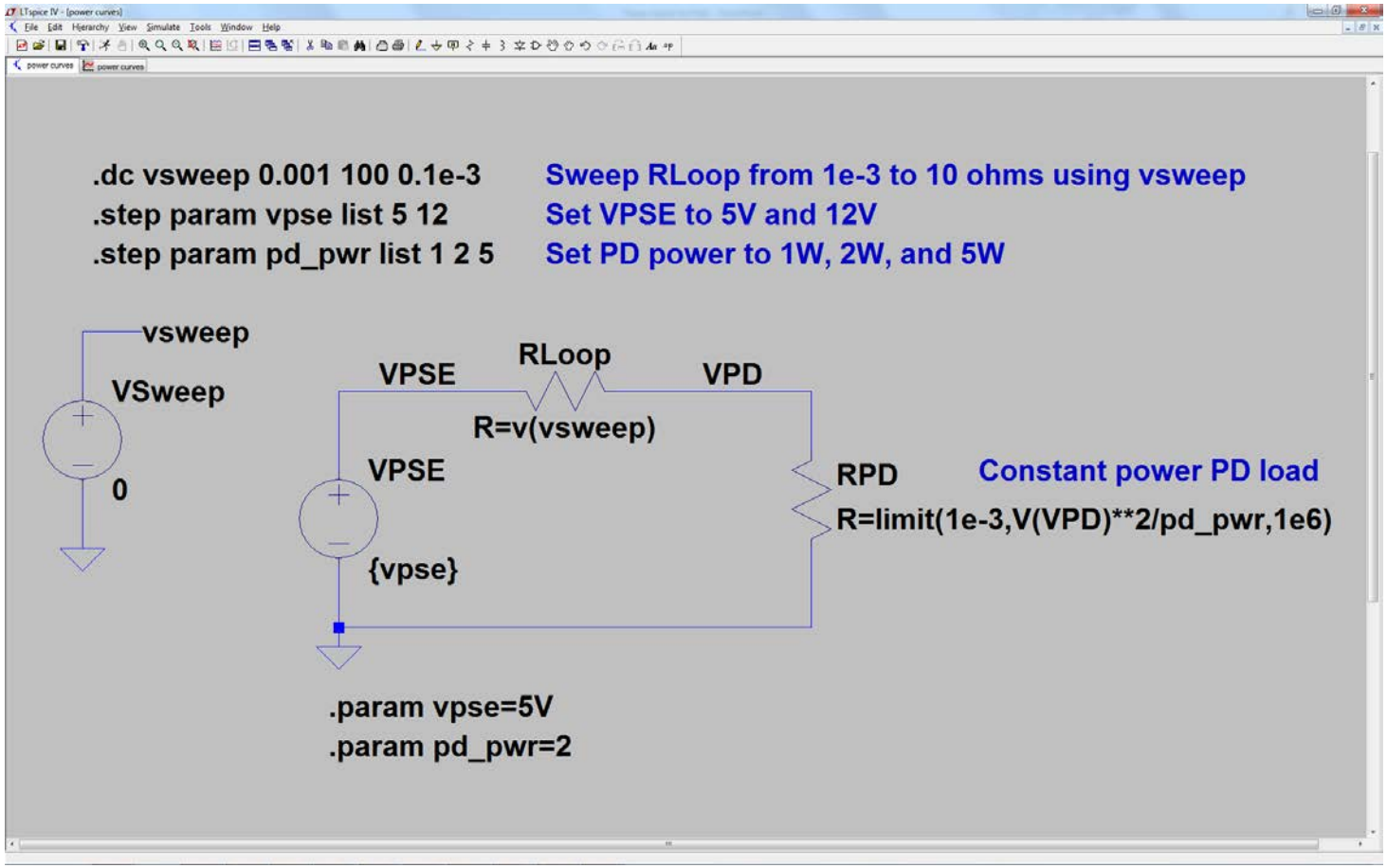


$R_{Loop}=R_{PSE}+R_{Link\_segment}$

What Constrains the Maximum Power that can be Delivered by the PSE to the PD?

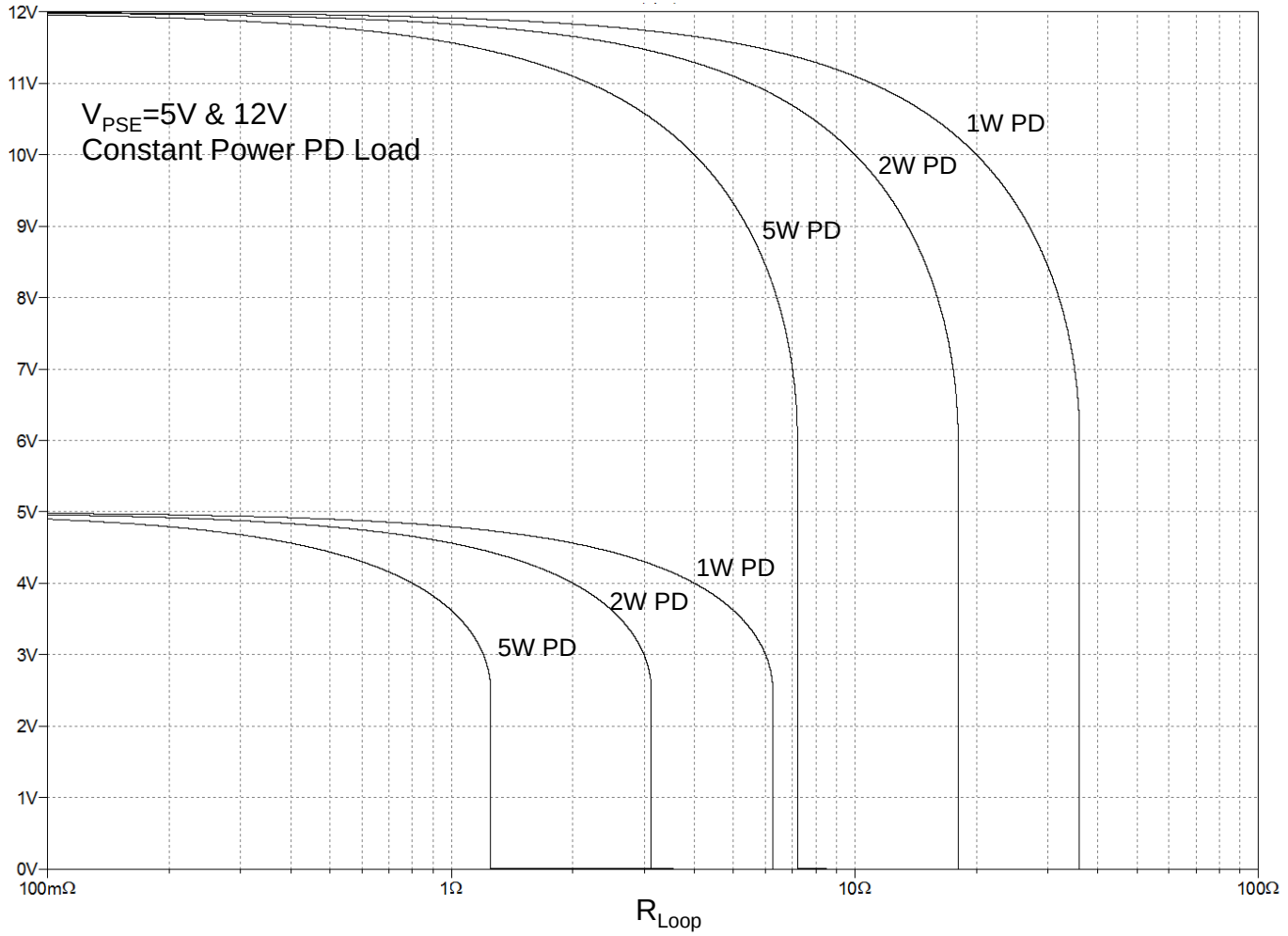
- PSE source voltage:
  - The higher the PSE source voltage (V_{PSE}) the higher the amount of power that can be delivered to the PD.
- PSE to PD loop resistance:
  - The higher the loop resistance, the lower the total amount of power that can be delivered to the PD.
  - For a given V_{PSE} and loop resistance (R_{Loop}), maximum PD power delivery occurs when 50% of V_{PSE} is dropped across R_{Loop}, i.e. $V_{PD}=V_{PSE}/2$.
- PSE/PD loop stability:
  - As a practical matter, a constant power PD requires that V_{PD} be significantly greater than 50% of V_{PSE} in order to ensure DC loop stability.

Simple Circuit Model for Analyzing DC Loop Stability*

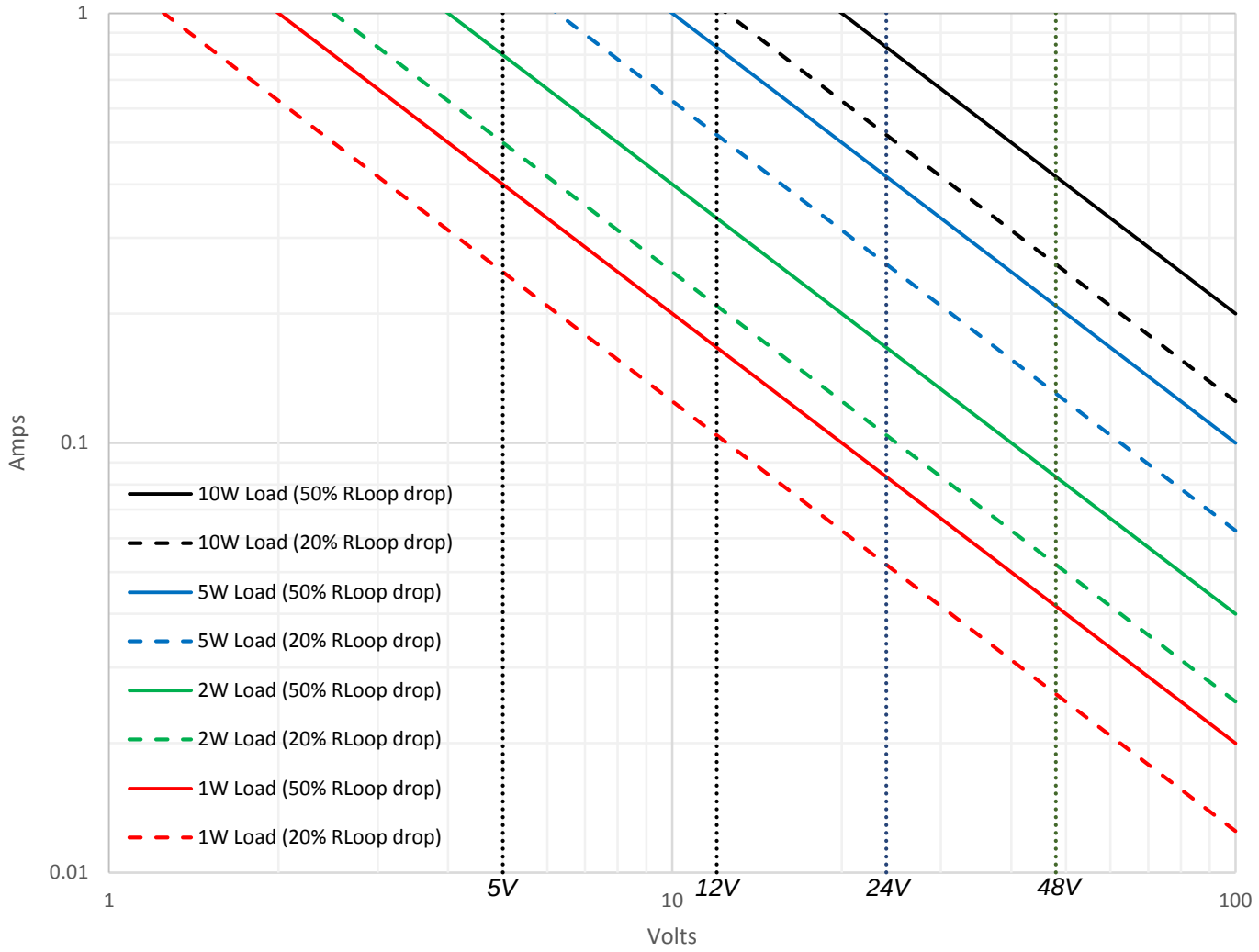


*See darshan_3bu_1_0914.pdf for detailed analysis of DC loop stability.

V_{PD} vs. R_{Loop} Curves from Simple Circuit Model



PI Current vs. V_{PSE} for P_{PD}=1W, 2W, 5W, & 10W



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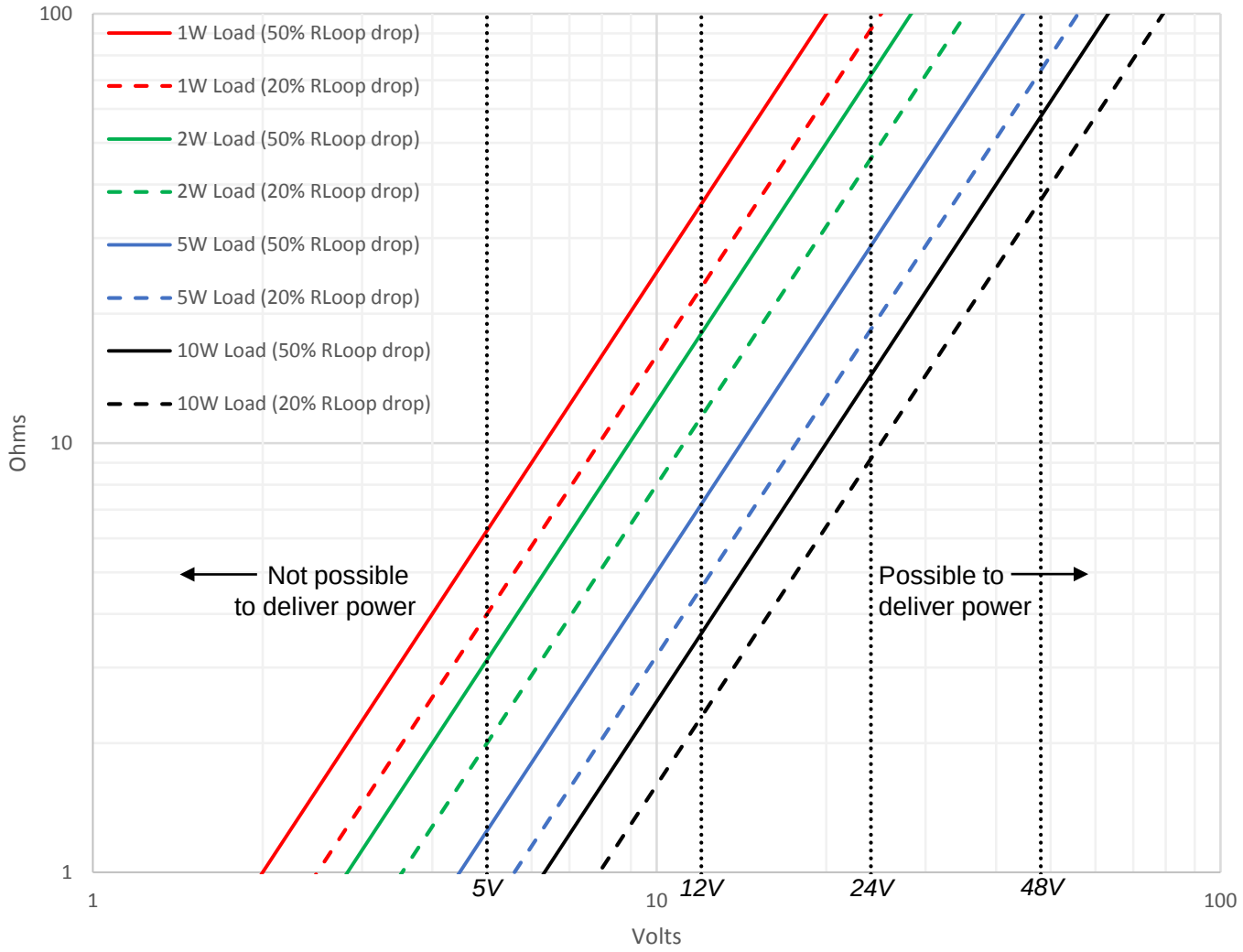
Maximum R_{Loop} vs. V_{PSE} for P_{PD}=1W, 2W, 5W, & 10W



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Example Load Scenario:

- V_{PSE}=10V, P_{PD}=5W, 15m of 26 AWG UTP @ 20°C, and 1Ω of PSE source resistance yields:
  - R_{Loop} = 15 × 2 × 0.14 Ω/m + 1 Ω = 5.2 Ω
  - Max R_{Loop} vs. V_{PSE} graph reveals that it is not possible to deliver 10W to the PD with this V_{PSE} and R_{Loop}!
- Increasing V_{PSE} to 14V for the above example yields:
  - 50% drop when R_{Loop} = 9.80 Ω
  - 20% drop when R_{Loop} = 6.27 Ω
  - I_{PI} = 0.714A for a 50% R_{Loop} drop*
  - I_{PI} = 0.446A for a 20% R_{Loop} drop*

*Coupling inductors' saturation current must be greater than I_{PI} to ensure data integrity.

Proposed Class Table

System Class									
R_{Loop} loss 20%	I (5V)	I (12V)	II (12V)	II (24V)	III (24V)	III (48V)	IV (48V)	V (48V)	VI (Open)
*$V_{PSE(max)}$ (V)	5.5	14	14	28	28	56	56	56	-
*$V_{PSE(min)}$ (V)	4.75	9	9	18	18	36	36	36	-
$I_{PI(max)}$ (A)	0.53	0.28	0.69	0.35	0.69	0.35	0.87	2.08	-
**$R_{Loop(max)}$ (Ω)	1.8	6.5	2.6	10.4	5.2	20.7	8.3	3.5	-
***$P_{PD(max)}$ (W)	2	2	5	5	10	10	25	60	-
****P_{PSE} (W)	2.5	2.5	6.25	6.25	12.5	12.5	31.25	75	-
$V_{PD(min)}$ (V)	3.8	7.2	7.2	14.4	14.4	28.8	28.8	28.8	-

*V_{PSE} is the open circuit voltage measured at the PSE PI.

**R_{Loop} is defined as the sum of the PSE source resistance and link segment round trip resistance.

***P_{PD} is measured at the PD PI.

****P_{PSE} does not include power dissipated by the PSE source resistance.

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Questions?

Motion

- Adopt the class table proposed in gardner_3bu_1_0315a.pdf.

  Y:

  N:

  A: