Detection and Class Fix

Andy Gardner

LINEAR TECHNOLOGY

Presentation Objectives

- To present a remedy that prevents a PD from being damaged when it is connected to an incompatible, non-classifying PSE.

Clause 96 and 97 Fault Tolerance Requirements

- 96.8.3 MDI fault tolerance states:
  - "The wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time."

Table 96–6—Connection fault

BI_DA+	BI_DA-
No fault	No fault
BI_DA-	BI_DA+
Ground	No fault
No fault	Ground
+50 V dc	No fault
No fault	+50 V dc
Ground	+50 V dc
+50 V dc	Ground

Proposed remedy for Clause 104

- Reduce the 48V Class maximum voltage in Table 104-1 from 60V to 50V and reduce the minimum voltage from 48V to 45V.
- Increase T_{od} min in Table 104-3 from 750ms to 10s in order to minimize the power dissipation in a PD when an incompatible PSE attempts to power it.
- Add the following to 104.6.2:

  PDs and PSEs shall withstand wire pair faults as specified in 96.8.3.

  A PD shall not be damaged when a Class 9 PSE attempts to power it.

Questions?