PoDL SCCP Revisions

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Presentation Objectives

- Revise SCCP timing diagrams and electrical requirements
  - Increase margin in Reset command
  - Fix overlapping timing in Read command
  - Add pullup current
  - Fix rise time to match pullup current
- Note
  - t_{RL} has a meaning in 1-Wire™ not compatible with SuggestedRemedy

Cl **104** *SC* **104.7.3.3** *P* **61** *L* **35** # 81

"Zimmerman, George" CME Consulting / LTC

Comment Type **TR** *Comment Status* **X**

"The master device shall initiate a read time slot by pulling VPSE low and then pulling-up VPSE within tW1L. This is exactly the same language as generating a Write 1 timeslot, making the read time slot and the write 1 timeslot not uniquely identifiable. Additionally, there is a timing problem, because according to this tW1L can be between 0.09 ms and 0.33 ms, while the master may sample anytime between 0.27ms and 0.33ms, meaning that if the slave hasn't recognized tW1L until near the end of its allowed duration, it won't have asserted data. The original spec seems to have had a separate tRL, which was slightly shorter than tW1L, and figure 104-15 shows the tW1L expiring before the tMSR. Recommend reinstating tRL as a shorter duration than tMSR min."

SuggestedRemedy

"Change ""tW1L"" to ""tRL"", both on P61 L35 and in Figure 104-15. Add tRL to Table 104-7, with a range of 0.09 ms to 0.25 ms (not exactly sure on the max time, but it has to be less than 0.27ms with some margin). Adjust PICS SCCP14 to reference tRL."

Proposed Response *Response Status* **O**

Modify Table 104-7 SCCP electrical requirements – Part 1

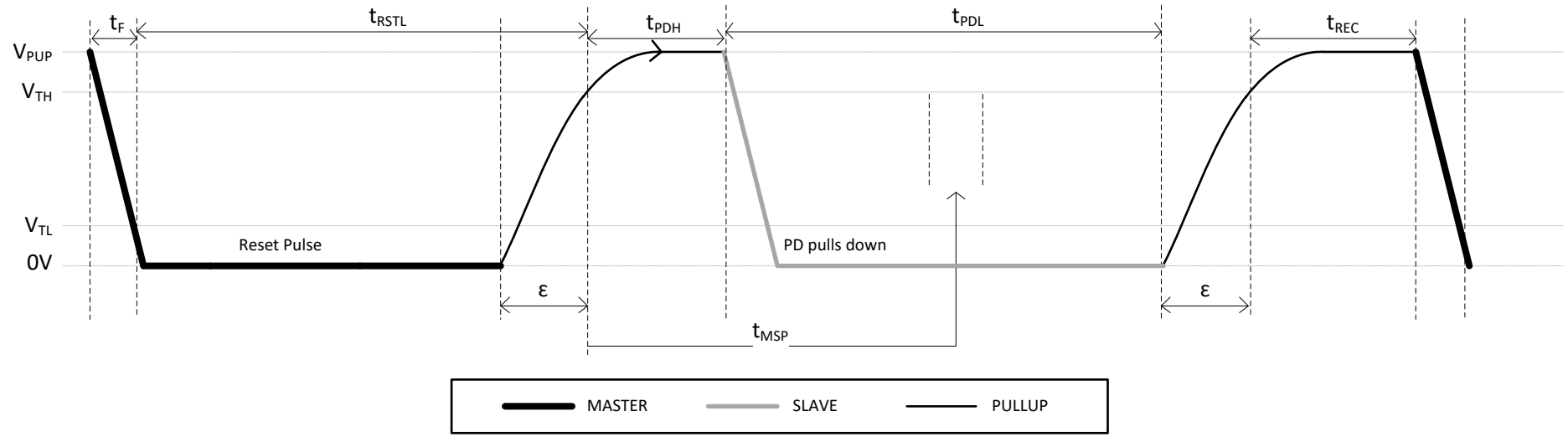
Item	Parameter	Symbol	Unit	Min	Max	
1	PSE Pullup Voltage	V_{PUP}	V	$V_{good\_PSE,max}$	5V	at $I_{probe,min}$
2	PSE Pullup Current	I_{PUP}	mA	9	16	
3	Input Logic High	V_{TH}	V	3	--	
4	Input Logic Low	V_{TL}	V	--	1	
5	Sink Current	I_L	mA	10		V_{PORT}>0.8V
6	Time Slot	t_{SLOT}	ms	2.7	3.3	
7	Recovery Time	t_{REC}	ms	0.27	0.33	
8	Write 0 Low Time	t_{W0L}	ms	1.8	2.2	
9	Write 1 Low Time	t_{W1L}	ms	~~90~~ 0.08	~~330~~ 0.25	
10	Slave Sample Write Time	t_{SSW}	ms	0.5	1.5	
11	Master Sample Read Time	t_{MSR}	ms	0.27	0.33	
12	Read 0 Low Time	t_{R0L}	ms	0.5	1.5	

Modify Table 104-7 SCCP electrical requirements – Part 2

Item	Parameter	Symbol	Unit	Min	Max	
13	Reset ~~Time~~ Low Time	t_{RSTL}	ms	9	11	
14	Presence-Detect High	t_{PDH}	ms	0.5	1.5	
15	Presence-Detect Low	t_{PDLOW}	ms	~~2~~ 2.5	~~6~~ 7.5	
16	Master Sample Presence Time	t_{MSP}	ms	~~1.6~~ 1.8	~~2.0~~ 2.2	
17	Rise Time	t_R	ms	0.025	0.105	
18	Fall Time	t_F	ms	0.025	0.1	
19	Bus Capacitance	C_{BUS}	ms	--	6	

Reset command timing proof

$t_{PDH,max} + t_{F,max} = t_{MSP,min}$

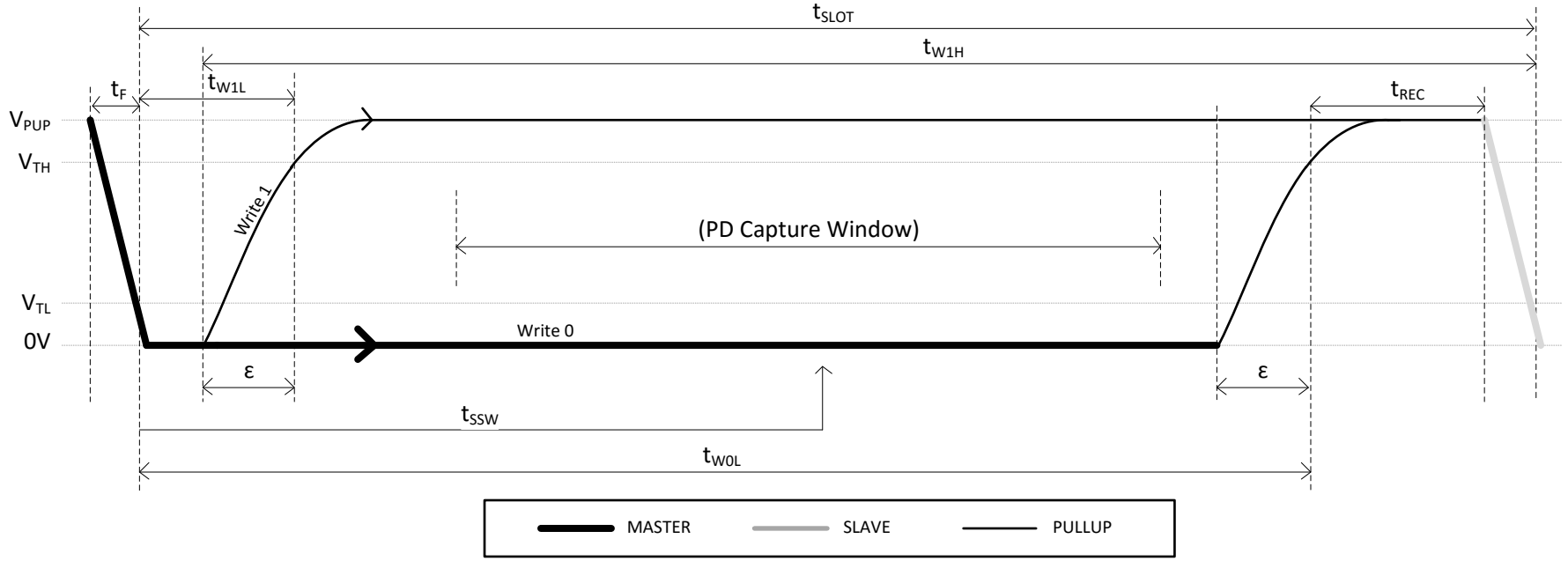


Symbol	Min	Typ	Max	Unit	Note
t_F	0		100	us	5V pu vs 100Ohm pd
ε		105	~~230~~	us	~~4mA PSE pu / 0.2uF C_{chan} to 4.6V~~ 9mA PSE pu / 0.2uF C_{chan} to 4.7V
t_{RSTL}	9	10	11	ms	PSE LO time for Reset pulse
t_{PDH}	0.5	1.0	1.5	ms	PD HI, measured from rising edge V_{TH}
t_{PDL}	~~2.0~~ 2.5	~~4.0~~ 5.0	~~6.0~~ 7.5	ms	PD LO, presence pulse, measured from rising edge V_{TH}
t_{MSP}	~~1.6~~ 1.8	~~1.8~~ 2.0	~~2.0~~ 2.2	ms	PSE presence capture, measured from rising edge V_{TH}
t_{REC}	270	300	330	us	Must charge PD SCCP reservoir capacitor
$t_{SLOT,RST}$			~~18.1~~ 20.6	ms	
t_{LO}			10	ms	PD must maintain state

Red indicates parameters captured in SCCP electrical requirements

No margin on t_{MPS}
Change
t_{PDL} to 2.5, 5, 7.5
t_{MSP} to 1.8, 2, 2.2
t_{SLOT} 20.6

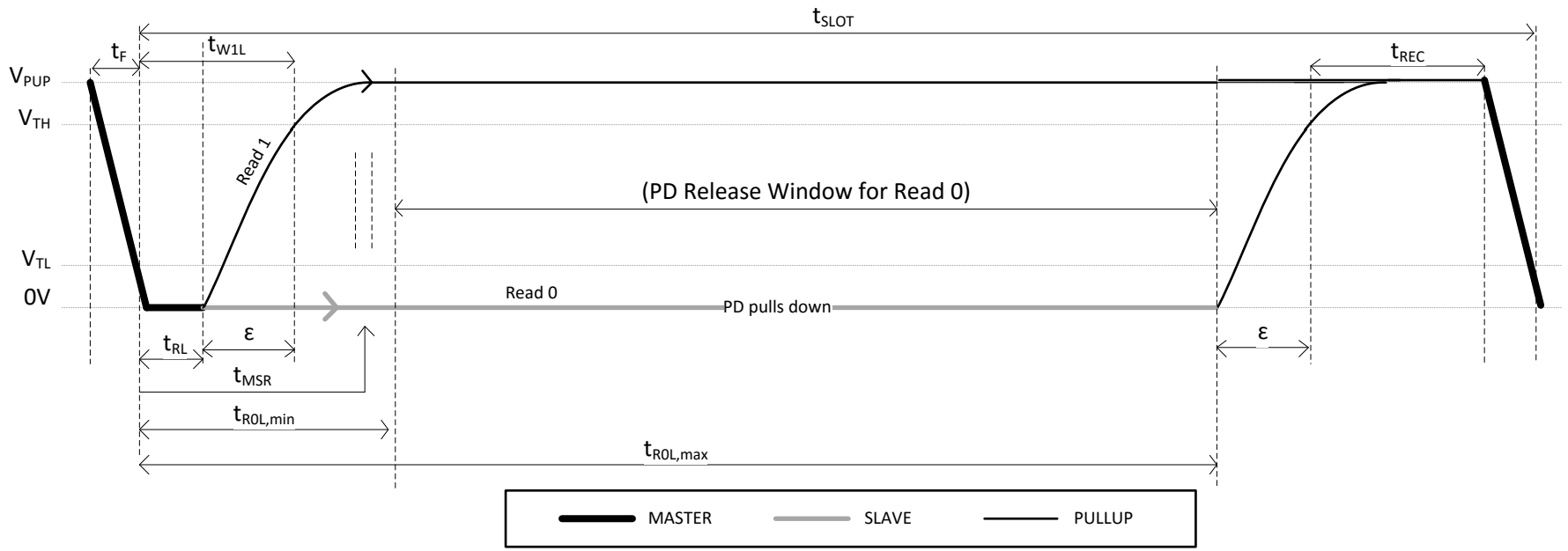
Write 0/1 slot timing proof



Symbol	Min	Typ	Max	Unit	Note
t_F	0		100	us	5V pu vs 100Ohm pd
ε			105 ~~230~~	us	~~4mA PSE pu / 0.2uF C_{chan} to 4.6V~~ 9mA PSE pu / 0.2uF C_{chan} to 4.7V
t_{W1L}	90		330	us	PSE LO time for Write 1 symbol
t_{W1H}	1.6	1.8	2.0	ms	PSE HI time for Write 1 symbol
t_{SSW}	0.5	1.0	1.5	ms	PD capture measured from falling edge V_{TL}
t_{W0L}	1.8	2.0	2.2	ms	PSE hold time for Write 0 symbol
t_{REC}	270	300	330	us	Charge PD SCCP reservoir capacitor
t_{SLOT}	2.7	3.0	3.3	us	

Red indicates parameters captured in SCCP electrical requirements

Read 0/1 slot timing proof



Symbol	Min	Typ	Max	Unit	Note
t_F	0		100	us	5V pu vs 100Ohm pd
ε	80	105	~~230~~	us	~~4mA PSE pu / 0.2uF C_{chan} to 4.6V~~ 9mA PSE pu / 0.2uF C_{chan} to 4.7V
t_{W1L}	~~90~~		~~330~~ 250	us	
t_{RL}		T_{W1L} - ε		us	
t_{MSR}	270	300	330	us	PSE capture, from falling edge V_{TL}
t_{R0L}	0.5	1.0	1.5	ms	PD release, measured from falling edge V_{TL}
t_{REC}	270	300	330	us	Must charge PD SCCP reservoir capacitor
t_{SLOT}	2.7	3.0	3.3	us	

Red indicates parameters captured in SCCP electrical requirements