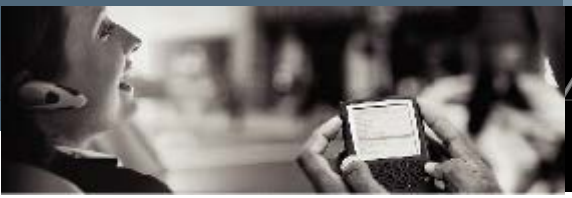
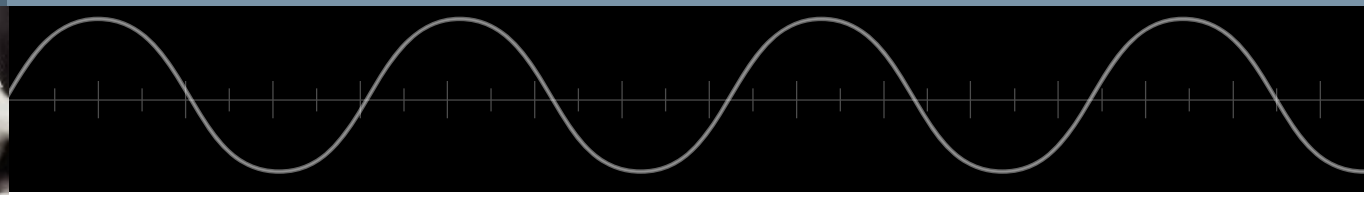
PoDL Wakeup Scheme Proposal

Andy Gardner

Linear Technology





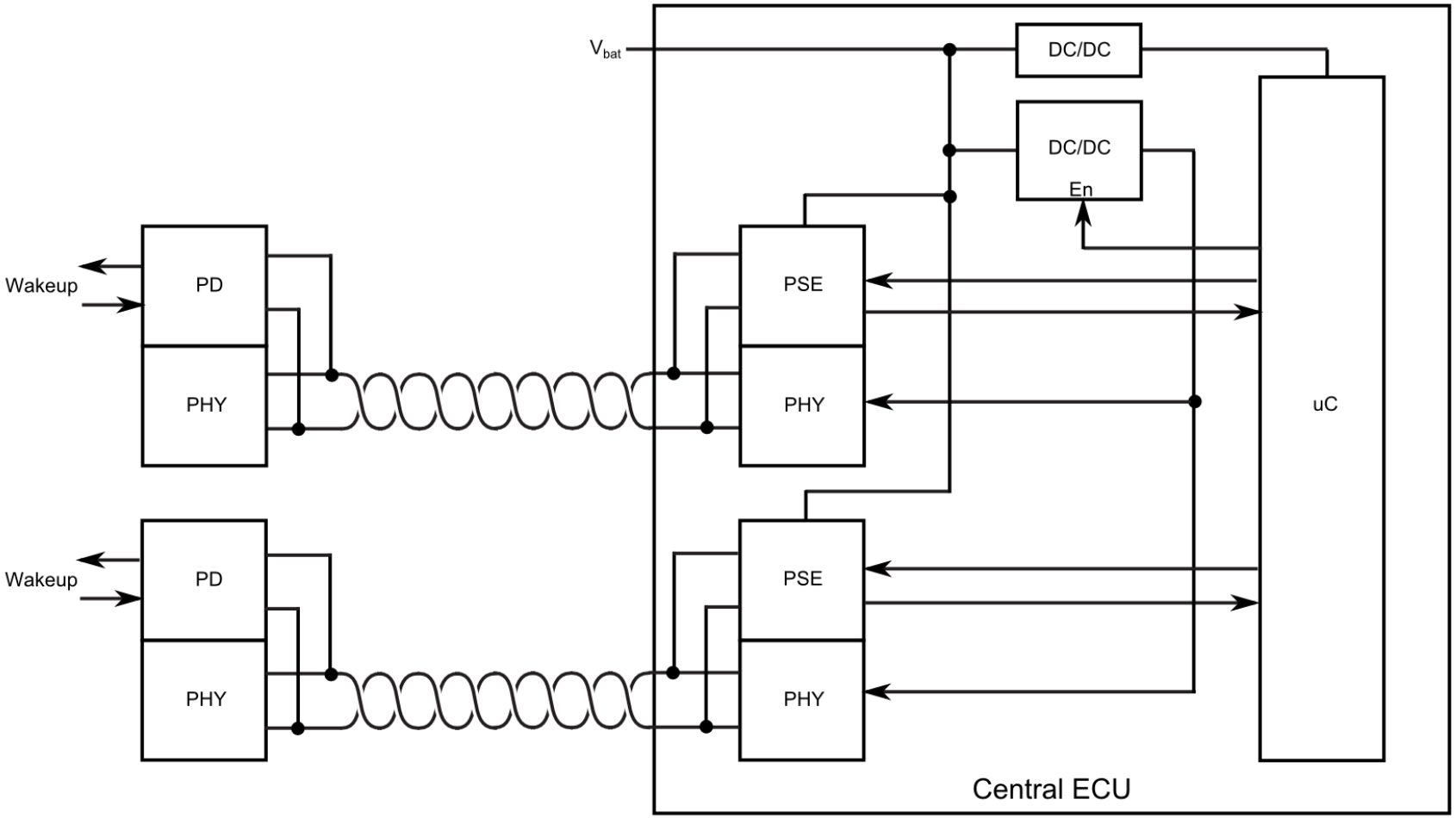
Presentation Objectives

- Review requirements for waking-up a sleeping link
- Present a use case for wakeup
- Present a wakeup scheme
- Discussion
- Straw poll

Requirements for Wakeup Scheme

- A very low power ECU state with wakeup capability is required.
  - ECU sleep state power consumption should be significantly less than 100µA.
  - PHYs may be disabled or unpowered while link is asleep.
- Link propagation delay for wakeup signals should be significantly less than the time required for fast power-up.
- Wakeup is initiated by simple dominant signals.
  - Link always wakes-up in response to a wakeup signal.
- Sleep is requested by simple recessive signals.
  - Link may only sleep when both PSE and PD request sleep.
- By definition, both ends of the link wake-up or sleep together.

Wakeup Use Case



Wakeup Use Case Assumptions

- Link may be asleep while PSE is applying power to the link.
- If no PSE power is present, PD must have auxiliary power source in order to wakeup the link.
- PSE may wakeup PD and vice versa.
- Wakeup forwarding is handled by a µC that is always powered.

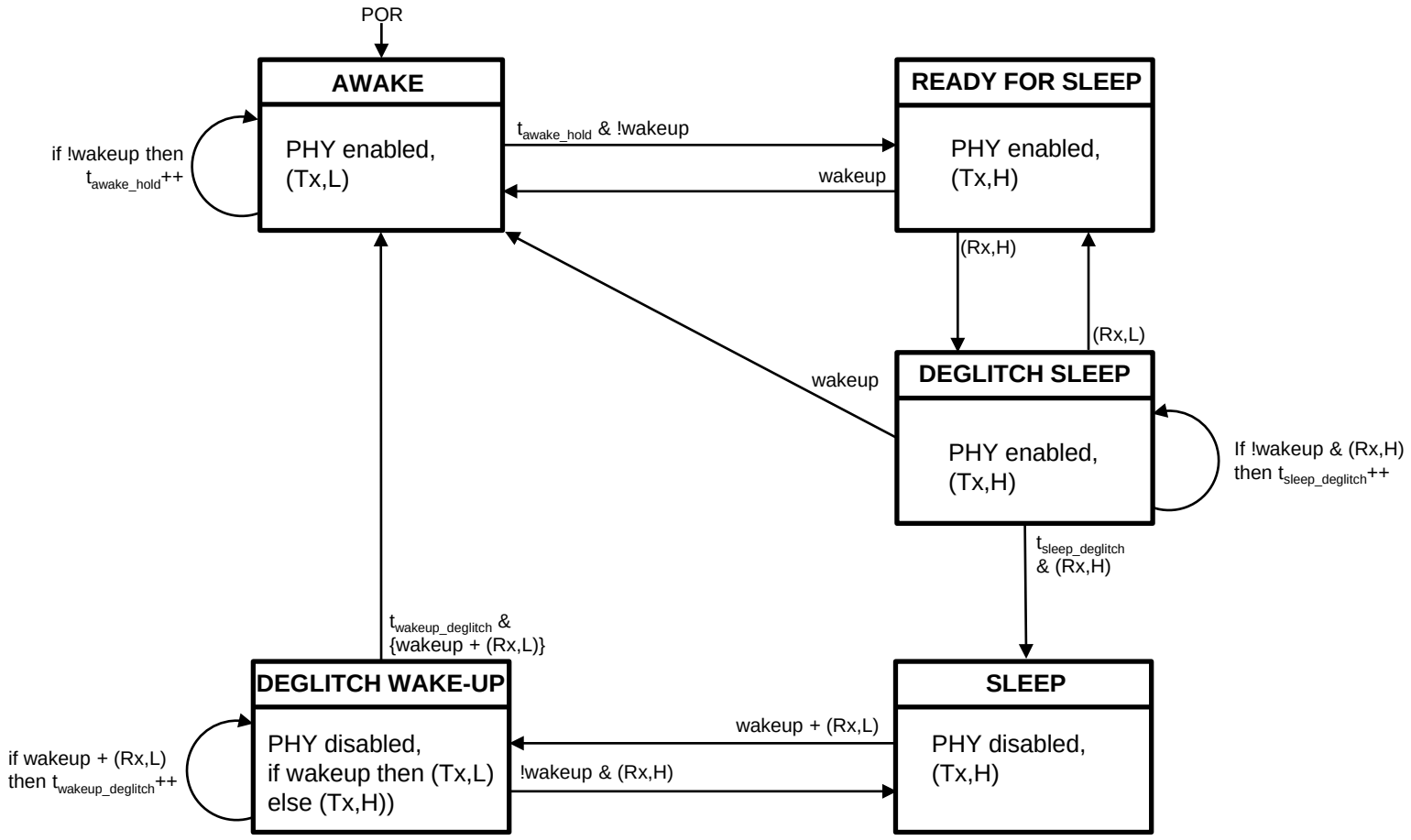
Wakeup Signals

PSE power at PI?	PD needs to wakeup the link	PSE needs to wakeup the link
Yes	PD draws current greater than I_{wakeup}	PSE discharges V_{PI} to less than the PD $V_{sig\_disable}$ and then re-asserts full voltage at V_{PI}; rising-edge initiates PD wakeup
No	PD cannot wakeup link without auxiliary power	PSE asserts full voltage at V_{PI} and rising-edge initiates PD wakeup
No (but PD has auxiliary power source)	PD applies voltage greater than TTL logic high voltage at its PI	

Sleep Signals

	PD ready to put link to sleep	PSE ready to put link to sleep
Ready-to-sleep event	PD reduces average current to less than I_{sleep}	PSE periodically pulses V_{PI} below $V_{off(max)}$ for at least $t_{sleep\_deglitch}$ but less than $t_{off(min)}$
Link partner response if not ready-to-sleep	PSE continues to deliver full voltage to PI	PD continues to consume current greater than I_{wakeup}
Link partner response if ready-to-sleep	PSE pulses V_{PI} below $V_{off(max)}$ for at least $t_{sleep\_deglitch}$	PD reduces average current to less than I_{sleep}

Wakeup State Diagram



(Tx,L) is a wakeup signal,
(Tx,H) is a sleep signal.

Questions?

Straw Poll

Who is in favor of adding a wake-up specification to the 802.3bu standard?

Y:

N:

A: