Review of Proposed Clause 96 Draft

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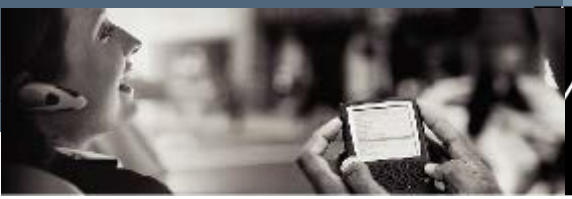
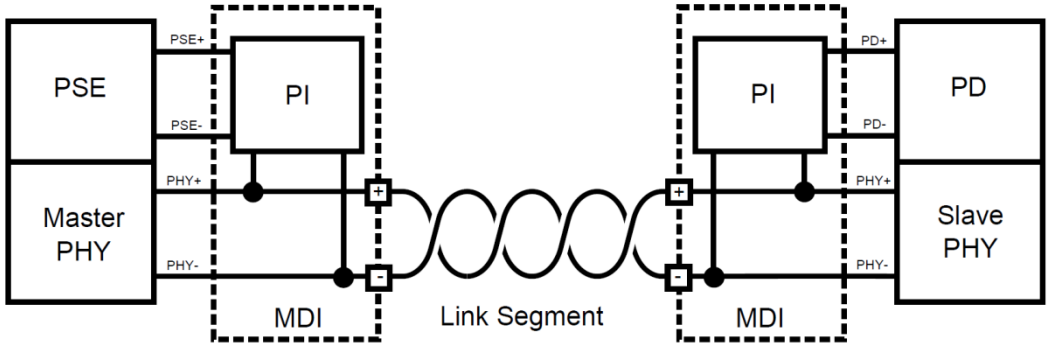


Presentation Objectives

- To review key concepts and terminology for the proposed Clause 96 draft.
- To review those portions of the proposed draft that still need to be addressed.

Partitioning of PoDL

- The PSE and PD as defined in the draft do **not** include the coupling networks
- Power interface (PI):
  - In PoE the PI was part of the MDI and simply referred to the connector terminals.
  - In PoDL the PI is still part of the MDI, but it now comprises both the coupling networks **and** the connectors, e.g. MagJack®.



PoDL System Types

- There are two system types:
  - Type 1 PoDL is compatible with 100BASE-T1 Ethernet
  - Type 2 PoDL is compatible with 1000BASE-T1 Ethernet
  - A type 1+2 PoDL is compatible with both 100BASE-T1 and 1000BASE-T1 Ethernet.
- The two types also apply to the PSE, PI, and PD.
  - The PIs (a.k.a. coupling networks) are constrained by the PHYs' droop, IL, and RL requirements.
  - PSE and PD transient and ripple noise are constrained by the PHYs' noise floor requirements referred back through the coupling networks.

PoDL Classes

- The scheme in buntz_3bu_01_0114.pdf has been adopted in the draft with the following changes:
  - 20% margin for losses in the cable and coupling networks has been added to the required PSE power levels.
  - The required PI current for a given class was based on assumptions about the minimum required PSE output voltage, e.g. 6V minimum for 12V V_{PSE} classes.

	System class									
	I (5V)	I (12V)	II (5V)	II (12V)	III (12V)	IV (12V)	IV (48V)	V (12V)	V (48V)	VI
Minimum required PSE output power (W)	2.4	2.4	6	6	12	30	30	72	72	*TBD*
Minimum required PSE output voltage (V)	4.5	6	4.5	6	6	6	24	6	24	*TBD*
Maximum required PI current (A)	0.6	0.4	1.4	1	2	5	1.3	12	3	*TBD*
Maximum allowed PD input power (W)	2	2	5	5	10	25	25	60	60	*TBD*

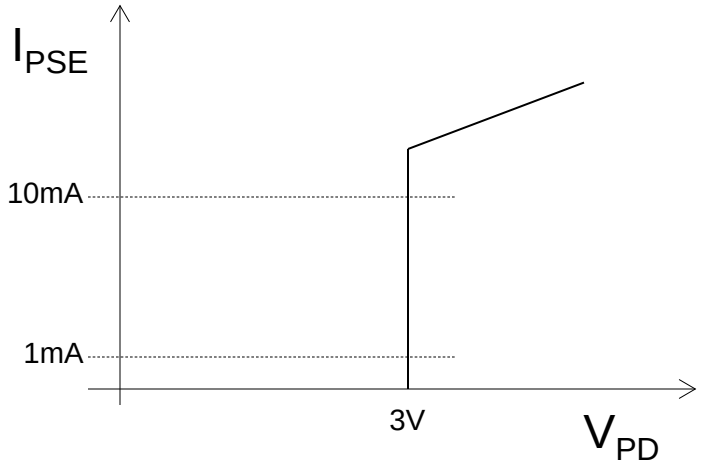
LINEAR TECHNOLOGY

PoDL PIs

- The PIs (coupling networks) are loosely defined.
  - Saturation current and DCR are constrained by the required class current, voltage, and power.
  - Minimum required inductance is constrained by the PHY droop requirement.
  - Inductor inter- and intra-winding capacitance is constrained by the PHY IL and RL requirements.
- An informative annex regarding the requirements on the PIs may be required (see gardner_3bu_1_0514.pdf).
- It may not be economically feasible to implement a PI that is both type 1 and type 2 for higher power levels.

PoDL PD Signature

- A current limited 3V constant voltage signature is proposed for the PD in the draft (see gardner_3bu_1_0714.pdf).
- Successful detection of the PD signature is required before applying power to the PI.
- Detecting a current limited, constant voltage signature through the PI vs. testing for an open and short prior to the application of power is easier and faster.



PD Classification and PSE/PD Mutual ID

- Classification is optional for a PD.
- The serial communication classification protocol (SCCP) is the proposed scheme for serial communication between the PSE and PD during classification and mutual ID.
- SCCP is based on the Maxim 1-Wire® Bus (see gardner_3bu_1_0914.pdf).
  - The PSE sources the bus pull-up current.
  - The PD signature device limits the bus logic high voltage.
- SCCP bus timing as proposed may not be compatible with type 1 systems because of the 100BASE-T1 droop requirement.
- SCCP function commands and protocols still need to be defined.

PoDL PSE and PD Noise Limits

- Work still needs to be done in order to fill out the PSE and PD EC tables in the draft.
- 1000BASE-T1 has put forward single tone noise limits at the PHY (see wang_3bu_1_0514.pdf).
- The analysis of the effects of PSE and PD voltage and current transients, respectively, has been done (see gardner_3bu_1_0514.pdf).
- Enough information is in place to calculate ripple noise and transient noise limits for the PSE and PD.
  - These limits may be more restrictive than was the case for PoE.

PSE and PD State Diagrams

- These are changed substantially from PoE
- PSE does detection, optional classification before applying power to PI.
- PD waits tpwr_dly after disabling detection signature before enabling MDI power.
- State variables and timers still need to be defined in the draft
- Peer review of the diagrams is both needed and welcome.

Maintain Power Signature (MPS)

- This is TBD in the draft.
- MPS needs to allow a PSE to differentiate between an open circuit and a low-power load condition.
  - PoE MPS scheme may be too power hungry for PoDL.
- Suggestions for a workable scheme are welcome!

Isolation and Fault Tolerance

- Requirements from PoE were copied into the draft with one major change:
  - The PSE is required to switch at least the positive conductor (both conductors may be switched).
- The PD in PoDL needs to be isolated from the frame or chassis ground:
  - Break ground loops
  - Fault tolerance (see Wienchowski_3bw_02_0914.pdf)
- Additional requirements?

PHY Electrical Specifications for PoDL

- Test fixtures for droop, jitter, distortion, PSD mask, and alien cross-talk are included.
  - Test fixtures in 100BASE-T1 are DC coupled!
- Droop.
  - Total droop is specified for 100BASE-T1 PHYs at less than 45% at 500ns.
  - How do we apportion droop between the PHY and PoDL?
- Insertion and Return loss.
  - This was left TBD.
  - Will PoDL be allowed to degrade PHY IL and RL?
  - If so, by how much?

Conclusion

- A draft for Clause 96 1-Pair Power over Data Lines (PoDL) has been put forward.
- Much work remains to be done before draft is complete.
- Please review and comment before the next meeting cycle!

Questions?