Serial Communication Classification Protocol (SCCP) for PoDL

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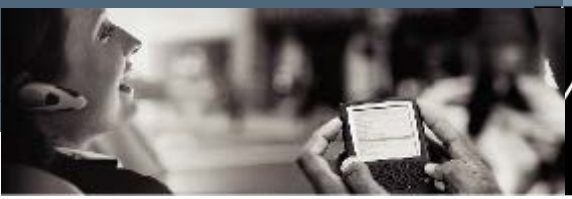


Presentation Objectives

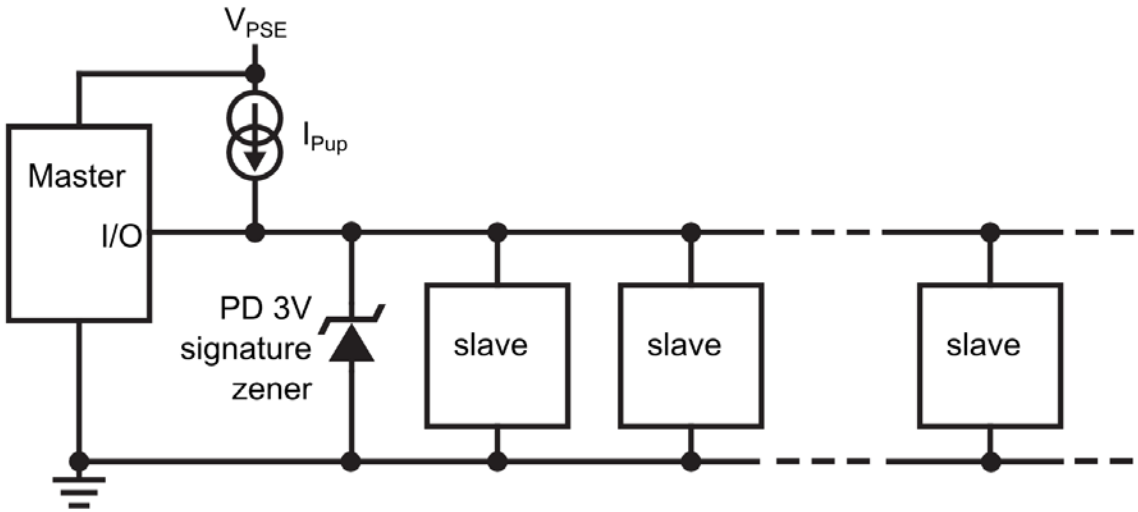
- To review key concepts and requirements for the proposed serial communication classification protocol (SCCP).
- To review those portions of the SCCP that still need to be addressed in the draft.

SCCP is Optional for PDs

- Successful detection of a PD signature is mandatory for link power.
- Classification is an optional requirement for link power.
- The SCCP will not work when the link is powered.
  - DLL may be used for communication between the PD and PSE when the link is powered.
- The SCCP may also be used for general purpose communication between the PSE and PD in the absence of link power.
  - Slave devices at the PD PI may rely upon ‘parasitic power’ from the PSE master device.

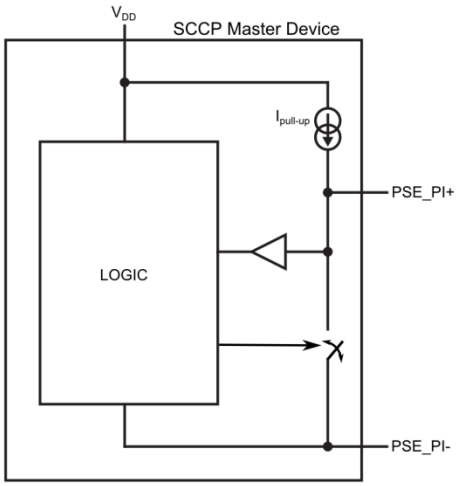
SCCP is derived from Maxim's 1-Wire® Bus

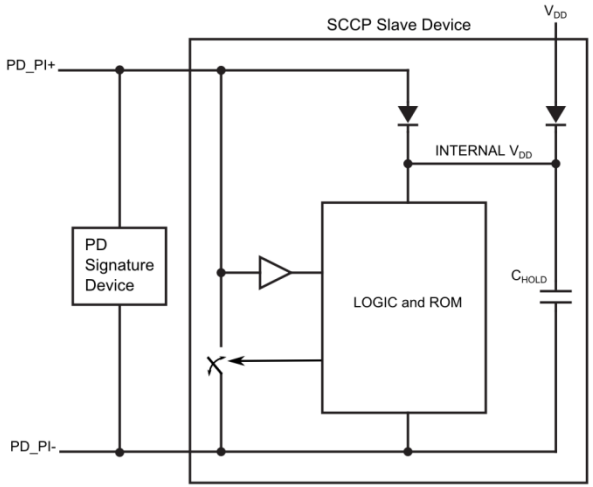
- Master device is at PSE PI.
- Slave device is at PD PI.
- Multi-drop slaves are supported.
- As is, SCCP is capable of bidirectional half-duplex communication at a rate of ~16kbps.
  - This rate may not be compatible with 100BASE-T1 PoDL!



SCCP Master and Slave

- Master sources pull-up current at PSE PI.
- Slave defines $V_{I/O}$ at PD PI using the PD constant voltage signature device.
- Slave(s) may derive parasitic power from the PSE pull-up current (~30mW).
- 3V I/O signaling levels are proposed in the draft.





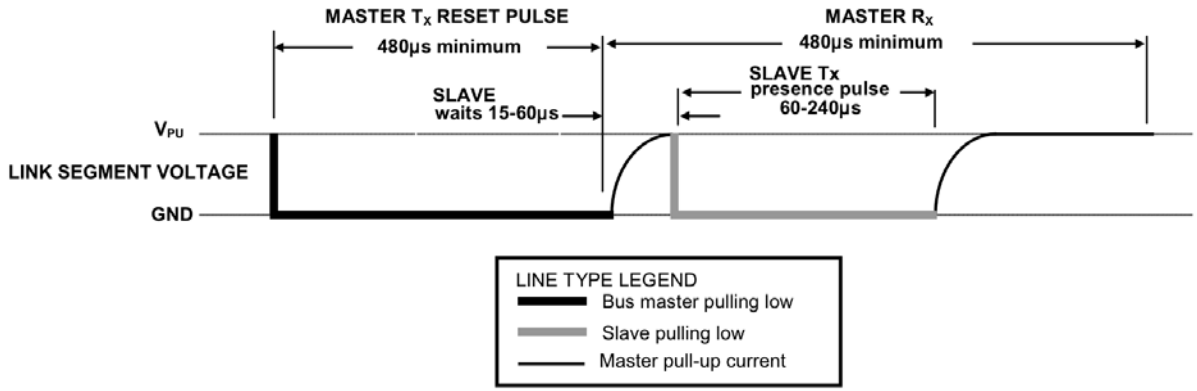
LINEAR TECHNOLOGY

SCCP Signaling Protocols

- Reset pulse
  - All transmissions are initiated by the master with a reset pulse which is followed by a slave Ack pulse, i.e. start of frame.
- Write “1”
- Write “0”
- Read “1”
- Read “0”
- All bit R/W operations are context dependent.
- All data and commands are transmitted LSB first.
- Data transmission length is typically 1-byte but could be longer.

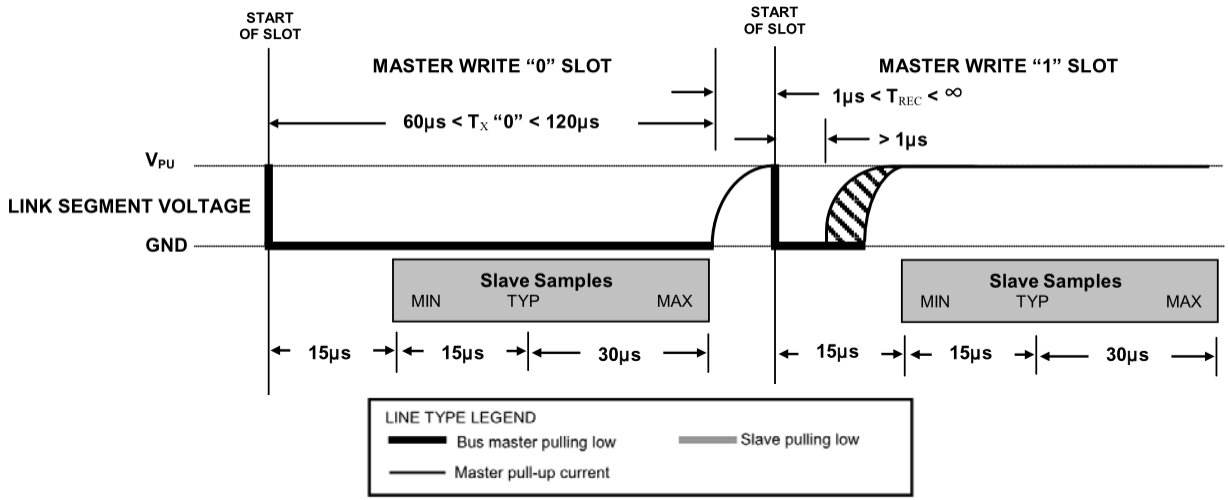
Reset Pulse

- This is equivalent to ‘start of frame.’
- Master pulls low for at least 480 μs and releases.
- Slave acknowledges by pulling low for at least 60 μs.
- PI voltage needs to rise in <15 μs.



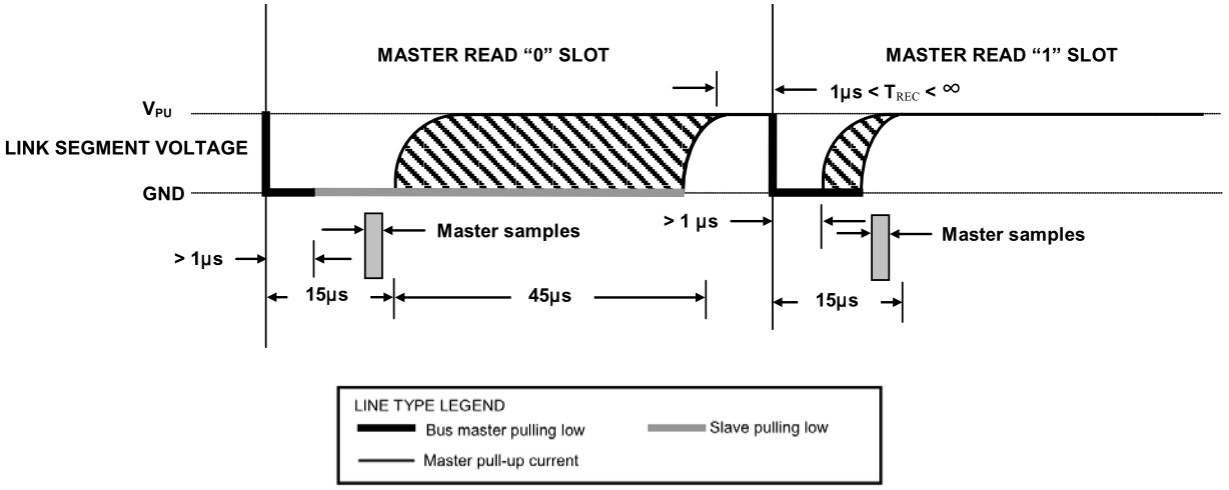
Write-Bit Operation

- Master initiates transmission with a falling edge.
- Falling edge triggers a monostable multivibrator in the slave that is clocked to read the master's data 30µs later.
- PI voltage needs to rise in <15µs.



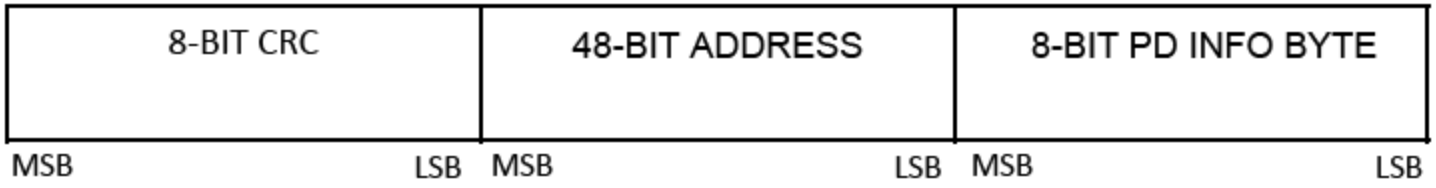
Read-Bit Operation

- Master initiates transmission with a falling edge.
- Master releases after 1µs.
- Slave either pulls low or allows PI voltage to rise.
- Master may sample PI voltage after 15µs.



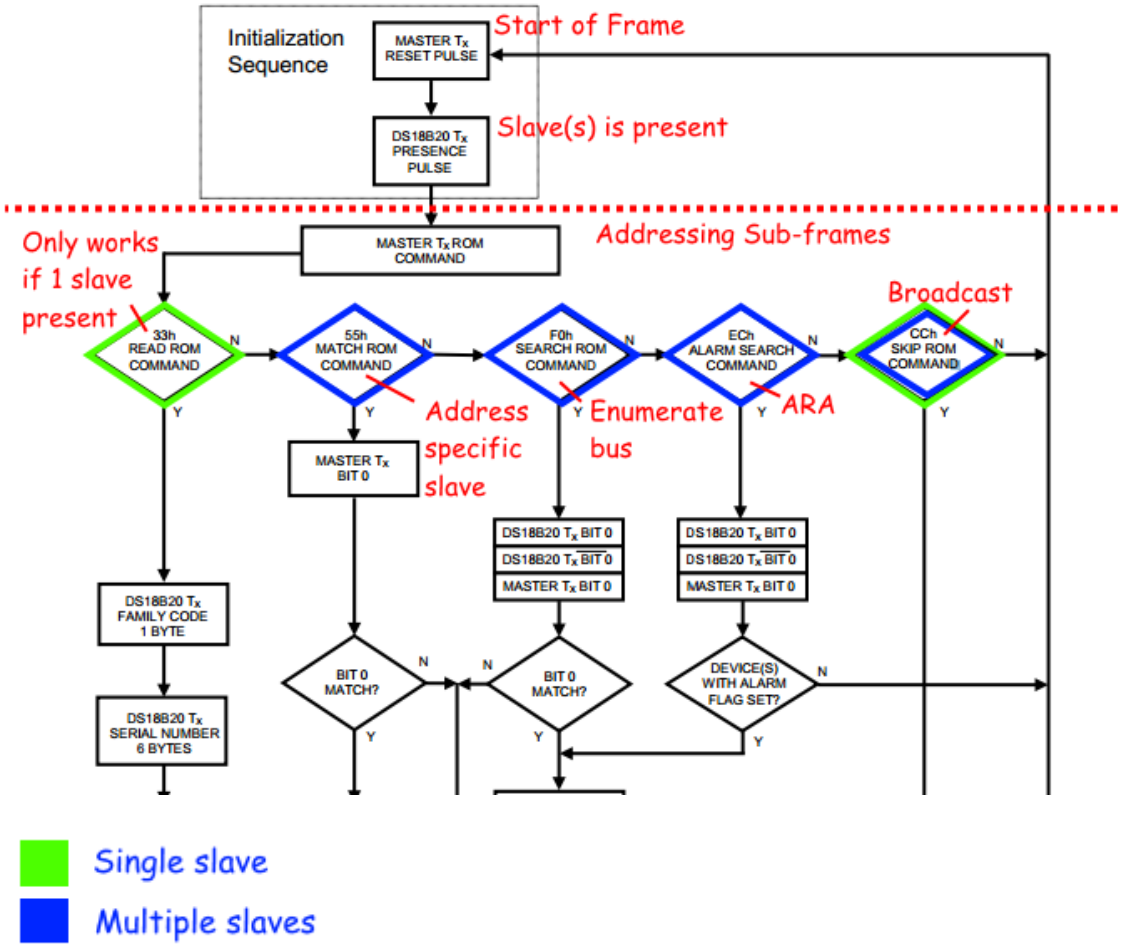
SCCP Addressing for Multi-Drop Slaves

- Is there a requirement to support multi-drop serial communication between a PSE and PD for PoDL?
  - If so, then the ROM command addressing scheme from 1-Wire® is proposed in the draft.
- The ROM address field in 1-Wire® is 64-bits long
  - Lowest byte may contain info about PD such as class and type
  - Next 6 bytes contain unique address info – do we need 6 address bytes for PoDL?
  - CRC byte is last



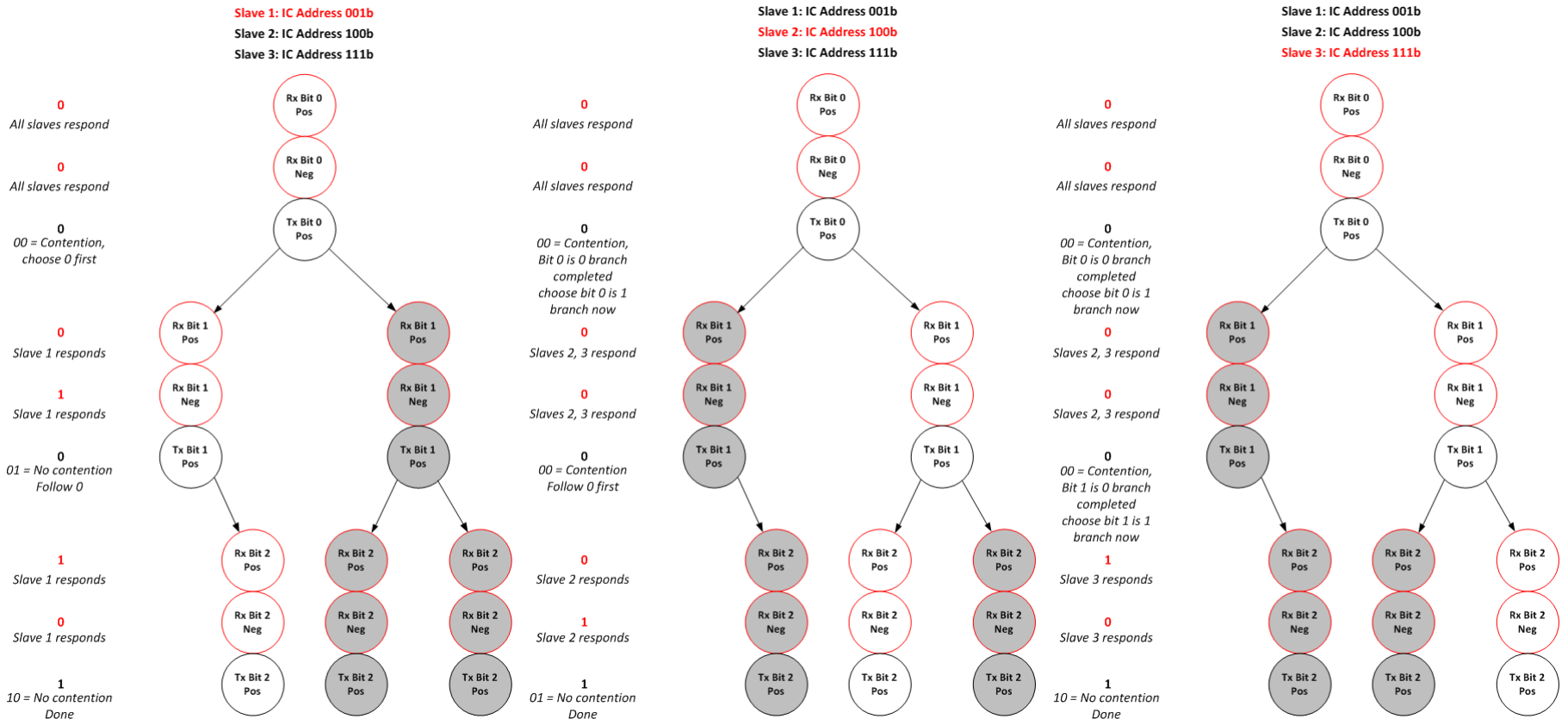
SCCP Addressing Protocols

- 1-Wire® has 5 ROM command protocols that were used in the draft for SCCP multi-drop addressing.
- Flow-chart in draft was copied from Maxim 1-Wire® device datasheet with new command names.



SCCP Enumeration uses a Binary Tree Search Algorithm

- 3-bit address search examples:



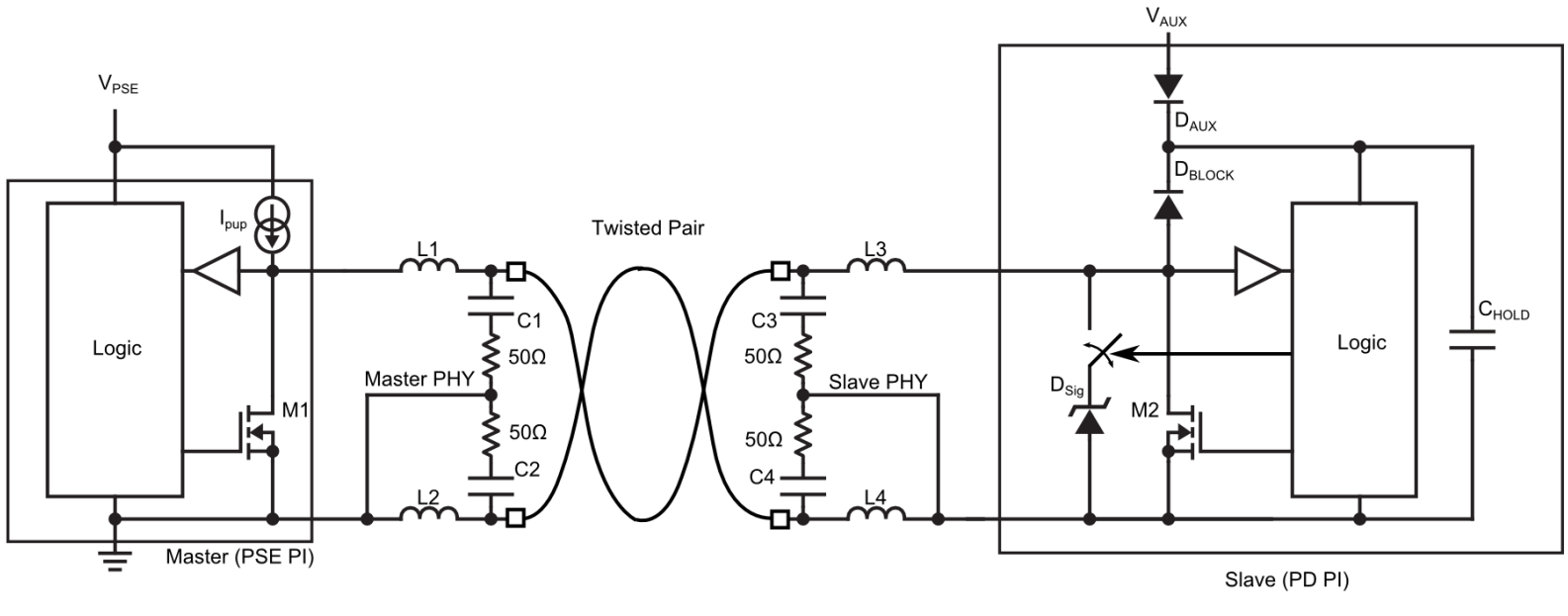
SCCP Function Commands

- This part of the SCCP was left as TBD.
- Some obvious commands for a PD might include:
  - Read PD status
  - Reset PD status
  - Write PSE information
  - Read or write PD GPIO state
  - Others?

Data Rates for SCCP

- Maxim 1-Wire® timing is geared for 16kbps.
  - Electrical parameters in the draft are consistent with this.
  - Bus must rise in <15μs
- Capacitive load on SCCP for 100BASE-T1 PoDL and 1000BASE-T1 PoDL are very different:
  - The 100BASE-T1 droop specification requires PoDL inductors of >42μH which implies PHY DC blocking capacitors > 68nF for a critically damped system.
  - 1000BASE-T1 currently has no droop requirement, but the PHY HPF pole is >10MHz so PHY DC blocking capacitors >1.8nF may be sufficient.
- Do we redefine SCCP timing for 100BASE-T1 PoDL?
  - 500bps is consistent with today's 100BASE-T1 droop requirement.

PoDL SCCP Bus Block Diagram



$$L1 = L2 = L3 = L4 = L_{PoDL} > \frac{-50\Omega \times t_{droop}}{\ln(1 - 0.45)}$$

Conclusions

- Maxim's 1-Wire® signaling protocols and parasitic slave power concept have been used as the basis for SCCP in the draft.
- Addressing protocols based on the 1-Wire® ROM commands are also in the draft.
  - Is there a requirement for multi-drop SCCP?
- The 1-Wire 16kbps data rate is compatible with 1000BASE-T1 PoDL but not with 100BASE-T1 PoDL.

Questions?