A Power Solution for Automotive Applications over 100BASE-T1 Data Line

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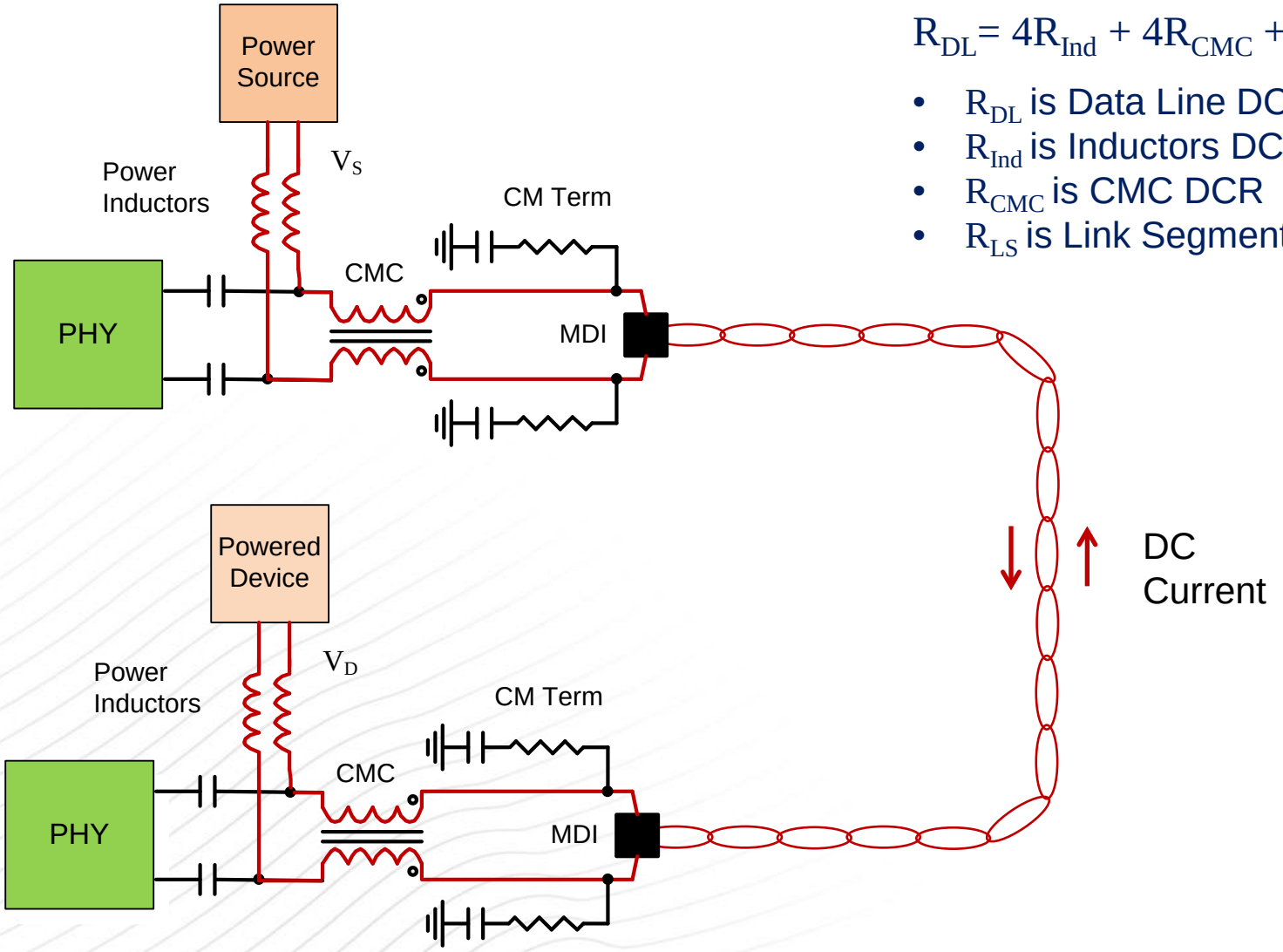
Outline

- A PoDL solution for automotive applications over 100BASE-T1 data line is analyzed. The net deliverable power to the device and power efficiency using various source voltages are discussed.

A PoDL schematic for automotive applications over UTP cables



$R_{DL} = 4R_{Ind} + 4R_{CMC} + 2R_{LS}$

- R_{DL} is Data Line DCR
- R_{Ind} is Inductors DCR
- R_{CMC} is CMC DCR
- R_{LS} is Link Segment DCR

Foreword

- Power inductors are placed at the PHY side of CMC to help with MDI balance requirements in automotive applications over UTP cabling.
- When power inductors are used at PHY side of CMC, the CMC has to carry the DC current.
- To optimize power efficiency of a PoDL solution, the power loss on the data lines as well as loss on the Voltage regulators need to be considered.
- In addition to power efficiency, size, cost and weight of cables, CMC and power inductors need to be taken into account. High source voltages may be needed to deliver high power in this case.
- Data line DCR affects deliverable power and power efficiency of a PoDL solution. DCR increase due to high temperature needs to be considered.

Data Line DCR

- The following data are provided at room temperature of 20C.
  - DCR per wire for a 15m Link Segment (cable and connectors) = 2Ω
  - DCR per wire for a 300mA CMC[1] = 1.5Ω
  - DCR per single power inductor = 0.5Ω
- Total Data Line DCR at room temperature is calculated to be;

$$R_{DL} = 4x0.5 + 4x1.5 + 2x2 = 12\Omega$$

- Total Data Line DCR at max temperature of 125C is calculated to be;

$$R_{DL,125C} = R_{DL}(1+0.00393(125-20)) = 17\Omega$$

assuming copper temperature coefficient of 0.00393

1. Note: The selected CMC for analysis allows maximum DC current of 300mA under all operating conditions. This is in addition to data current of about 10mA (rms).

Maximum deliverable power to a device

- Max deliverable power to a powered device $P_{D,max}$ is calculated for a given R_{DL} and V_s ;

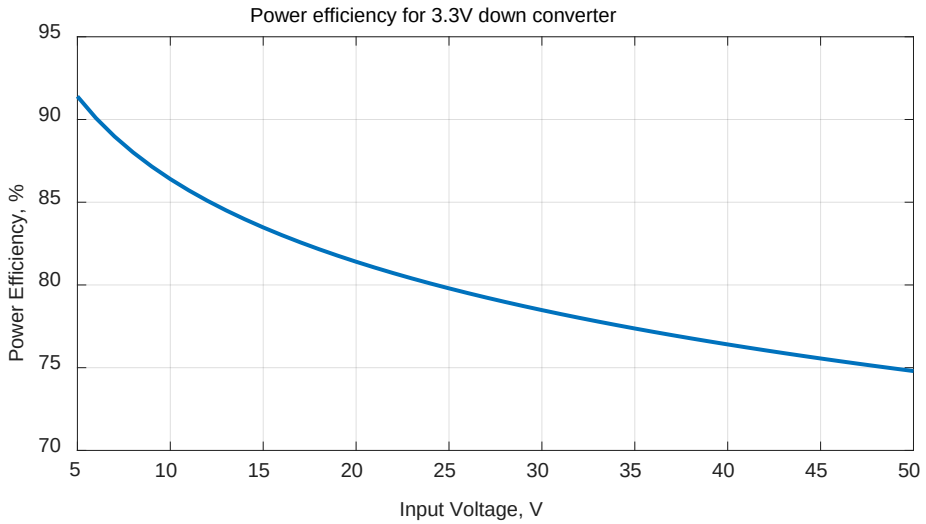
$$P_{D,max} = V_s^2 / 4R_{DL} \quad \text{if} \quad (V_s / 2R_{DL} < I_{max})$$

$$(V_s - I_{max} R_{DL})\, I_{max} \quad \text{otherwise}$$

- For $R_{DL,20C} = 12\Omega$ and $I_{max} = 0.3A$, we get;
  - $P_{D,max} = 0.88W$ for $V_S = 6.5V$ (un-regulated, form a low battery)
  - $P_{D,max} = 2.52W$ for $V_S = 12V$ (regulated)
  - $P_{D,max} = 6.12W$ for $V_S = 24V$ (regulated)
  - $P_{D,max} = 13.32\ W$ for $V_S = 48V$ (regulated)
- For $R_{DL,125C} = 17\Omega$ and $I_{max} = 0.3A$, we get;
  - $P_{D,max} = 0.62W$ for $V_S = 6.5V$ (un-regulated, form a low battery)
  - $P_{D,max} = 2.07W$ for $V_S = 12V$ (regulated)
  - $P_{D,max} = 5.67W$ for $V_S = 24V$ (regulated)
  - $P_{D,max} = 12.87W$ for $V_S = 48V$ (regulated)
- The above calculated power is lost in part in the voltage regulator, therefore actual delivered power to the device is lower.

Regulator loss and net device power

- Power efficiency for voltage down converters depends on many parameters. For devices using 3.3V supply, the plot shown is observed from some existing switching regulators[1].



- For $R_{DL,125C} = 17\Omega$ and $I_{max} = 0.3A$, considering Voltage regulator loss, the maximum net power that can be delivered to a device is;

Net $P_{D,max}$ = 1.84W for V_S = 12V (regulated source), P_S = 3.6W
Net $P_{D,max}$ = 4.64W for V_S = 24V (regulated source), P_S = 7.2W
Net $P_{D,max}$ = 9.77W for V_S = 48V (regulated source), P_S = 14.4W

1. Note: The curve assumed here is an approximation of regulators power efficiency. More accurate numbers may be obtained consulting data sheet of a particular voltage regulator used in a design.

Power Loss on Data Line and Voltage Regulator

Power Loss (L_{DL} in Watt , L_{Reg} in Watt) at 125 Celsius			
P_D	**V_S=12V**	**V_S=24V**	**V_S=48V**
1W	(0.158 , 0.139)	(0.031 , 0.197)	(0.008 , 0.249)
2W	(1.237 , 0.229)	(0.134 , 0.389)	(0.030 , 0.496)
3W	X	(0.327 , 0.575)	(0.070 , 0.742)
4W	X	(0.634 , 0.754)	(0.126 , 0.987)
5W	X	(1.097 , 0.924)	(0.200 , 1.231)
6W	X	X	(0.292, 1.474)
7W	X	X	(0.405 , 1.715)
8W	X	X	(0.538 , 1.955)
9W	X	X	(0.693 , 2.194)
10W	X	X	(0.872 , 2.431)

- Solve the second order equation $P_D = I (V_s - R_{DL} I)$ for I and then $L_{DL} = R_{DL} I^2$ is the data line loss. For example when $P_D = 2W$ and V_s=24V, I is calculated to be 0.089A for $R_{DL} = 17\Omega$ and L_{DL}=0.134W. X denotes no solution when $I > 0.3A$. P_D denotes power delivered to voltage regulator and therefore comprises the net device power plus the regulator loss L_{Reg}. L_{Reg} is calculated based on regulator input voltage $V_D = (V_s - R_{DL} I)$ and P_D and using the power efficiency curve.

Power efficiency for various source voltages and device powers

Power Efficiency ($P_{D,net}$ in Watt / P_S in Watt)			
P_D	**V_S=12V**	**V_S=24V**	**V_S=48V**
1W	74% (0.861 / 1.158)	78% (0.803 / 1031)	75% (0.751 / 1.001)
2W	55% (1.771 / 3.237)	75% (1.611 / 2.134)	74% (1.504 / 2.030)
3W	X	73% (2.425 / 3.327)	74% (2.258 / 3.070)
4W	X	70% (3.246 / 4.634)	73% (3.013 / 4.126)
5W	X	67% (4.076 / 6.097)	72% (3.769 / 5.200)
6W	X	X	72% (4.526 / 6.292)
7W	X	X	71% (5.258 / 7.405)
8W	X	X	71% (6.045 / 8.538)
9W	X	X	70% (6.806 / 9.693)
10W	X	X	70% (7.569 / 10.872)

- Power Efficacy is calculated;

$$\eta = P_{D,net} / P_S = (P_D - L_{Reg}) / (P_D + L_{DL})$$

- See the table in the previous page for L_{Reg} and L_{DL}. X denotes no solution when CMC, power inductors or cable is limited by I_{max} = 0.3A.

Optimizing power, lowering data line DCR

- The following factors can be considered to improve power efficiency of a PoDL solution.

1. Placing PoDL inductors on the cable side of CMC. This will eliminate power loss in data line CMC, improves power efficiency and results in smaller size CMC. The challenge is balance requirement in PoDL inductors which should hold under all working conditions[1] (?).

2. Reducing DCR in CMC and PoDL inductors. This is expected to increase size, weight and cost of a solution and should be considered only if the saving in power is significant as compared to the loss in the powered device voltage regulator or if operation with low voltage sources is required.

3. Reducing DCR in data cable (link segment). This is expected to increase cable weight and cost and should be considered if the power saving is significant as compared to other losses including that of regulators.

1. Note: The balance needs to be verified while the PoDL supply GND is connected to data GND, otherwise a separate power CMC is required for power supply isolation adding to power loss, cost and weight of the solution.

Summary and conclusion

- Presented a PoDL solution using a 300mA CMC with more than 70% efficiency when considering the loss over data line as well as Voltage regulator at the powered device.
- For the presented PoDL solution, the total data line DCR is about 12Ω and may go up to 17Ω at a temperature of 125C.
- For devices requiring near 1W power, regulated Voltages of 12V, 24V or 48V may be used for source. For devices requiring between 1.5W to 3W, either 24V or 48V source may be considered. For devices requiring 3.5W to 7.5W, 48V supply needs to be used.
- For the assumed data line DCR, use of un-regulated battery (min of 6.5V) as source is not recommended unless the required power of the powered device is less than 0.5W. If battery voltage is maintained to be closer to the nominal 12V and with lower DCR for data line, then higher power may be delivered without using regulated supply at source.