0.0.0.1 Link Segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	DC loop resistance	104.2	M	Yes [ ]	~~Less than 6.5Ω~~Less than 6.0Ω for 12V unregulated system power classes and less than 6.5Ω for all other system power classes.

0.0.0.2 Power sourcing equipment (PSE)

Item	Feature	Subclause	Status	Support	Value/Comment
PSE1	Voltage and power requirements	104.3.2	M	Yes [ ]	As defined in Table 104-1 for each relevant system class
PSE2	PSE behavior	104.3.3	M	Yes [ ]	In accordance with state diagram shown in Figure 104-4
PSE3	~~Applying power~~	~~104.3.3.1~~	~~M~~	~~Yes [ ]~~	~~Not until a detection of a valid PD is present~~
PSE4	~~Power not supplied within T_{inrush} with SCCP disabled~~	~~104.3.3.1~~	~~M~~	~~Yes [ ]~~	~~Wait for TED before attempting to apply power again~~
PSE5	~~Power not supplied within T_{inrush} with SCCP enabled~~	~~104.3.3.1~~	~~M~~	~~Yes [ ]~~	~~Initiate and successfully complete PD classification before attempting to apply power again~~
	external_wakeup variable	104.3.3.3	M	Yes [ ]	Re-detect the PD before re-applying the full operating voltage to the PI after request is received
	pd_wakeup varibale	104.3.3.3	M	Yes [ ]	Re-detect the PD before re-applying the full operating voltage to the PI after valid current signature at the PI is detected
PSE6	pi_powered variable	104.3.3.3	M	Yes [ ]	If false, do not apply power to the PI. If True, apply power to the PI
PSE7	sleep_detected variable	104.3.3.3	M	Yes [ ]	~~TBD~~Transition to SLEEP state when the average value of I_{port} is less than or equal to I_{sleep} threshold
PSE8	wakeup_detected variable	104.3.3.3	M	Yes [ ]	~~TBD~~
PSE9	PSE-probing	104.3.4	M	Yes [ ]	Probe the PI in order to detect a valid PD signature
PSE10	Detection currents	104.3.4.1	M	Yes [ ]	Within I_{valid} current range specified in Table 104-2 with a valid PD detection signature as specified in Table 104-4

PSE11	Accept valid PD signature	104.3.4.2	M	Yes [ ]	From link segment with a constant voltage in the range of V_{good_PSE} in response to a probing current in the range of I_{valid} as specified in Table 104-2
PSE12	Reject invalid PD signature	104.3.4.3	M	Yes [ ]	From link segment that exhibits the following characteristics outlined in Table 104-2 and Table 104-5: a) Constant voltage less than or equal to $V_{bad_lo_PSE}$max b) Constant voltage greater than or equal to $V_{bad_hi_PSE}$min c) Capacitance greater than or equal to C_{bad}min
PSE13	Applying power with SCCP enabled	104.3.5	M	Yes [ ]	Only after attempting to complete classification and mutual identification
PSE14	Providing power to the PSE PI	104.3.6	M	Yes [ ]	To conform to electrical limits~~ set out~~ in Table 104-3
PSE15	PSE output	104.3.6	M	Yes [ ]	To conform with electrical requirements set out in Table 104-3~~5~~ in both powered and unpowered modes
PSE16	PI SLEEP voltage while in SLEEP state	104.3.6.1	M	Yes [ ]	Within V_{Sleep} range outlined in Table 104-3
PSE17	SLEEEP_SETTLE state	104.3.6.1	M	Yes [ ]	Discharge the PSE PI to the range of V_{Sleep}
	Enter SLEEEP_SETTLE state	104.3.6.2	M	Yes [ ]	If a valid MPS is not present at the PI while operating in the POWER_ON state
	PI discharge while in SLEEP_SETTLE state	104.3.6.2	M	Yes [ ]	To the range of V_{sleep} with a current greater than $I_{discharge}$
	PD wakeup request valid while in SLEEP state	104.3.6.2.1	M	Yes [ ]	If I_{port} is in the valid range of I_{wakeup} for a minimum of t_{wakeup}
	PD wakeup request invalid while in SLEEP state	104.3.6.2.1	M	Yes [ ]	If I_{port} is greater than $I_{wakeup\_bad\_hi}$ or less than $I_{wakeup\_bad\_lo}$
~~PSE18~~	~~PD sleep request while in POWER_ON state~~	~~104.3.6.4~~	~~M~~	~~Yes [ ]~~	~~Valid if I_{Port} averaged over sliding window t_{Sleep} wide is less than or equal to I_{Sleep} min~~
~~PSE19~~	~~PI discharge while in SLEEP_SETTLE state~~	~~104.3.6.4~~	~~M~~	~~Yes [ ]~~	~~To the range of V_{Sleep} with a current greater than $I_{discharge}$~~
~~PSE20~~	~~PD wakeup request while in SLEEP state~~	~~104.3.6.4~~	~~M~~	~~Yes [ ]~~	~~Valid if I_{Port} is greater than I_{Wakeup} min for a minimum of t_{Wakeup}~~
PSE21	Power not applied as specified	104.3.6.6~~5~~	M	Yes [ ]	New detection cycle initiated before power application
PSE22	V_{PSE} to V_{Sleep}~~Off~~ discharge time while in POWER_ON state	104.3.6.7~~6~~	M	Yes [ ]	Defined as T_{Off} in Table 104-3
PSE23	P_{Class}	104.3.6.8~~7~~	M	Yes [ ]	As defined in Table 104-1

PSE24	Measurement of P_{Class}	104.3.6.8~~7~~	M	Yes [ ]	Averaged from uniform sliding window of 1 second wide
PSE25	~~PSE PI power removal while in SLEEP state~~Normal Operating voltage removal while in POWER_ON state	104.3.7	M	Yes [ ]	In absence of PD Maintain ~~Power Signature~~Full Voltage Signature
PSE26	MFVS~~PS~~ present	104.3.7.1	M	Yes [ ]	If I_{Port} ~~averaged over sliding window T_{MPS} wide~~ is greater than or equal to I_{Hold} max for a minimum of T_{MFVS}
PSE27	M~~PS~~FVS absent	104.3.7.1	M	Yes [ ]	If I_{Port} ~~averaged over sliding window T_{MPS} wide~~ is less than or equal to I_{Hold} min
PSE28	M~~PS~~FVS absent for duration greater than TM~~P~~FVDO	104.3.7.1	M	Yes [ ]	~~Remove power from the PI~~Reduce voltage at the PI to the range of V_{Sleep}

0.0.0.3 Powered Device (PD)

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Voltage and power requirements	104.4.2	M	Yes [ ]	As defined in Table 104-1 for each relevant system class
PD2	PD behavior	104.4.3	M	Yes [ ]	In accordance with state diagram shown in Figure 104-6
~~PD3~~	~~Present constant voltage signature~~	~~104.4.3.1~~	~~M~~	~~Yes [ ]~~	~~If PD input voltage is less than $V_{sig\_disable}$~~
~~PD4~~	~~Remove constant voltage signature~~	~~104.4.3.1~~	~~M~~	~~Yes [ ]~~	~~When input voltage exceeds $V_{sig\_disable}$ and wait t_{pwr_delay} before drawing power from the MDI~~
~~PD5~~	~~PD fault or MPS removal~~	~~104.4.3.1~~	~~M~~	~~Yes [ ]~~	~~Rising V_{PD} edge through the $V_{on(max)}$ causing PD to re-enable MDI power after delay of t_{pwr_delay}~~
~~PD6~~	~~Detection signature~~	~~104.4.4~~	~~M~~	~~Yes [ ]~~	~~Present either valid or non-valid at the PI~~
	Present valid detection signature	104.4.4	M	Yes [ ]	When V_{PD} drops below V_{sig_enable} unless it is asleep
	Removal of current draw of detection signature	104.4.4	M	Yes [ ]	When V_{PD} rises through $V_{sig\_disable}$
	PD detection signature	104.4.4	M	Yes [ ]	To consist of a current limited, constant voltage as specified in Table 104-4 when measured by the PSE
PD7	Valid detection signature	104.4.4	M	Yes [ ]	In accordance with the characteristics shown in Table 104-4
PD8	Non-valid detection signature	104.4.4	M	Yes [ ]	In accordance with at least one of the characteristics shown in Table 104-5
PD9	PD power	104.4.6	M	Yes [ ]	In accordance with the characteristics shown in Table 104-6
	Turn on voltage	104.4.6.1			Less than or equal to V_{On} as specified in Table 104-6
	Turn off voltage	104.4.6.1			Greater than or equal to V_{Off} as specified in Table 104-6
PD10	~~SLEEP and WAKEUP~~PD_SLEEP state input voltage~~s~~	104.4.6.1	M	Yes [ ]	~~In the range of V_{Sleep_PD}~~ Greater than $V_{Sleep\_PD\_min}$ as specified in Table 104-6
PD12	Input current while in SLEEP_PENDING and SLEEP states	104.4.6.2~~5~~	M	Yes [ ]	Drawn current is averaged over sliding window t_{Sleep} wide in the range of I_{Sleep} as specified in Table 104-6
PD13	Input current while in WAKEUP state	104.4.6.2~~5~~	M	Yes [ ]	Drawn current is within range of I_{Wakeup_PD} as specified in table 104-6

	PD ripple and noise	104.4.6.34	M	Yes [ ]	In accordance with specifications shown in Table 104-6 for all operating voltages in the range of V_{Port_PD} and over the range of input power of the device
	PSE ripple and noise	104.4.6.34	M	Yes [ ]	Operate in accordance to the levels specified in Table 104-3 in the presence of PSE ripple and noise appearing at the PD PI
	PD stability	104.4.6.53	M	Yes [ ]	When PD is fed voltage between V_{Port_PSE}min and V_{Port_PSE}max with R_{Loop_max} in series, P_{Port_PD} is defined by equation 104-1
PD16	PD ~~maintain power signature~~Maintain Full Voltage	104.4.7	M	Yes [ ]	Provide valid ~~MPS~~Maintain Full Voltage Signature (MFVS) at the PI
PD17	PD ~~maintain power signature~~MFVS current draw	104.4.7	M	Yes [ ]	Equal to or greater than I_{Hold_PD}~~(min) when averaged over sliding window T_{MPS} wide~~ for a minimum duration of T_{MFVS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than TMFVDO_PD
PD18	No longer require full input operating voltage~~power~~	104.4.7	M	Yes [ ]	Remove current draw of the MFV~~P~~S from the PI

0.0.0.4 Common Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
COME L1	PI output conductor pair fault tolerance	104.5.2	M	Yes [ ]	Meet the requirements of the appropriate specifying clause (See Clauses 96 and 97)
COME L2	100BASE-T1 PoDL system MDI return loss	104.5.3.1	M	Yes [ ]	Meet or exceed Equation 104-2
	1000BASE-TI PoDL system MDI return loss	104.5.3.1	M	Yes [ ]	Meet or exceed Equation 104-3
~~COME L3~~	~~Testing MDI return loss requirement in the presence of PI load current~~	~~104.5.3.1~~	~~M~~	~~Yes [ ]~~	~~Meet or exceed requirement given in equation 104-2~~
~~COME L4~~	~~Positive and negative droop magnitude~~	~~104.5.3.1~~	~~M~~	~~Yes [ ]~~	~~Less than TBD%~~

0.0.0.5 PSE Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
PSEEL 1	PSE PI	104.5.2	M	Yes [ ]	Withstand the application of short circuits between the wires within the cable for an indefinite period of time without damage
PSEEL 2	Short circuit current magnitude	104.5.2	M	Yes [ ]	Not to exceed I_{LIM}max as defined in Table 104-3 given an indefinite short circuit

0.0.0.6 PD Electrical

Item	Feature	Subclause	Status	Support	Value/Comment
PDEL1	DC isolation	104.5.1	M	Yes [ ]	Provided between all accessible external conductors, including frame ground (if any), and all MDI leads

0.0.0.7 SCCP

Item	Feature	Subclause	Status	Support	Value/Comment
SCCP1	SCCP master	104.6	M	Yes [ ]	Source the required pull-up current
SCCP2	SCCP master	104.6.1	M	Yes [ ]	Source a pull-up current in order to drive the bus voltage high and meet the required electrical specifications for SCCP

SCCP3	SCCP communication	104.6.3.1	M	Yes [ ]	Begins with an initialization sequence consisting of a result pulse from the master followed by a presence pulse from the slave. See Figure 104-~~10~~9
SCCP4	Initialization sequence	104.6.3.1	M	Yes [ ]	Master transmits a reset pulse by pulling its PI voltage low for t_{RSTL} and the releases its PI and goes into receive mode (RX)
SCCP5	Slave presence pulse	104.6.3.1	M	Yes [ ]	Transmitted after detecting rising edge at PD PI and waiting t_{PDHIGH}
SCCP6	Master write time slots	104.6.3.2	M	Yes [ ]	Write 1 time slot to transmit logic 1 to slave and write 0 time slot to transmit logic 0 to slave
SCCP7	Write time slot duration	104.6.3.2	M	Yes [ ]	Defined as t_{SLOT} shown in Table 104-10~~7~~
SCCP8	Write time slot recovery time	104.6.3.2	M	Yes [ ]	Defined as t_{REC} shown in Table 104-10~~7~~
SCCP9	Write time slot initiation	104.6.3.2	M	Yes [ ]	Initiated by pulling PI port voltage low as shown in Figure 104-10~~1~~
SCCP10	Write 1 time slot generation	104.6.3.2	M	Yes [ ]	Write by pulling PI port voltage low then release PI port within t_{LOW1}
SCCP11	Write 0 time slot generation	104.6.3.2	M	Yes [ ]	Write by pulling PI port voltage low then hold PI port low for t_{LOW0}
SCCP12	Read time slot generation	104.6.3.3	M	Yes [ ]	Generated by the master immediately after issuing a function command which requires data from the slave
SCCP13	Read time slot duration	104.6.3.3	M	Yes [ ]	Defined as t_{SLOT} shown in Table 104-7
SCCP14	Read time slot recovery time	104.6.3.3	M	Yes [ ]	Defined as t_{REC} shown in Table 104-7
SCCP15	Read time slot initiation	104.6.3.3	M	Yes [ ]	Initiate by pulling PI port voltage low for t_{INIT} then release the port
SCCP16	Slave transmit	104.6.3.3	M	Yes [ ]	Transmit a 1 or 0 at the slave PI after master initiates read time slot
SCCP17	Slave transmit 1	104.6.3.3	M	Yes [ ]	Leave PI port voltage high
SCCP18	Slave transmit 0	104.6.3.3	M	Yes [ ]	Pull PI port voltage low
SCCP19	Slave transmit 0 duration	104.6.3.3	M	Yes [ ]	While transmitting 0, hold the PI low for t_{LOW0}, then release the PI by the end of the time slot

SCCP20	Read time slot sample	104.6.3.3	M	Yes [ ]	Master releases PI and then samples subsequent voltage within t_{RDV} from the start of the time slot
SCCP21	Sum of T_{INIT}, T_{REC}, and master sample time	104.6.3.3	M	Yes [ ]	Less than t_{RDV} for a read time slot
SCCP22	Address command	104.6.4.3	M	Yes [ ]	Master must issue an appropriate address command prior to issuing a function command
SCCP23	Read address command	104.6.4.3.2	M	Yes [ ]	Only to be used when there is one slave on the bus
SCCP24	Function command response	104.6.4.3.3	M	Yes [ ]	Only sent when the 64-bit slave write address exactly matches that sent by the master
SCCP25	Write address mismatch	104.6.4.3.3	M	Yes [ ]	Wait for a reset pulse
SCCP26	Alarm search command response	104.6.4.3.5	M	Yes [ ]	Only by slaves with a set alarm flag
SCCP27	Alarm search cycle	104.6.4.3.5	M	Yes [ ]	Return to Step1 (Initialization) after every alarm search cycle