Detection, Inrush, and Over-Current Loose Ends

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Presentation Objectives

- Review and propose remedies for the portions of D1.3 pertaining to detection, inrush and output current that missing.

Detection and Inrush

- Total time from start of detection to end of the PD's t_{power_delay} needs to be consistent with automotive fast start-up time requirement (less than 10ms).
- If possible, the standard should allow a class of PDs to exist with up to 10µF C_{in} during inrush in order to minimize cost and complexity.
- The PSE slew rate and maximum current during inrush need to be large enough to allow C_{PD} to be fully in-rushed during fast start-up.
  - Example 0.2A/10µF = 20V/ms or ~3ms to ramp up V_{PD} to 60V.
- In order for detection to be compatible with fast start-up, the minimum probe current may need to be increased in order to ramp from V_{sleep} to $V_{signature}$ in a time that is consistent with the fast start-up requirement.
  - Need to define minimum $V_{signature}$ hold time and maximum time for detection, t_{DET} max.
  - May need to consider shorter hold time for T_{Wakeup} (currently 1ms min).

Proposed Changes to Baseline Text for Detection and Power-Up

- 104.3.4.2 Detection criteria
  - A PSE shall accept as a valid PD signature a link segment with a constant voltage in the range of V_{good_PSE} in response to a probing current in the range I_{valid} for at least T_{vsig_hold} min as specified in Table 104–2.
  - The PSE shall complete detection in less than T_{det} max when the PSE PI is pre-biased at V_{Sleep}.

Proposed Changes to Baseline Text for Detection and Power-Up Cont'd

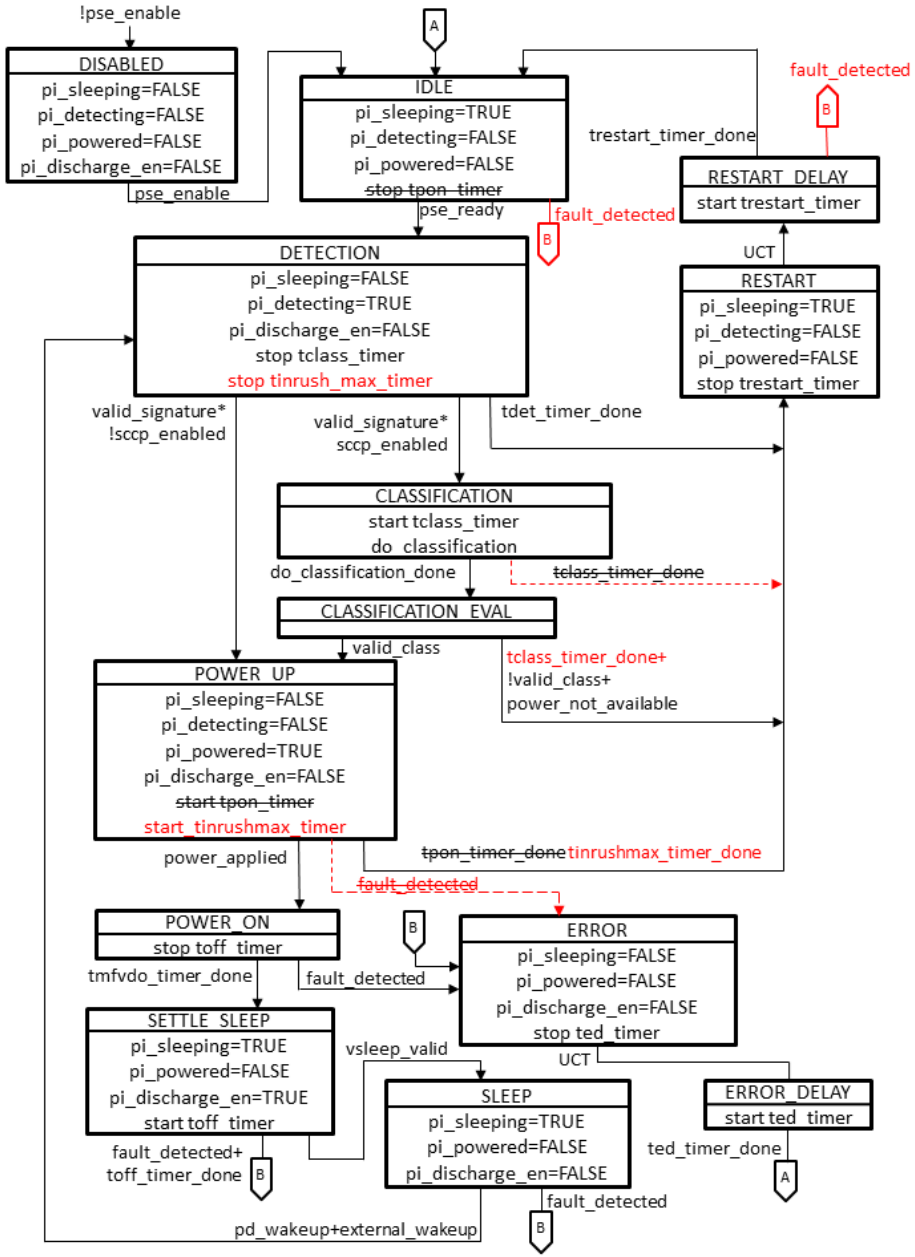
- 104.3.5 PSE classification of a PD and mutual identification
  - A PSE with SCCP enabled shall ~~attempt to~~ complete classification and mutual identification after detection and prior to ~~applying~~ application of full operating voltage ~~power~~ to the PI in a time less than T_{class} as specified in Table 104-3. If classification is not completed before the T_{class} timer expires, a new detection cycle shall be initiated before any subsequent application of full operating voltage.
- 104.3.6.5 Turn on time
  - The specification for ~~T~~$_{inrush}$ T_{inrush_max} in Table 104–3 applies to the maximum PSE power up time for a PD after completion of detection. If power is not applied as specified, a new detection cycle shall be initiated before any subsequent application ~~of power~~ of full operating voltage.

Proposed State Diagram Changes for Detection, Classification, and Power-Up

- Rename T_{pon} as T_{inrush_max} and define it as the longest time POWER_UP can last.
- Add fault_detected arcs to the IDLE and RESTART_DELAY states in order to force removal of sleep bias if the PSE is limiting current outside of the POWER_ON state for longer than t_{LIM}.
- Delete the tclass_timer_done exit arc from CLASSIFICATION state and add it as an additional OR'd condition to the exit arc out of the CLASSIFICATION_EVAL state.
  - Propose 300ms to 366ms as the maximum amount of time CLASSIFICATION and CLASSIFICATION_EVAL can last before re-detection is required.
  - Define do_classification function to be the proposed classification function command sequence proposed in heath_3bu_1_1015.pdf.

Proposed PSE state diagram changes

- $T_{pon} \rightarrow T_{inrush\_max}$
- tclass_timer_done moves to arc to RESTART exiting CLASSIFICATION_EVAL
- Arcs added for fault detected when not in POWER_ON state



V_{on} and $T_{powerdly}$

- $T_{powerdly}$ must be long enough to guarantee that the PD does not enable MDI_POWER before inrush is complete.
- $T_{powerdly}$ begins when V_{PD} rises through V_{on}.
- The draft currently defines V_{on} max but not V_{on} min!
  - Propose setting V_{on} min to 90% of V_{on} max as currently defined in the draft.
- $T_{powerdly}$ min must be long enough to ensure that inrush is complete before PD enables MDI power
  - Worst case spread occurs for 24V unregulated class where V_{on} min is 10.26V and V_{PSE} max is 36V.
  - Propose setting $T_{powerdly}$ max = 1.22 × $T_{powerdly}$ min and making it uniform for all power classes

Proposed Changes to Baseline Text for V_{on} and $T_{powerdly}$

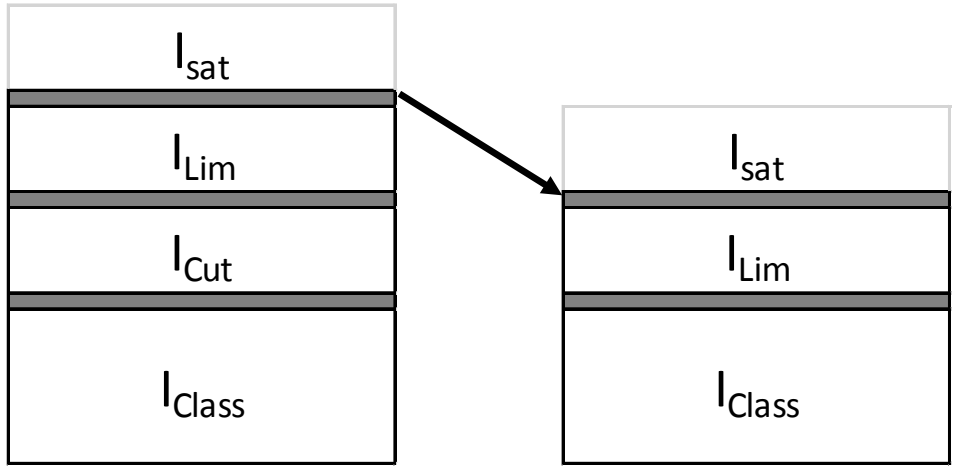
- 104.4.6.1 PD input voltage
  - The PD shall turn on at a voltage less than or equal to V_{On} after a delay in the range of t_{power_dly} as specified in Table 104–6. The PD shall turn off at a voltage greater than or equal to V_{Off}.
  - The PD shall turn on or off without startup oscillation and within the first trial for any valid load value when fed by V_{Port_PSE} min to V_{Port_PSE} max (as defined in Table 104-1) with a series resistance within the range of valid channel resistance.

What's currently in the draft for I_{CUT} and I_{LIM}?

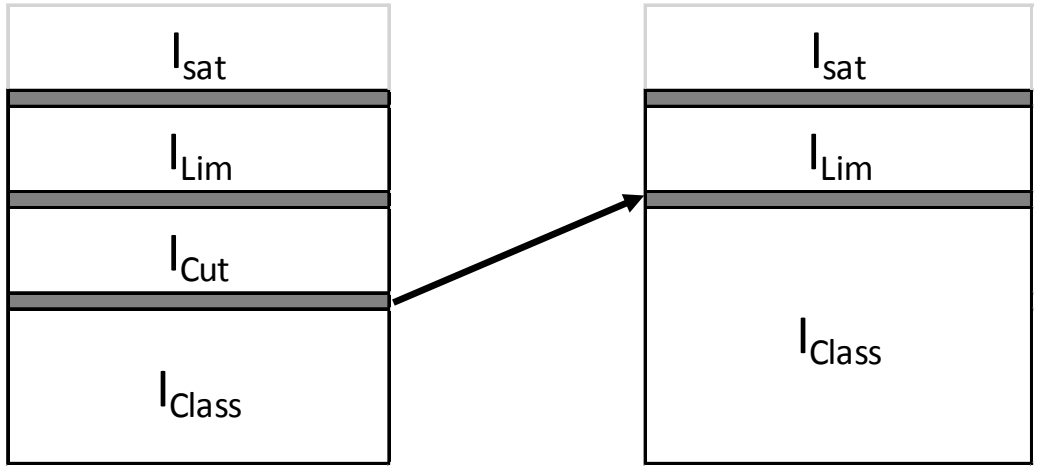
- I_{CUT} and T_{CUT}
  - I_{CUT} range is P_{Class}/V_{PSE} to $2PClass/V_{PSE}$
  - T_{CUT} range is 50ms to 75ms
  - The cumulative duration of T_{CUT} is measured using a uniform sliding window of at least 1s width
  - Power shall be removed if the PSE current exceed I_{CUT} for longer than T_{CUT}
- I_{LIM}
  - I_{LIM} is listed in the Table 104-3 with a TBD limit.
  - There is no sub-clause which describes I_{LIM}.

What do we really need for overcurrent protection?

- For PoDL, class current comes at premium because of the technical challenges and relative cost associated with higher saturation current in the coupling inductors.
- Consequently, we want to minimize any overhead pertaining to over-current protection.
- Instead of specifying both I_{CUT} and I_{LIM} why not just specify I_{LIM}?



Lower I_{Sat} for a given I_{Class} or…



…more I_{Class} for a given I_{Sat}

Proposed Changes to Baseline Text for Output Current cont'd

- Add 104.3.6.2.3 - Output current – at short circuit condition
  - During operation in the POWER_ON state, the PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104-3.
  - If I_{Port} exceeds I_{LIM} min during the POWER_ON state, the PSE output voltage may drop below $V_{PSE(PON)}$ min.
  - During operation in any other state when the PSE is enabled, the PSE shall limit I_{Port} to less than I_{SC} as specified in Table 104-2 for a duration of up to T_{LIM}.
  - If the PSE is limiting current in the POWER_ON state or any state when V_{Sleep} is applied at the PI, power removal from the PI shall begin within T_{LIM}.
  - Measurements of I_{Port} during a short circuit condition shall be made 1ms after the initial transient to allow for settling.
- ~~104.3.6.4 Overload current~~
  - ~~If I_{PORT}, the current supplied by the PSE to the PI, exceeds I_{CUT} for longer than T_{CUT}, the PSE may remove power from the PI. The cumulative duration of T_{CUT} is measured using a uniform sliding window of at least 1 second width.~~

Proposed Changes to Table 104-2

Item	Parameter	Symbol	Unit	Min	Max	Additional Information
3	Valid test probe current	I_{valid}	mA	~~4~~ TBD	10	
5	Output capacitance during detection and classification	C_{out}	nF		~~1~~ 200	
6	Detection timing	T_{det}	ms		TBD	
10	Signature hold time	T_{vsig_hold}	ms	TBD		

Proposed Changes to Table 104-3

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional Information
3	Output voltage dV/dt	dV_{PSE}/dt	V/ms		~~20~~ *TBD*	All	A	See 104.3.6.1
~~5~~	~~Overload current detection range~~	~~I_{CUT}~~	~~A~~	~~P_{Class} / V_{PSE}~~	~~$2xP_{Class}$ / V_{PSE}~~			~~See 104.3.6.4~~
~~6~~	~~Overload time limit~~	~~T_{CUT}~~	~~s~~	~~0.050~~	~~0.075~~			~~See 104.3.6.4~~
~~7~~ 5	Output current – at short circuit condition	I_{LIM}	A	~~TBD~~ $I_{PI\_Class(max)}$	~~TBD~~ $1.22 \times I_{PI\_Class(max)}$			~~See 104.3.6.4~~ See 104.3.6.2.3
6	Short circuit time limit	T_{LIM}	s	0.050	0.075			See 104.3.6.2.3
~~6~~	~~Inrush time~~	~~T_{inrush}~~	~~s~~	~~*TBD*~~				~~See 104.3.6.6~~
8	Maximum inrush time	T_{inrush_max}	s	*TBD*	*TBD*			See 104.3.6.2.2
10	Maximum classification time	T_{class}	ms	300	366			See 104.3.5
17	Wakeup current hold time for validity	T_{Wakeup}	ms	~~1~~ *TBD*				See 104.3.6.5.1

Proposed changes to Table 104-6

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
4a	Power supply turn on voltage (unregulated 12 V classes)	V_{on}	V	5.18	5.75		See 104.4.6.1
4b	Power supply turn on voltage (regulated 12 V classes)			12.2	13.6		
4c	Power supply turn on voltage (unregulated 24 V classes)			10.3	11.4		
4d	Power supply turn on voltage (regulated 24 V classes)			17.8	24.7		
~~4e~~	~~Power supply turn on voltage (unregulated 48 V classes)~~				~~22.8~~		
4f~~e~~	Power supply turn on voltage (regulated 48 V classes)			38.4	45.6		
7	Inrush enable delay time	$t_{powerdly}$	ms	1.46	1.78		

Proposed changes to Table 104-6 con’td

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
6a	Input capacitance during detection and ~~classification states~~ inrush	C_{PD}	uF		*TBD*		
6b	Input capacitance during classification		µF		0.2		

Conclusion

- Remedies for missing portions in draft 1.3 pertaining to detection, inrush, and current limit were presented.
- Remaining TBDs need to be addressed by gardner_3bu_2_1015.

Questions?