Detect and Inrush Timing

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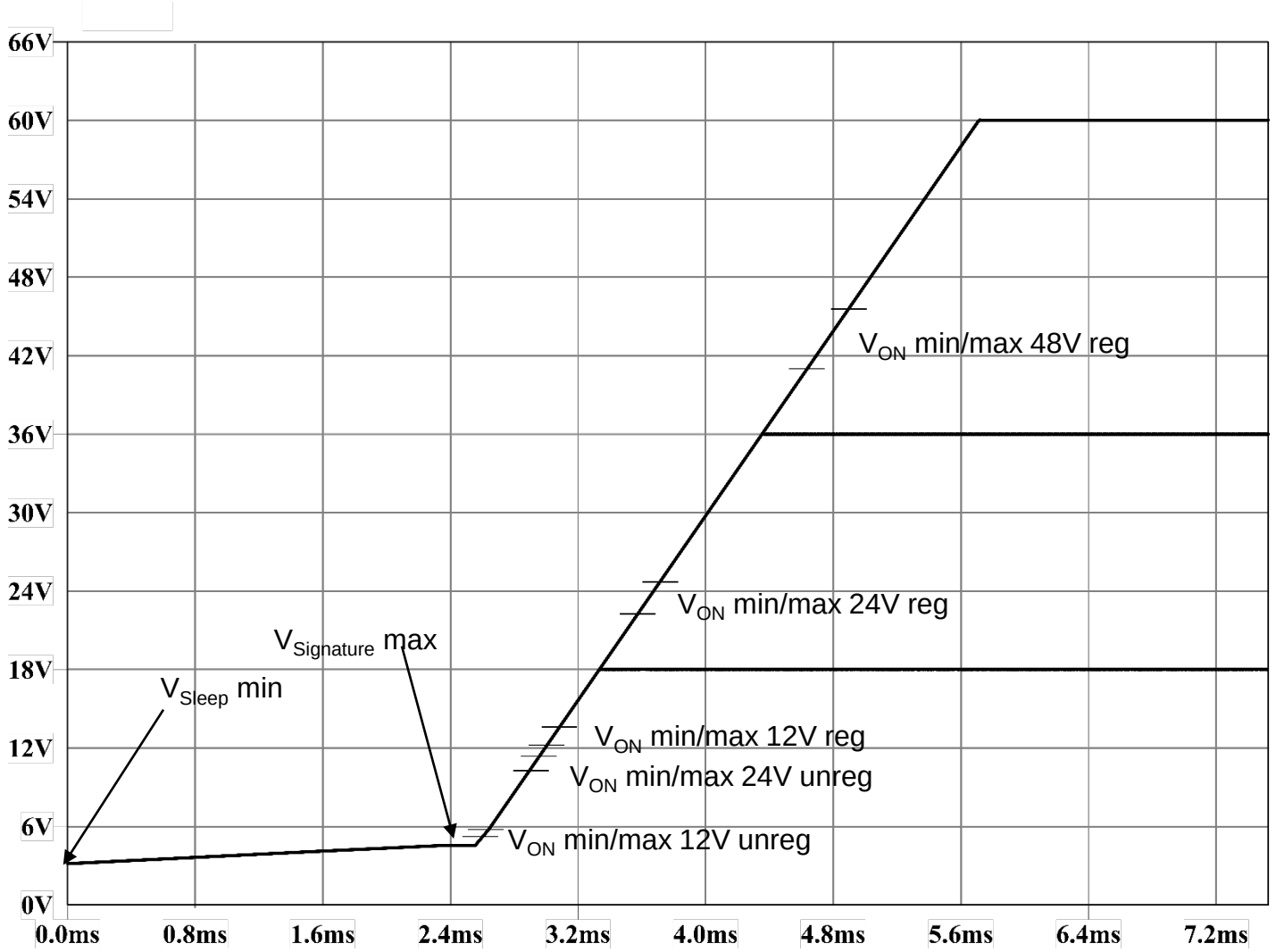
Presentation Objectives

- Present an analysis of worst case timing for detection and inrush
- Propose values for I_{detect}, T_{det}, dV_{PSE_inrush}/dt, I_{inrush}, T_{inrush}, T_{inrush_max}, C_{PD} max during inrush, and $T_{powerdly}$.

Assumptions for Fast Start-Up Delay Analysis

- PI is pre-biased at V_{sleep} min
- PD V_{sig} at max value (4.55V)
- I_{detect} is at minimum value (suggest 8mA)
- C_{PSE} is at its maximum value (suggest 200nF)
- C_{PD} is at its maximum value (suggest 10µF)
- dV_{PSE}/dt is 20% below the max
  - 17.6V/ms =0.18A/(10µF+200nF)
- $T_{powerdly}$
  - Has to be long enough to allow inrush to complete, based on maximum delta between max V_{PSE} and min V_{on} which occurs for the unregulated 24V class
  - Same value is used over all power classes for simplicity
  - Worst case power-up delay occurs for V_{on} max

Worst Case V_{PD} Power-Up Waveforms



Turn-on time delays

	12 unreg	12 reg	24 unreg	24 reg	48 reg
tdetect,max	2.55E-03	2.55E-03	2.55E-03	2.55E-03	2.55E-03
tinrush	7.91E-04	7.91E-04	1.81E-03	1.81E-03	3.17E-03
tpower_delay,min	7.27E-04	3.26E-04	1.46E-03	7.80E-04	1.07E-03
tpower_delay,max	1.78E-03	1.78E-03	1.78E-03	1.78E-03	1.78E-03
total	4.43E-03	4.87E-03	4.75E-03	5.50E-03	6.68E-03
iprobe, min	0.008	0.008	0.008	0.008	0.008
iinrush,min	0.18	0.18	0.18	0.18	0.18
Vsleep,min	3.15	3.15	3.15	3.15	3.15
Vsig,max	4.55	4.55	4.55	4.55	4.55
Vsig,min	4.05	4.05	4.05	4.05	4.05
Von,max	5.75	13.6	11.4	24.7	45.6
Von,min	5.175	12.24	10.26	22.23	41.04
VPSE,max	18	18	36	36	60
VPSE,min	6	14.4	12	26	48
CPD,max	1.00E-05	1.00E-05	1.00E-05	1.00E-05	1.00E-05

Proposed Values for D1.4

- V_{on} min = 90% of Von max
- C_{PD} max during detect and inrush: 10µF
- C_{PD} max during classification: 200nF
- I_{valid} min: 8mA
- T_{det} max: 3.11ms
- T_{Wakeup} min: 100µs
- T_{vsig_hold} min: 100µs
- Type A dV_{PSE}/dt max: 22 V/ms
- T_{inrush_max}: 3.17ms to 3.87ms
- $T_{powerdly}$: 1.46ms to 1.78ms

Questions?