Control and Status Registers

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- Clause 33 has PSE registers for control & status
- Enabling Clause 30 management is easier if we define registers
- Registers provide a ready, standardized diagnostic interface
- Approach: follow pattern of registers used in Clause 33
  - Keep it simple
  - LH bits to indicate faults (e.g., overload) vs. counters
  - Consequence: increment timing needs to be <= about 2/sec
- Recommend: Make restart_time due to failure escapes ~0.4-0.5sec, so that monitoring restarts can be done with 1 bit rather than a counter in the register

Where to put Registers?

- Clause 33 used Clause 22 register space
  - So, the registers are actually specified in Clause 33
  - BUT: Clause 22 register space is full!
- BASE-T1 PHYs use Clause 45 registers
  - Registers are defined in Clause 45, with all the other registers
  - Systems using BASE-T1 will likely use Clause 45 management
- CHOICE: Define Clause 45 registers for PoDL
  - BUT – Clause 45 doesn't really have an appropriate register class for power (not PMA/PMD, PCS, PHY XS, TC, or AutoNeg)
- CHOICE:define a new MDIO Manageable Device (MMD): 'Power Unit'
  - Scalable and can coexist with PHYs to be defined

New Power Unit MMD: 12

Change reserved row m.5.15:12 and insert row to add Power Unit Registers in Table 45-2 as shown, below reserved row m.5.15:12 for and immediately above row for register m.5.11 (unchanged rows not shown):.

Table 45–2—Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.5.15:~~12~~ 11	Reserved	Value always 0	RO
m.5.12	Power Unit present	1 = Power Unit present in package 0 = Power Unit not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read only

- Allows Power Unit to be managed alongside of PHYs
  - Could be used for new Clause 33 or other power devices too

Single-Pair PSE Control Register

Table 45–211f—Single-Pair PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
12.0.15:3	Reserved	Value always 0	RO
12.0.2	Enable Power Classification	1 = Power classification enabled 0 = Power classification disabled	R/W
12.0.1:0	PSE Enable	1 1 = Reserved 1 0 = Reserved 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

Single-Pair PSE Status 1 Register

Table 45–211g—Single-Pair PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
12.1.15	Power Removed	1 = Power has been removed due to fault 0 = Power has not been removed	RO/ LH
12.1.14	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.1.13	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.1.12	Class Timeout	1 = Classification timeout condition detected 0 = No Classification timeout condition detected	RO/ LH
12.1.11	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.1.10	MFVS Absent	1 = MFVS absent condition detected 0 = No MFVS absent condition detected	RO/ LH
12.1.9:7	PSE Type	1 x x = Reserved 0 1 1 = Reserved 0 1 0 = Type A+B PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO

Single-Pair PSE Status 1 Register (continued)

Table 45–211g—Single-Pair PSE Status 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
12.1.6:3	PD Class	1 1 x x =Reserved 1 0 1 x =Reserved 1 0 0 1 =Class code 9 1 0 0 0 =Class code 8 0 1 1 1 =Class code 7 0 1 1 0 =Class code 6 0 1 0 1 =Class code 5 0 1 0 0 =Class code 4 0 0 1 1 =Class code 3 0 0 1 0 =Class code 2 0 0 0 1 =Class code 1 0 0 0 0 =Class code 0	RO
12.1.2:0	PSE Status	1 1 x = Reserved 1 0 1 = Reserved 1 0 0 = Error 0 1 1 = Searching 0 1 0 = Delivering power 0 0 1 = Sleeping 0 0 0 = Disabled	RO

[a]RO = Read Only, LH = Latched High

Single-Pair PSE Status 2 Register

Table 45–211h—Single-Pair PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
12.2.15:3	Reserved	Value always 0	RO
12.2.2:0	PD Type	1 x x = Reserved 0 1 1 = Reserved 0 1 0 = Type A+B PD 0 0 1 = Type B PD 0 0 0 = Type A PD	RO

[a]RO = Read Only, LH = Latched High

Mappings to Clause 30 Elements

REGISTER FIELD	MANAGEMENT FIELD
PSE Enable:	aPoDLPSEAdminState,
Enable Power Classification:	**(NONE)**
Power Removed:	aPoDLPSEPower DeniedCounter
Valid Signature:	**(NONE)**
Invalid Signature:	aPoDLPSEInvalidSignatureCounter
Overload	aPoDLPSEOverLoadCounter
MFVS Absent:	aPoDLPSEMaintainFullVoltageSignatureAbsentCounter
PSE Type:	aPoDLPSEType
PD Class	aPoDLPSEDetectedPDPowerClass
PSE Status:	aPoDLPSEPowerDetectionStatus
PD Type	aPoDLPSEDetectedPDType
Class Timeout:	aPODLPSEInvalidClassCounter
(NONE):	aPODLPSEActualPower, PoDLPSEPowerAccuracy, aPoDLPSECumulativeEnergy

Thank You!

See posted draft text in private area for more information