Power Matters

Microsemi

IEEE802.3bu
PoDL Requirements Derived from System Model

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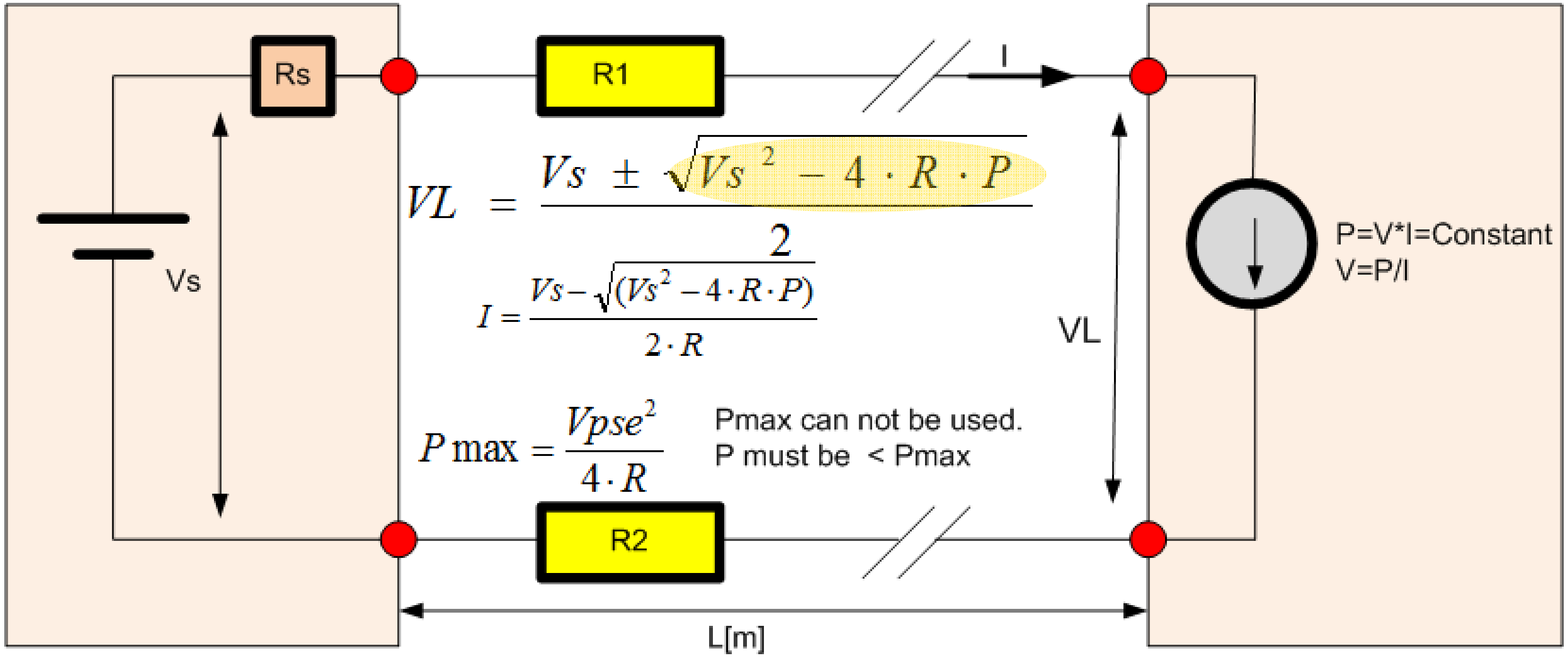
Microsemi

Objectives

- *To discuss a list of requirements from PSE and PD in automotive applications that are derived from The General Case of Remote Power Feeding Model.*
  - *Ensuring system stability*
    - *PD Under Voltage Lock Out (UVLO)*
    - *Source voltage vs. Wire size and Load power*
  - *Optimization of wire size vs. system parameters*
  - *Different PSE voltages vs. Single voltage*
    - *The need for classification*
    - *Compensation of wire drop*
    - *Addressing cold crank*
  - *Active current limit in PSE vs. Fuse*
    - *Wire optimization*
    - *Transformer core optimization*
    - *Stability*
    - *Protection against excess energy in Inductor interface or during faults*
  - *Reporting of faults*

System Power Model – The general case

- Rs=Power Source output resistance
- L= Cable length with a resistance of Rc=R1+R2=Cable round loop resistance
- R=Total loop resistance=Rs+R1+R2 is the actual source output resistance of the voltage source Vs.



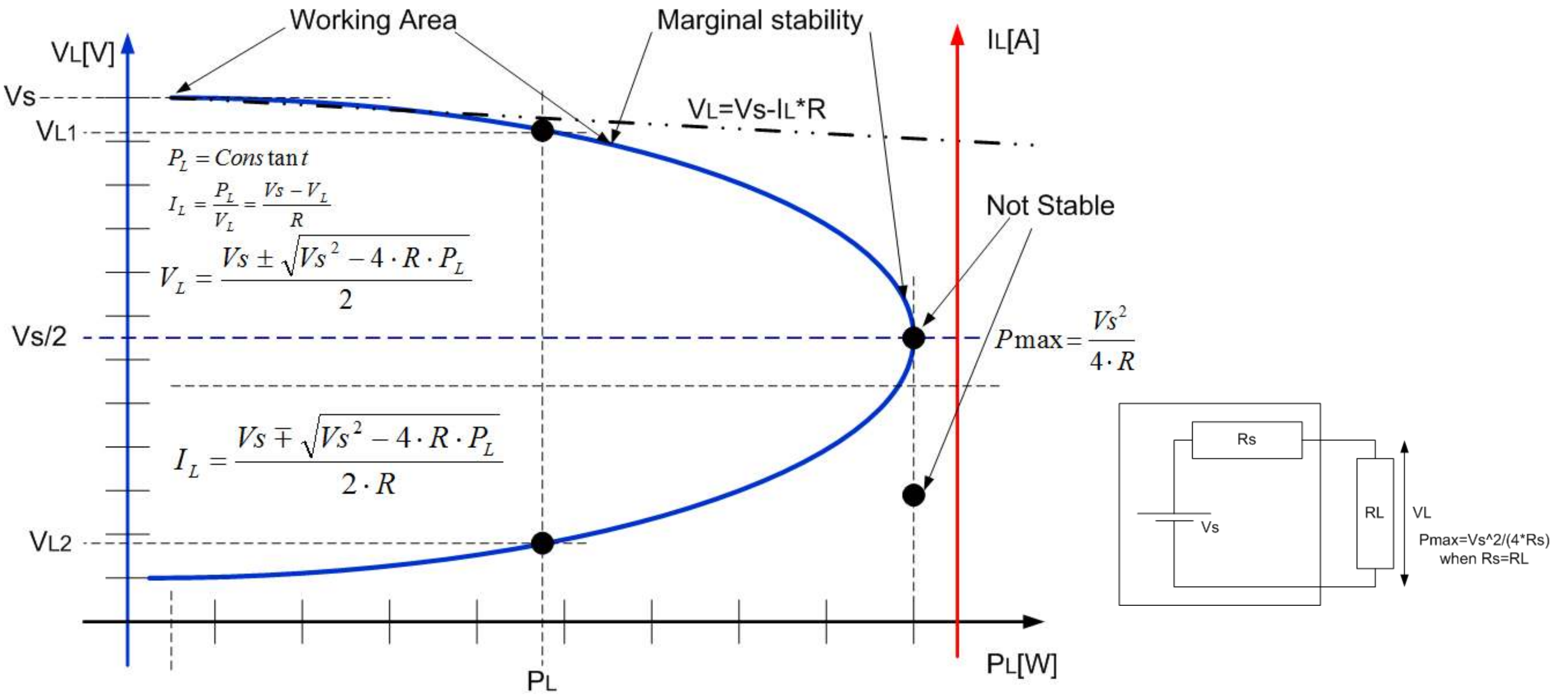
$$VL = \frac{Vs \pm \sqrt{Vs^2 - 4 \cdot R \cdot P}}{2}$$

$$I = \frac{Vs - \sqrt{(Vs^2 - 4 \cdot R \cdot P)}}{2 \cdot R}$$

$$P\max = \frac{Vpse^2}{4 \cdot R}$$

If $Vs^2 >> 4*R*P_L$ than VL=~Vs as we used too or in general $V_L = Vs - I*R$.
So if it is working for you, it is understood why based on the model above.

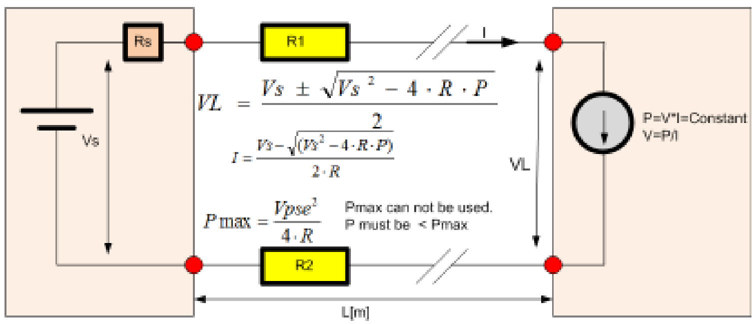
Ensuring system Stability – Working on upper curve

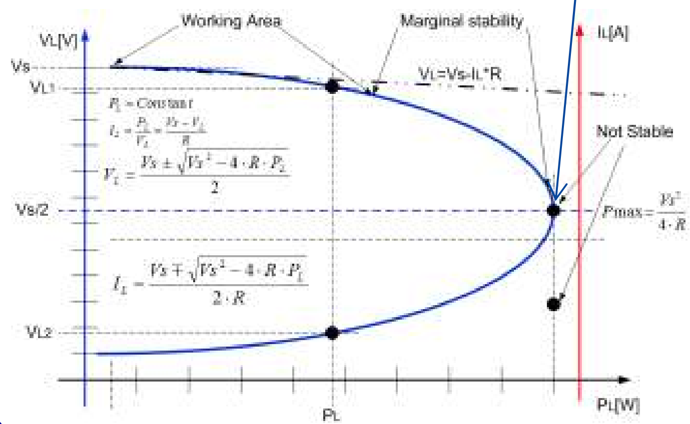


- The above curve shows:
  - Two solutions for VL for given PL. We must work on the higher VL value curve.

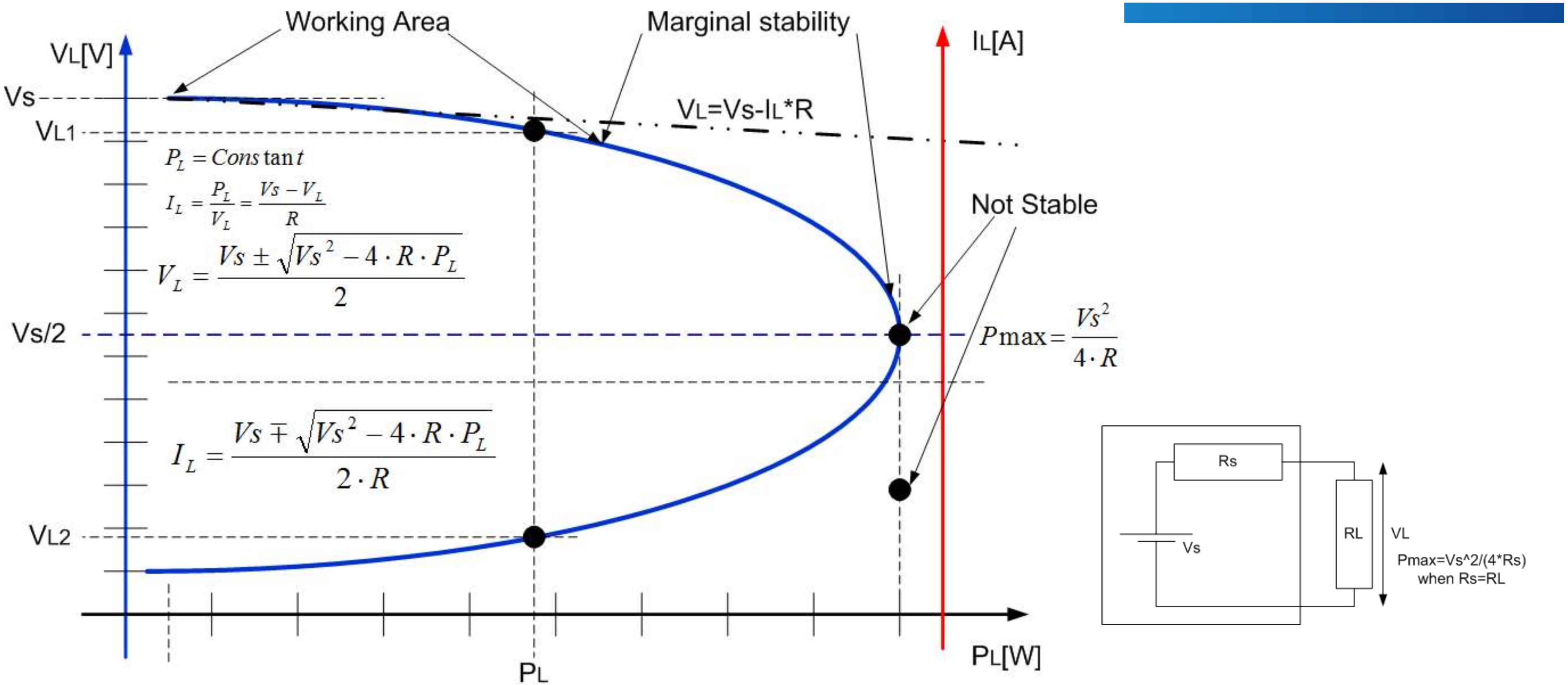
Ensuring system Stability - Example

- If operation is required at:
  - Vbat=Vs= 9V min. AND
  - 15m cable with 0.126Ω/m wire AND Rs=0.2 Ω (add 40% to the resistance at 125°C from 20 °C) AND Load input power PL is 4W
- Then:
  - R=2*15m* 0.126Ω/m *1.4+0.2 Ω=~5.5 Ω
  - (Vs^2-4*R*PL)^0.5=(9^2- 4*5.5 Ω *4W)^0.5=(-7)^0.5 negative root ➔ VL below stability point and will stay there ➔ will not work.
  - **Remedy:**
  - **Reduce load or Cable length OR Increase Vs or wire diameter**





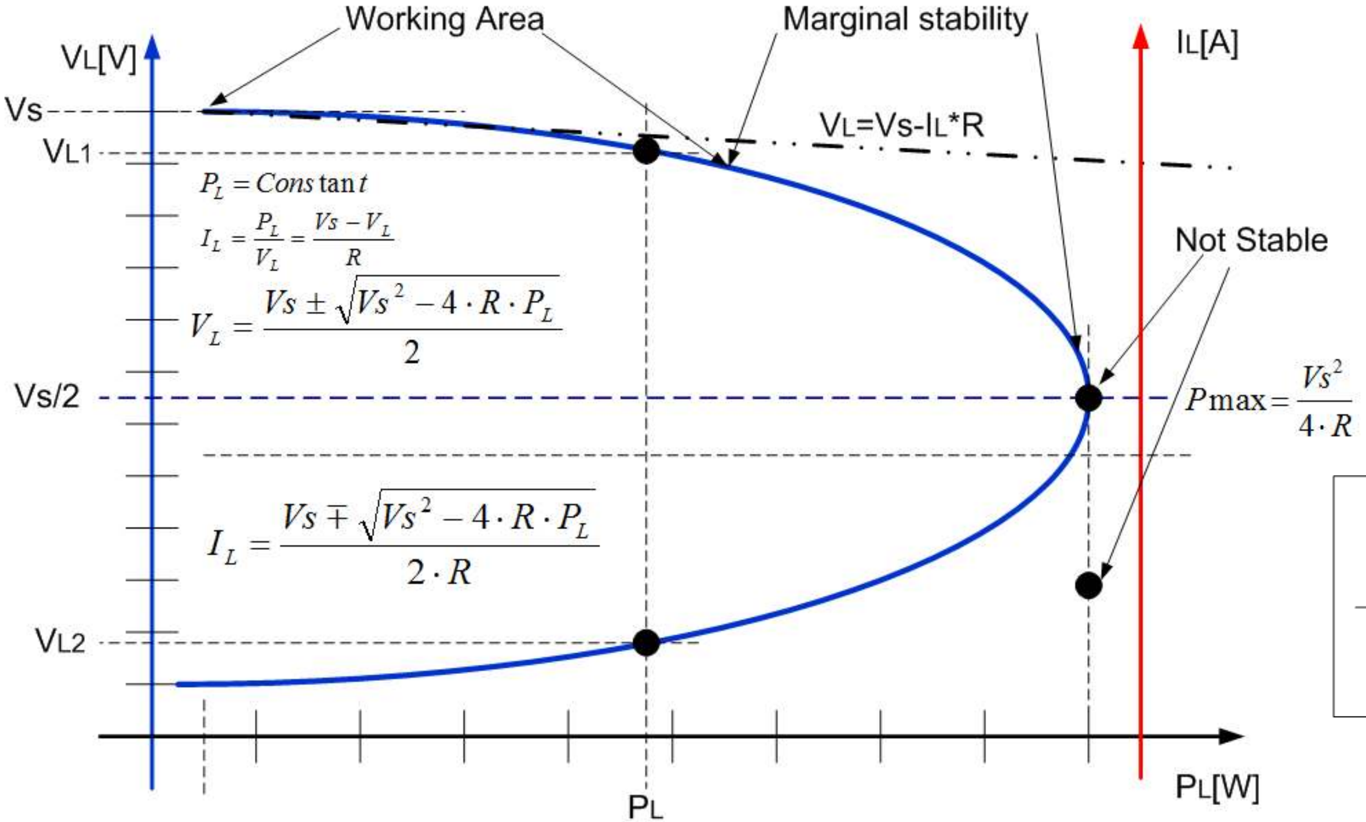
Ensuring system Stability – Why UVLO is required?

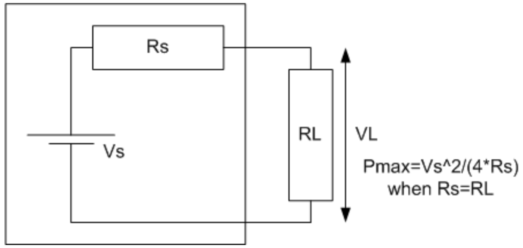


- The above curve shows:
  - **Why UVLO is a must at DC/DC on load side?**
    - **To ensure staying at upper value during startup and bus transient voltages**
    - **PD starts to work at Von**
    - **PD is OFF at Voff**
    - **Von>Voff**

Ensuring system Stability–Minimum source Voltage

Source voltage vs. Wire size and Load power



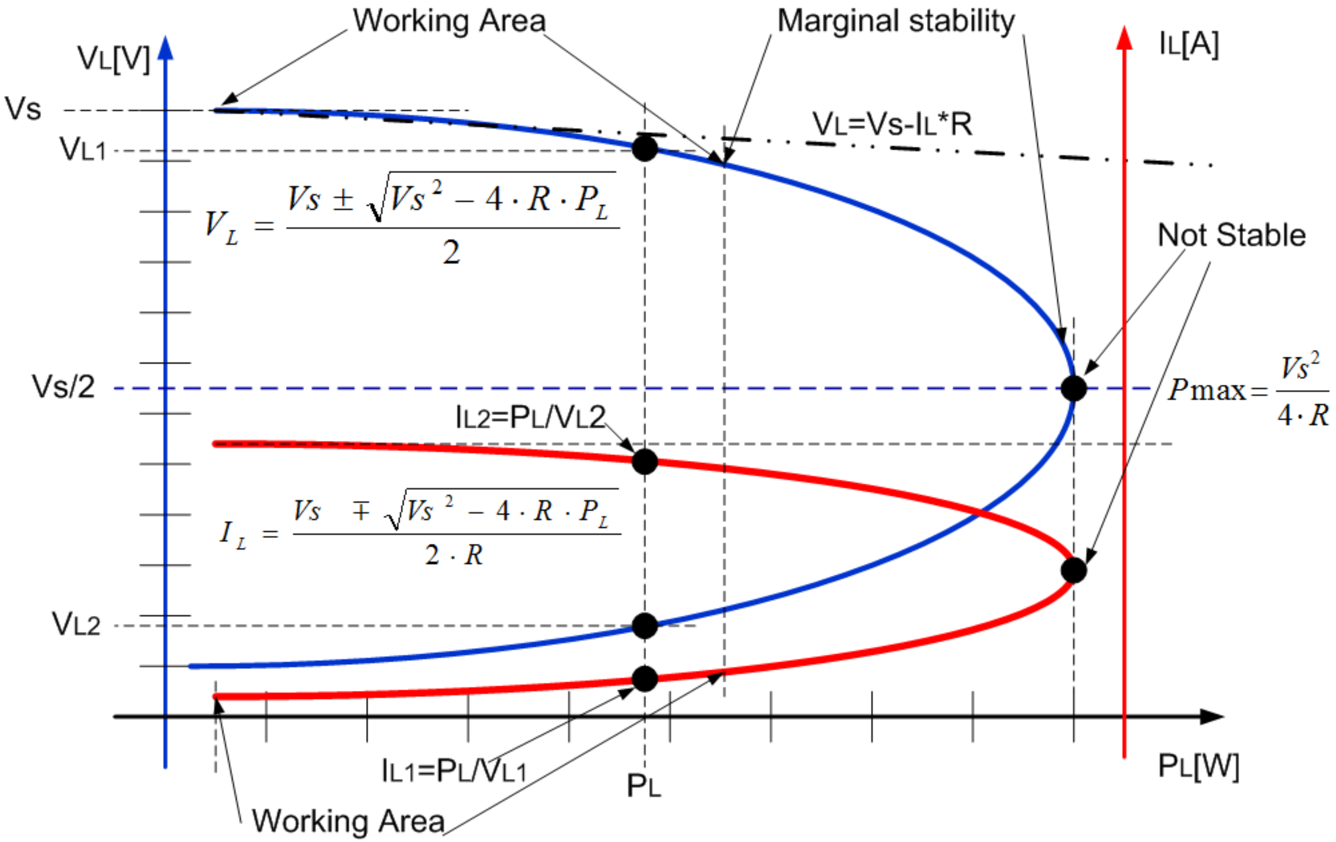


- To be in stable operating point we need: $Vs^2 - 4 \cdot R \cdot P_L > 0$
- As a result, Minimum source voltage is: $Vs > \sqrt{4 \cdot R \cdot P_L}$
- Different Vs for different loads and wire resistance

Ensuring system Stability

Why UVLO in a PD is a must.

Why current limit protection (preferred active one) is required.



Adding the load current plot vs. load power.

- The above curve shows:
  - **Why UVLO is a must at DC/DC on load side – we already answer it.**
  - ***We must work on the "negative" solution of IL hence***
    - ***UVLO at the PD is a must***
    - ***Current limiter is recommended (in addition to other faults)***
    - ***Allows wire size optimization and adaptation to different source voltages***

Optimization of wire size vs. system parameters

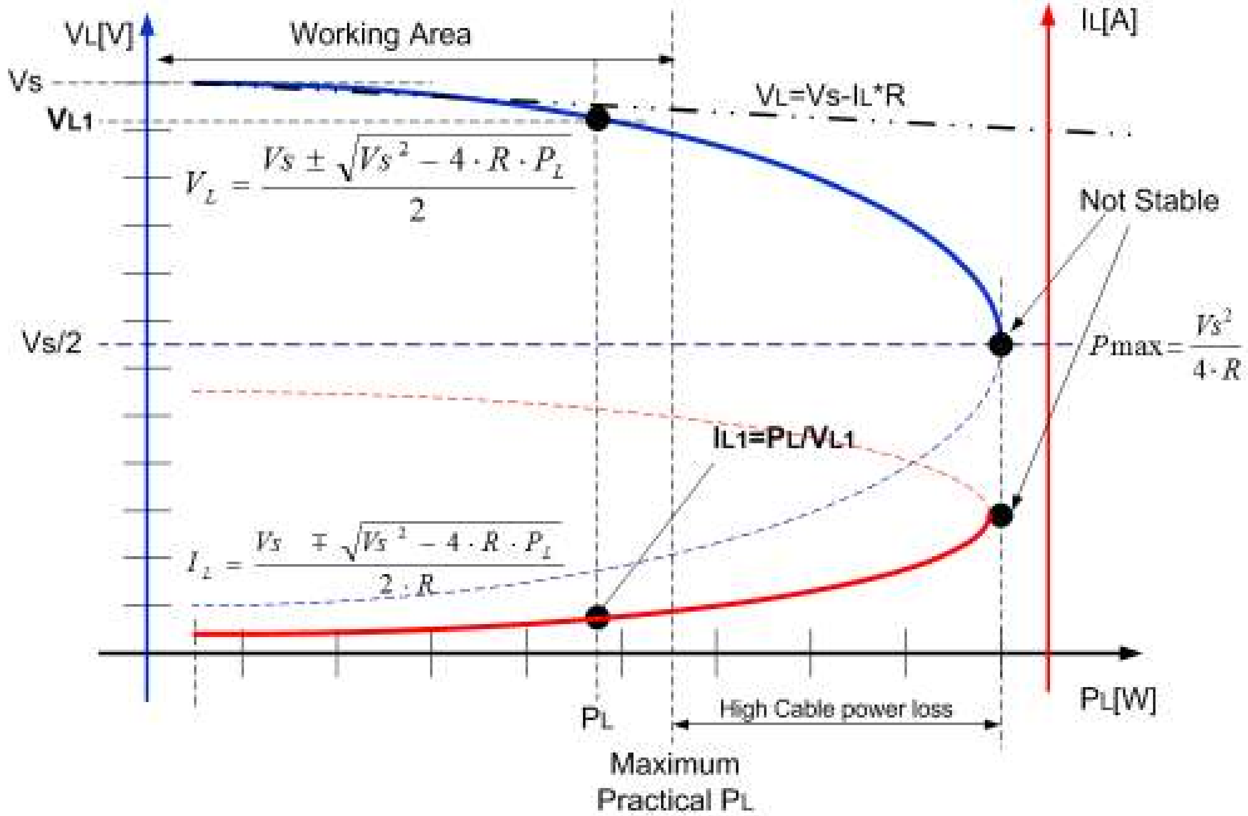
- There is an objective to use less copper ➔ lower weight etc.
- Wire size can be optimized by:

$$R < \frac{Vs^2}{4 \cdot P_L}$$

- In order to protect infrastructure and equipment we can use Fuse or active current limit.
  - Fuse need high margin from nominal working current.
  - Active current limit
    - automatic reset
    - easy testing
    - Programmable per power/voltage class
    - Easy fault reporting

System Stability – Maximum load power

- Our working area for any use case with DC/DC at the load



- PL_practical < Pmax =Vs^2/(4*R) ➔ Vs_min>(4*R*PL_practical)^0.5
- How to exactly determine Vs_min? <u>See design equations next slides</u>
- Active Current limiter device between source voltage and load is recommended

How to exactly determine PL_practical and Vs_min?

- The not optimized way. We use large wire diameter, reducing R.
  - $4*R*P_L << Vs^2$, ➔ $P_L <<$ Pmax. Equation converge to simple $V_L = Vs - IL*R$. All is working.
- For optimizing the cable size, weight and cost
  - $4*R*P_L < Vs^2$, ➔ $P_L <$ Pmax, but were exactly?
  - The analytical way is to limit cable power loss, Pc. so $K = P_L/Ps = P_L/(P_L+Pc)$ (Load/Source power ratio) will be lower than 80%. Typical $K \geq 0.8$ is reasonable.
  - Set $Pc \leq PL*(1/K-1)$.
  - Once Pc is set, I_L can be derived $(Pc/R)^{0.5}$ and then the rest of system parameters. In this way, PL will be below Pmax.
- There are other optimization methods. All of them will results with similar/close results.
- See annex A for detailed optimization derivation

Vs_min vs. PL and cable length

Ppd_in	1	1.5	2	3	4	5	6	7	8	9	10
L=3.5	4.2	5.1	5.9	7.3	8.4	9.4	10.3	11.1	11.9	12.6	13.3
L=15	7	8.6	10	12.2	14	16	17.3	18.7	20	21.2	22.3
L=40	11	13.4	15.5	19	22	24.4	26.8	28.9	31	32.9	34.6

Table 1: Vs_min v.s. Cable length and PD input power. Vs_min=9V area is enclosed with red dashed line.

Ppd_in	1	1.5	2	3	4	5	6	7	8	9	10
L=3.5	4.2	5.1	5.9	7.3	8.4	9.4	10.3	11.1	11.9	12.6	13.3
L=15	7	8.6	10	12.2	14	16	17.3	18.7	20	21.2	22.3
L=40	11	13.4	15.5	19	22	24.4	26.8	28.9	31	32.9	34.6

Table 2: Vs_min v.s. Cable length and PD input power. Vs_min=16V area is enclosed with red dashed line.

For a wire with 0.126Ω/m, k=0.85:

- 16V minimum will support all power range at L=3.5m, 5W at L=15m and 2W at L=40m (Table 2)
- Above 9V, a DC/DC is required to boost voltage for PL>4W (Table 1)

Different PSE voltages vs. Single voltage

- *We need design flexibility and system cost optimization*
- *We saw that for different sets of load power and wire resistance we need different minimum source voltage for:*
  - *Ensuring stability*
  - *Compensation of wire drop*
  - *Addressing cold crank scenarios*

- *It generate the need for classification*
  - *Classification may be implemented by L1 methods or*
    - *Low frequency single wire communication type.*
      - *See example at : http://www.ieee802.org/3/bu/public/sep14/gardner_3bu_1_0914.pdf*

Active current limit in PSE vs. Fuse

- Active current limit helps with:
  - Wire optimization
  - Transformer core optimization
  - Stability
  - Protection against excess energy in Inductor during transient events / loose connection or other faults.

Reporting of faults

- To be discuss the need for fault reporting and the means to do it.

Conclusions

- UVLO at load side DC/DC is a must (Von>Voff)
- Active Current Limiter at the power source side is highly recommended for:
  - Reliable deterministic and controlled operation
  - Optimized cable diameter, transformers etc. and not oversized it
- Different minimum source voltage is needed to be guaranteed for a given load power and cable resistance (length, diameter).
  - As a result classification function is required for cost optimization.
- The need and the means for faults report need to be discussed.

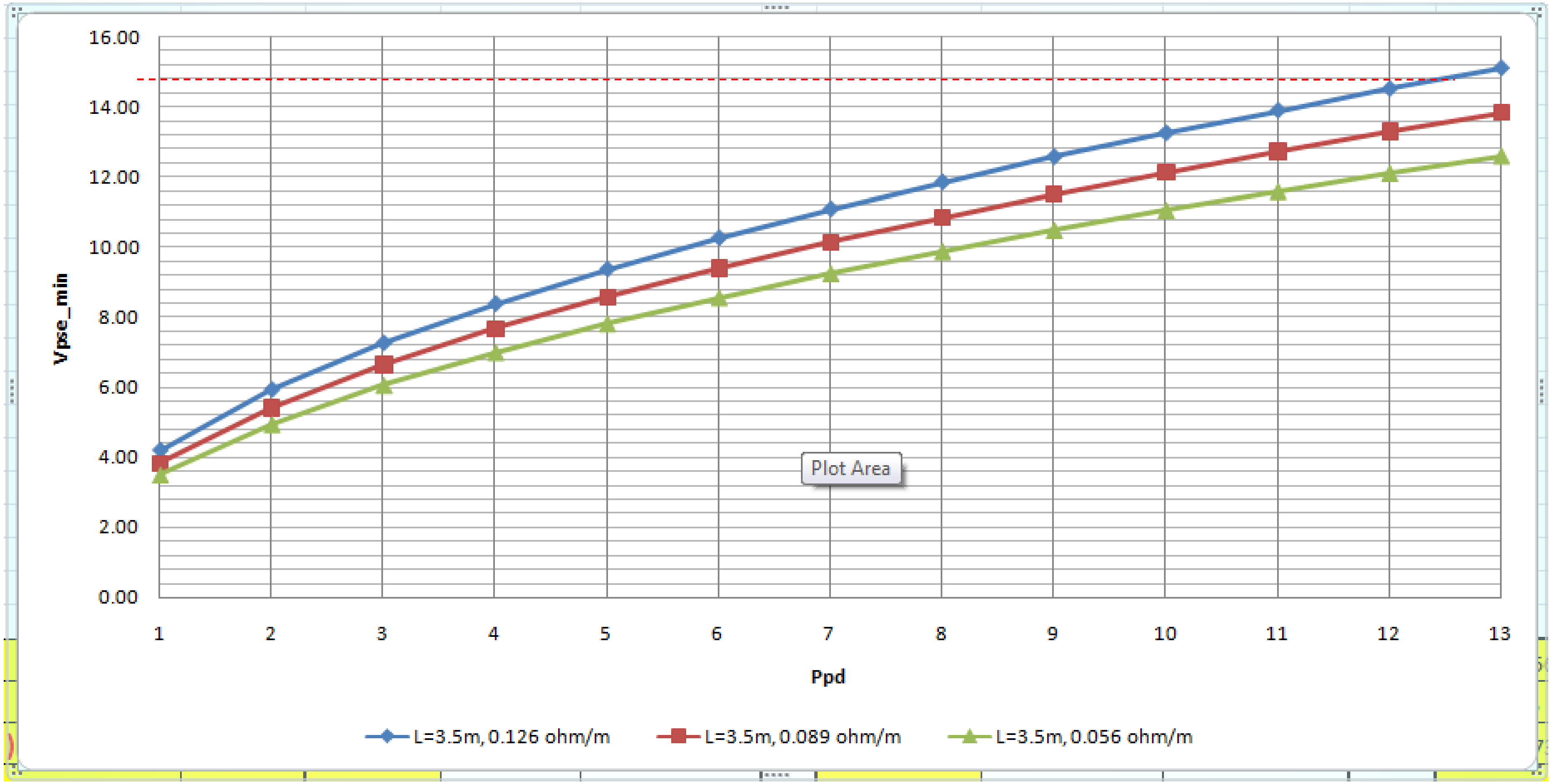
Backup slides

Annex A: Calculation Procedure – Vs_min derivation

- R=Total Round Loop cable resistance including source resistance
- PL is the power measured at the input of the load. It is already include DC/DC efficiency and the load connected to the DC/DC.
- Pc is the maximum cable power loss. It sets $K=P_L/Ps=P_L/(P_L+Pc)$ to be <0.8. This is a realistic number and normally required. (K is not DC/DC efficiency!). Limiting Pc ensures Load voltage VL>Vs/2 for stable operation (See curves in previous slides).
- As a result, for given K we can compute Pc directly from maximum load power P_L. $K=P_L/Ps$. $K=P_L/(P_L+Pc)$. ➔ $Pc=P_L*(1/K-1)$.
- R and Pc are known hence maximum channel DC current can be computed: Pc=R*I^2 ➔ I_max=(Pc/R)^0.5
- Minimum load voltage can be calculated since $P=V_L*I$ ➔ $V_L\_min=P_L/I$
- The minimum source voltage can be calculated :$Vs\_min=V_L\_min+I*R$
- Design margins and temperature effects are not included above. To address it, it is required to set R at maximum system operating temperature and add additional design margin (10%) to the resultant Vs_min to account for +/-5% power supply tolerance.

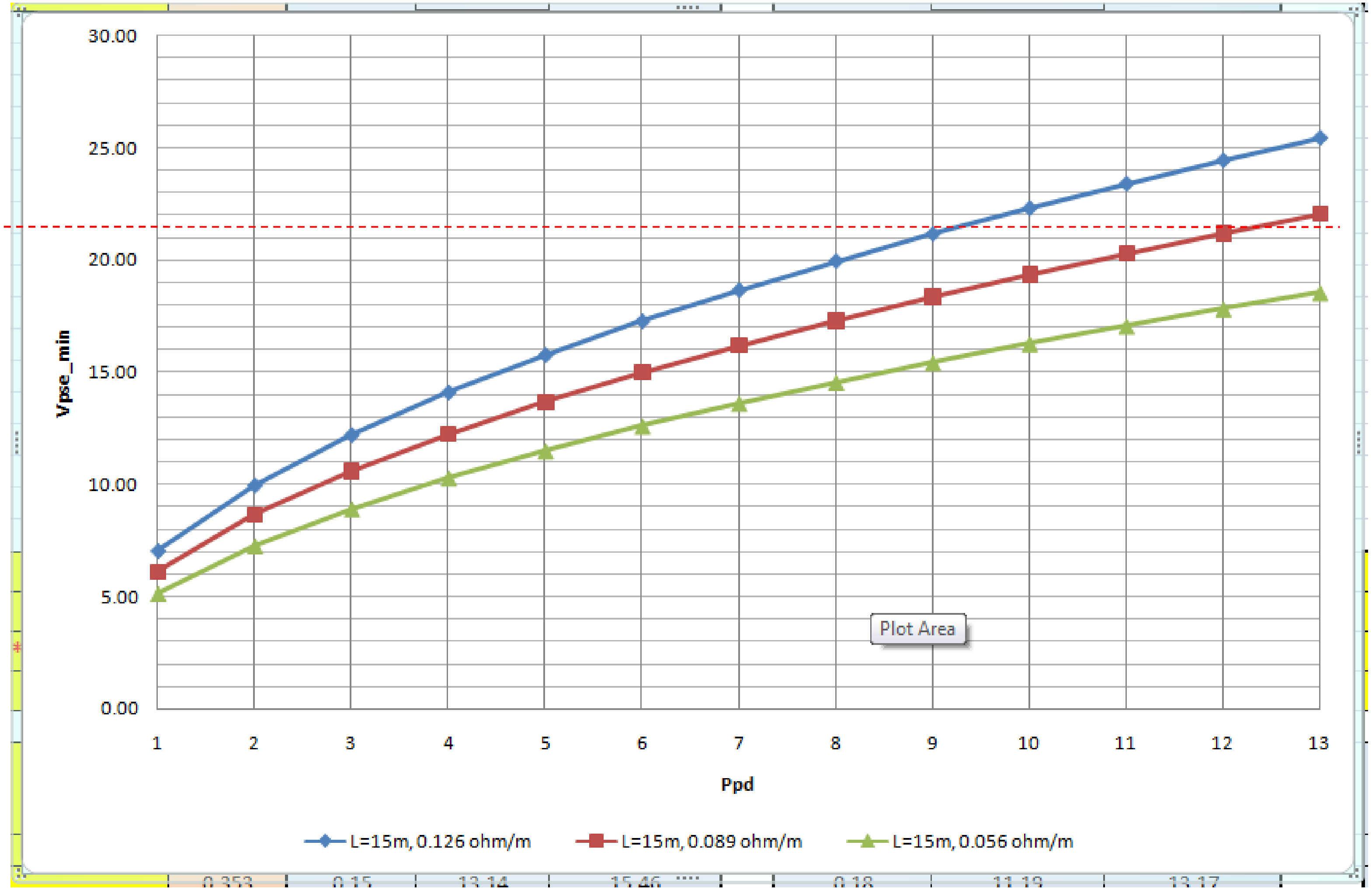
Vs_min for L=3.5m with 0.05, 0.089, 0.126 Ω/m wire vs. load power Ppd=PL

The following slides show the requirements for minimum source voltage required to supply load power (Ppd=PL) for given wire size and cable length.



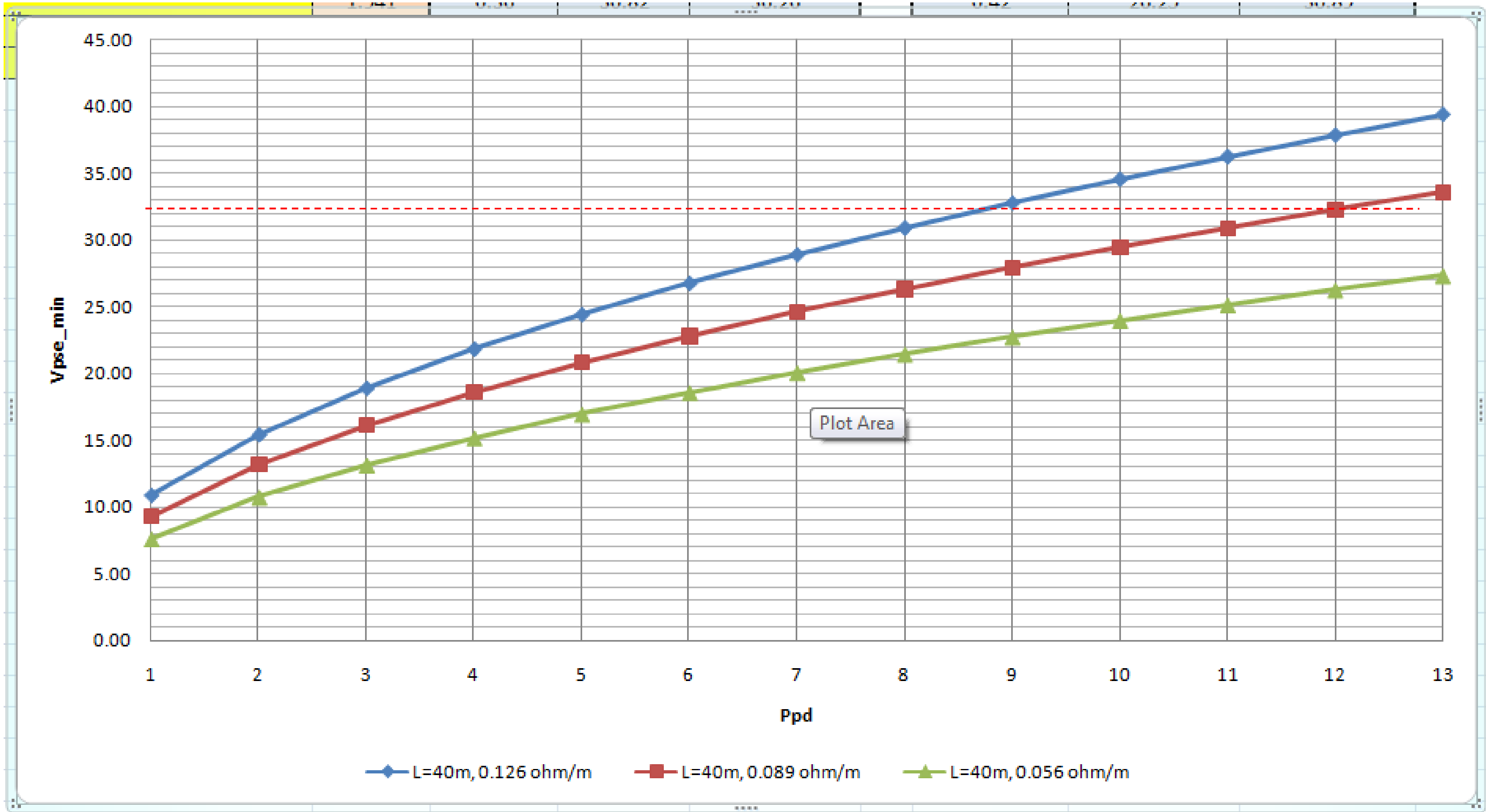
TA=125°C. k=0.85. Ppd=PL is measured at the device input which reflects sensor power and its DC/DC efficiency.

Vs_min for L=15m with 0.05, 0.089, 0.126 Ω/m wire vs. load power Ppd=PL



TA=125°C. k=0.85. Ppd=PL is measured at the device input which reflects sensor power and its DC/DC efficiency.

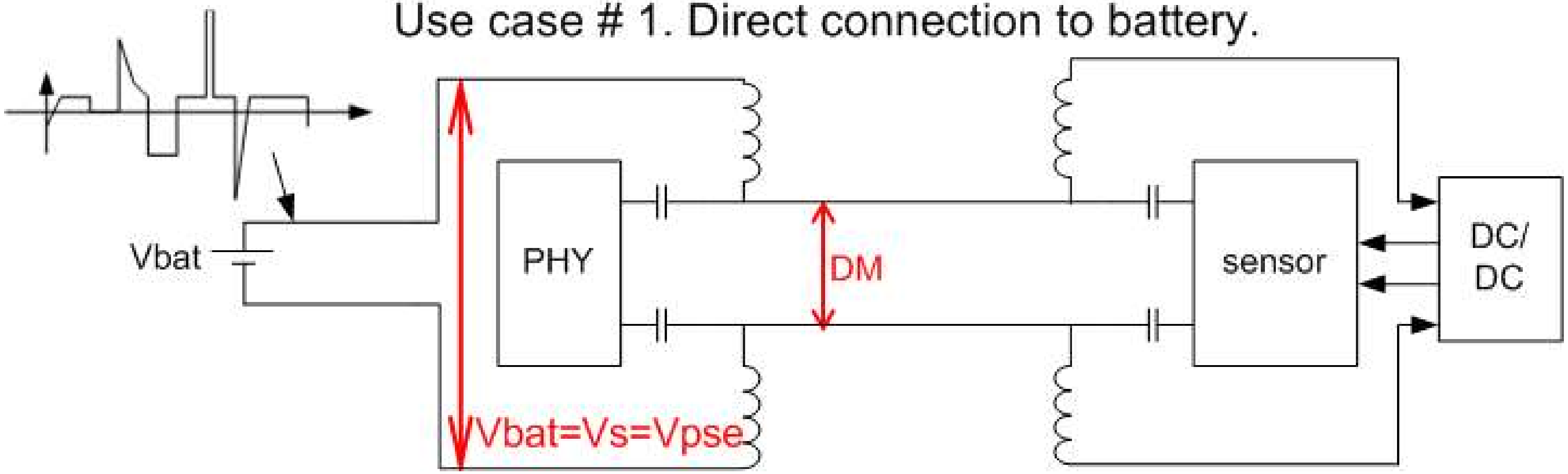
Vs_min for L=40m with 0.05, 0.089, 0.126 Ω/m wire vs. load power Ppd=PL



TA=125°C. k=0.85. Ppd=PL is measured at the device input which reflects sensor power and its DC/DC efficiency.

Basic use case concept

Use case # 1. Direct connection to battery.



Objectives

http://www.ieee802.org/3/bu/P802d3bu_Objectives.pdf

- Specify a power distribution technique for use over a single twisted pair link segment.
- Allow for operation if data is not present.
- Support voltage and current levels for the automotive, transportation, and industrial control industries.
- Do not preclude compliance with standards used in automotive, transportation, and industrial control industries when applicable.
- Support fast-startup operation using predetermined voltage/current configurations and optional operation with run-time voltage/current configuration.
- Ensure compatibility with IEEE P802.3bp (e.g., EMI, channel definition, noise requirements).