1-Wire® Bus for Ethernet PoDL

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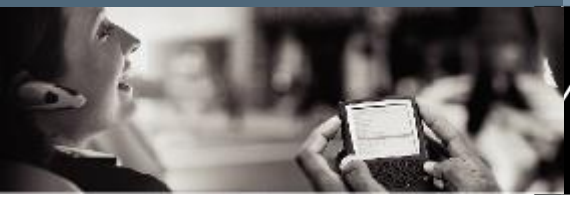

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Supporters

- Gaoling Zou – Maxim Integrated Products, Inc.
- Steve Carlson – High Speed Design
- George Zimmerman – CME Consulting, Inc.

Presentation Objectives

- Review PoDL Detection and Classification Requirements
- Propose bidirectional, PSE-PD serial-link use cases for PoDL.
- Present an overview of 1-Wire ® bus.
- Propose a 1-Wire ® bus scheme for PoDL.
- Quantify the bit rate limitations for such a scheme.

PoDL Detection and Classification

- Detection and classification is optional for PoDL, e.g. engineered systems may not require it.
- Plug-and-play PoDL applications may require detect and class.
- A low-frequency, bidirectional serial-link would allow several bytes of data to be passed back-and-forth between the PSE and PD during detect and class quickly and efficiently.
- There are many uses cases for a low-frequency, bidirectional serial link between the PSE and PD…

Low-Frequency, Bidirectional Serial Bus Use Cases for PoDL

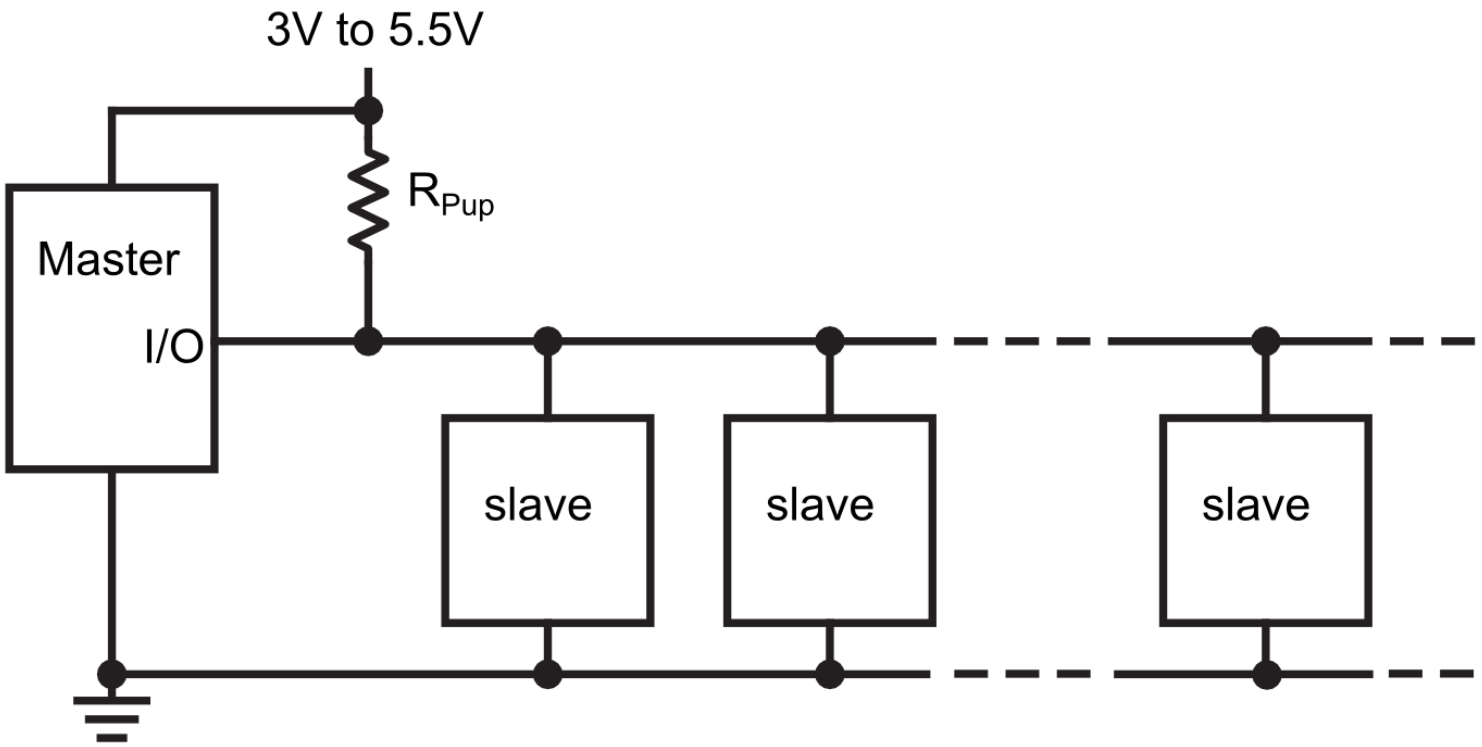
- PSE detects presence of PD, i.e. simple detection.
- PSE-PD mutual identification.
- PSE configures PD prior to powering the link, e.g. demotion.
- PSE determines Ethernet slave PHY parameters prior to powering the link and sends them to the master PHY.
- PSE interrogates PD after a power fault in order to determine PD status.
- PSE and PD communicate over unpowered link.
- PSE and PD communicate over unpowered link while Ethernet PHYs are active using auxiliary power at PD.
- A PSE may communicate with a two or more PDs (multi-drop PDs).

What is 1-Wire ® bus?

- First introduced in 1989 by Dallas Semiconductor in order to allow bidirectional, half-duplex communication between a master and one or more slaves over a single conductor pair.
- A master device can communicate with the slave devices over the single conductor pair while simultaneously powering the slaves with pull-up current, i.e. ‘parasitic’ power.
- A tutorial overview from Maxim is available at:

  http://www.maximintegrated.com/en/products/1-wire/flash/overview/

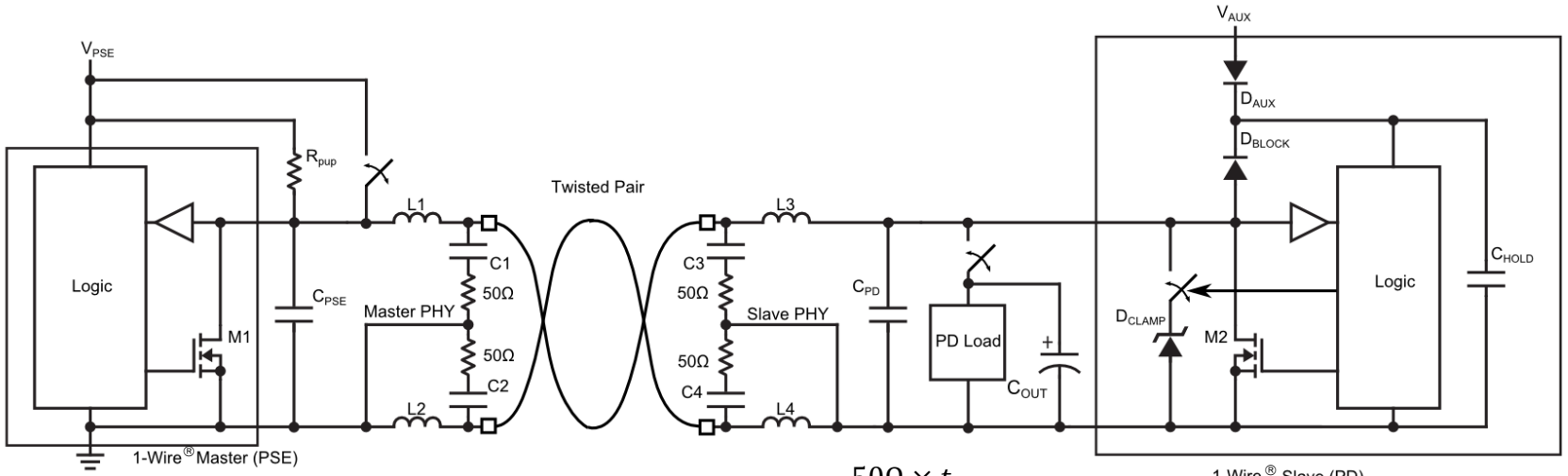
1-Wire ® Bus Block Diagram



1-Wire ® Bus Details

- The slave device must use a blocking diode and a ~1nF hold-up capacitor to derive parasitic power from the master's pull-up current.
- Data rates in excess of ~10 kbps may be achievable depending on the t_{droop} requirement (smaller t_{droop} yields faster rise time).
- The bus can't operate when the PSE is delivering voltage to the PD's load.
- If the PD has an auxiliary power source, it may be possible for the 1-Wire ® bus and the Ethernet link to operate simultaneously using the principle of frequency domain multiplexing (FDM).
- Serial communication protocols are initiated by the master and consist of bus reset, write-1, write-0, and read-bit commands (see Annex).
- Multiple slave devices may be present on the bus, and the master can detect each of them using an enumeration protocol.

PoDL 1-Wire ® Bus Block Diagram



$$L1 = L2 = L3 = L4 = L_{PoDL} > \frac{-50\Omega \times t_{droop}}{\ln(1 - 0.45)}$$

$$\Rightarrow for\ t_{droop} = 500ns, L_{PoDL} > 42\mu H$$

- PSE power and PD load switches are open when 1-Wire® bus is active.
- PD 1-Wire ® slave D_{CLAMP} switch is open when link is being powered.
- Multi-drop PD slaves are supported by 1-Wire ®.

PoDL 1-Wire® Bus Capacitance

- Assuming a damped circuit with $L_{PoDL}/50\Omega$ much smaller than the bus rise time yields:

$$C_{bus} \approx C_1 + C_3 + C_{PSE} + C_{PD}$$

- For PoDL with a damping ratio of ζ:

$$C_1 = C_3 = C_{\emptyset} > -\zeta^2 \times \frac{4 \times t_{droop}}{50\Omega \times \ln(1 - 0.45)}$$

$$\Rightarrow C_{bus} > -\zeta^2 \times \frac{8 \times t_{droop}}{50\Omega \times \ln(1 - 0.45)} + C_{PSE} + C_{PD}$$

- Example: if I_{PUP}=10mA and C_{PSE}=C_{PD}=0, a 3V rise-time is at least 160µs for t_{droop}=500ns and ζ=2.

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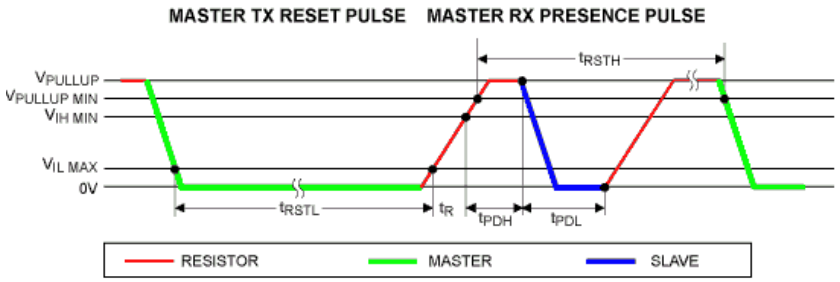
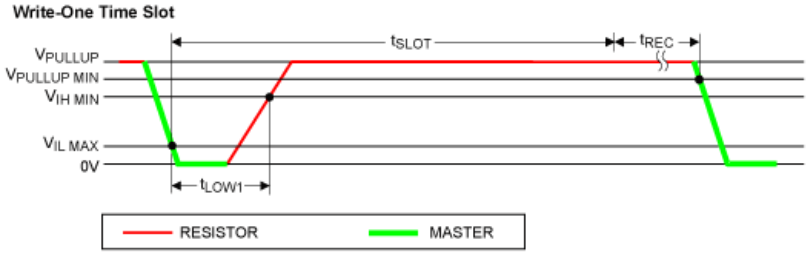
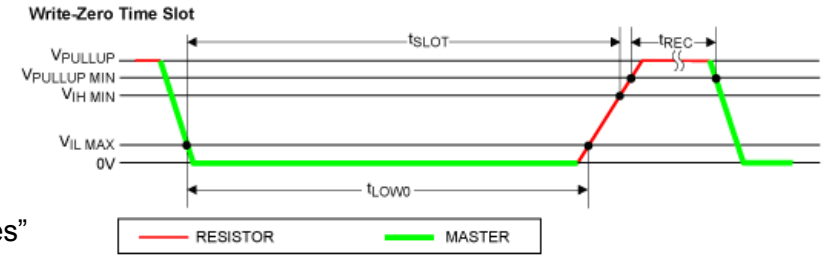
Conclusions

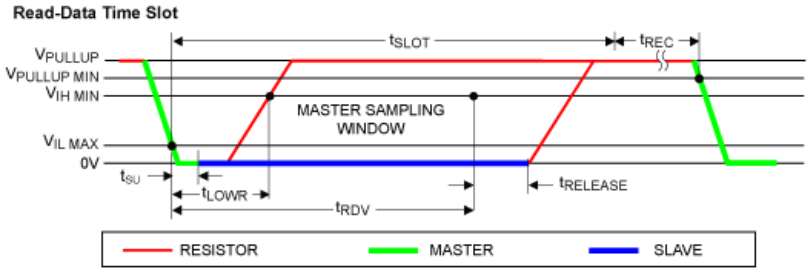
- 1-Wire ® bus is well suited to PoDL's requirements for detection and classification as well as providing a versatile, auxiliary communication channel while the link is not powered.
- In addition to PSE output and PD input capacitance, 1-Wire ® bus bandwidth is also constrained by $1/t_{droop}$.

Annex: 1-Wire ® Bus Commands









All illustrations taken from Maxim Application Note 74:
"Reading and Writing 1-Wire® Devices Through Serial Interfaces"