Momentary PoDL Connector and Cable Shorts

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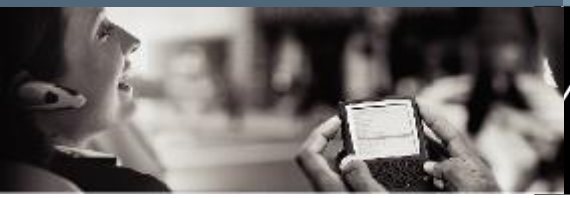
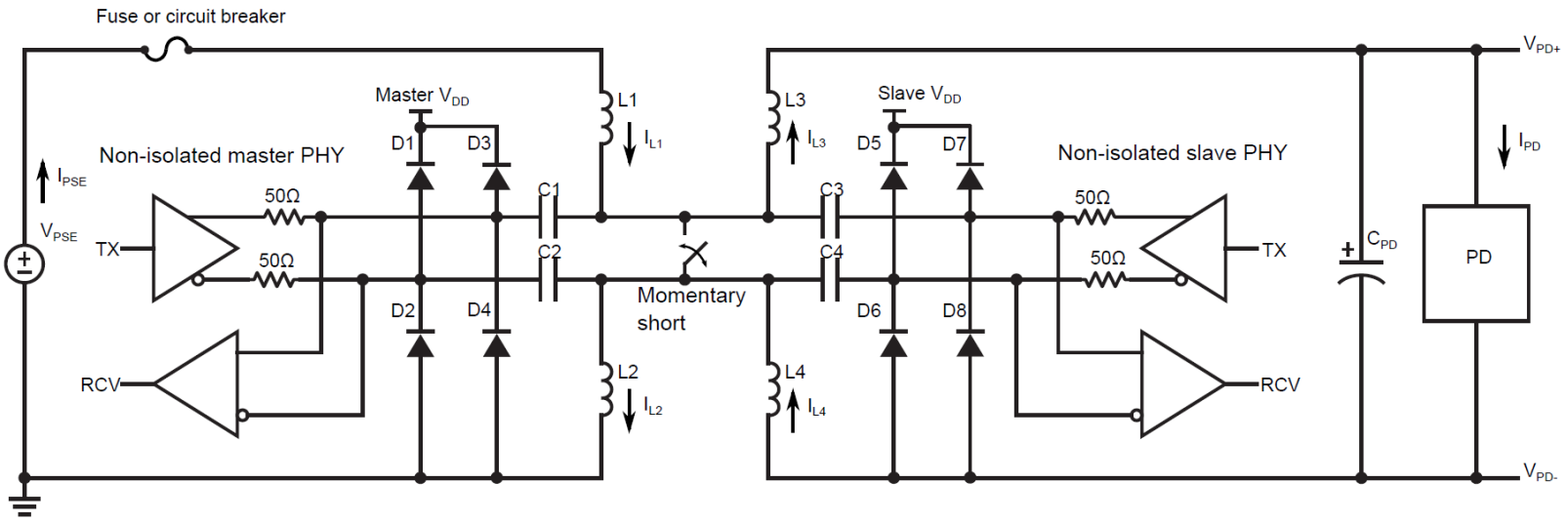


Presentation Objectives

- To put forward a momentary connector or cable short fault scenario for Ethernet PoDL.
- To quantify the requirements for surviving the energy dissipation and cable voltage transients subsequent to the momentary short.

PoDL Circuit with Momentary Short



- I_{PSE}= I_{PD}= I_{L1}= I_{L2}= I_{L3}= I_{L4} at steady-state.
- D1-D4 and D5-D8 represent the master and slave PHY body diodes, respectively.
- PoDL fuse or circuit breaker will open during a sustained over-current (OC) fault but may not open during a momentary OC fault.

PoDL Inductor Current Imbalance during a Cable or Connector Short

- During a connector or cable short, the PoDL inductor currents will become unbalanced.
- The current in inductors L_1 and L_2 will increase, while the current in inductors L_3 and L_4 will reverse.
- Maximum inductor energy is limited by the PoDL inductors' saturation current, i.e. $I_{SAT} > I_{PD(max)}$.
- Stored inductor energy resulting from the current imbalance will be dissipated by termination and parasitic resistances as well as the PHYs' body diodes.
- DC blocking capacitors C1-C4 need to be rated for peak transient voltages subsequent to the momentary short.

Max Energy Storage in PoDL Coupling Inductors during a Momentary Short

- PoDL inductors L1-L4 are constrained by t_{droop}:

$$L_{PoDL} > \frac{-50 \times t_{droop}}{\ln(1 - 0.45)}$$

$$\Rightarrow E_{L(total)} \approx 4 \times \frac{1}{2} \times L_{PoDL} \times {I_{SAT}}^2$$

- Example: if t_{droop}=500ns, L_{PoDL}=42µH which yields:

I_{SAT}	Total E_L
1A	84µJ
3A	756µJ
10A	8.4mJ

Peak Transient Voltage after a Short

- The maximum voltage across the PHY DC blocking capacitors C1-C4 following a momentary short assuming damping ratio ζ is:

$$V_{max} \approx I_{sat} \times \sqrt{\frac{L_{PoDL}}{C_{\varphi block}}} = I_{sat} \times \frac{50\Omega}{2 \times \zeta}$$

$$\text{where } C_{\varphi block} \geq -\zeta^2 \times \frac{4 \times t_{droop}}{50\Omega \times \ln(1 - 0.45)}$$

- The maximum voltage differential between the conductors in the twisted pair is then:

$$V_{max(diff)} = 2 \times V_{max} \approx I_{SAT} \times 50\Omega/\zeta$$

- Example: A critically damped PoDL network (ζ=1) with inductor I_{SAT} = 1A yields $V_{max(diff)} \approx$ 50V while an inductor I_{SAT} = 10A will yield $V_{max(diff)} \approx$ 500V.

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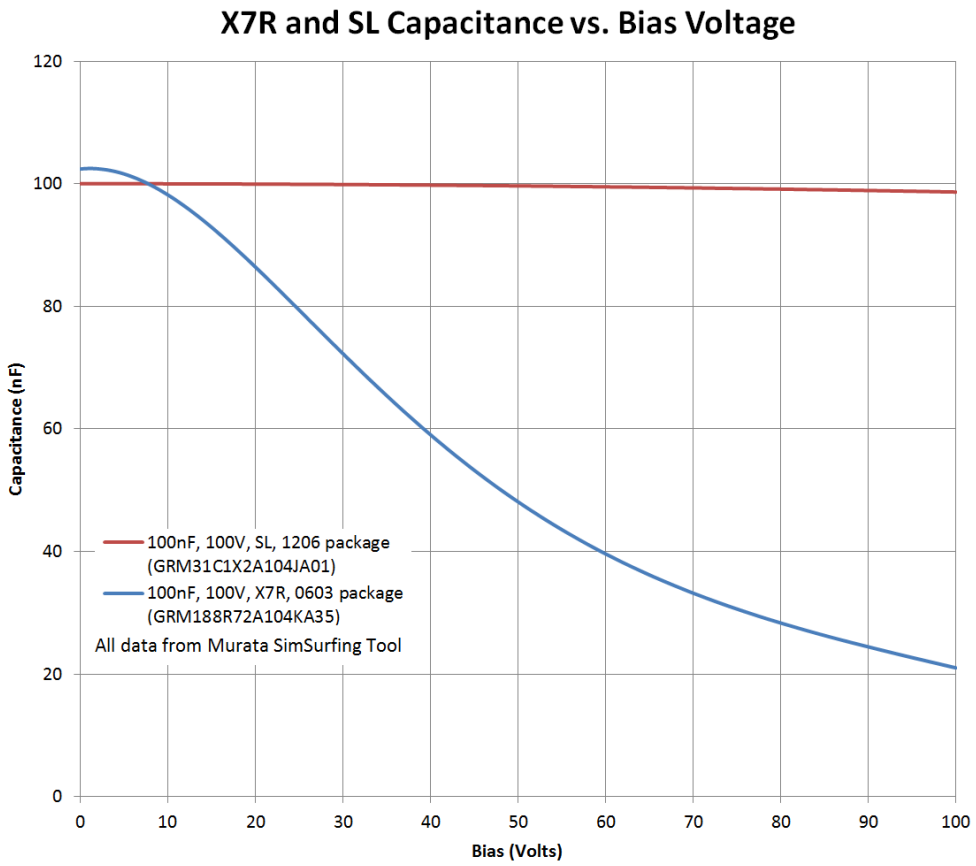
Ceramic Capacitor Voltage Coefficients

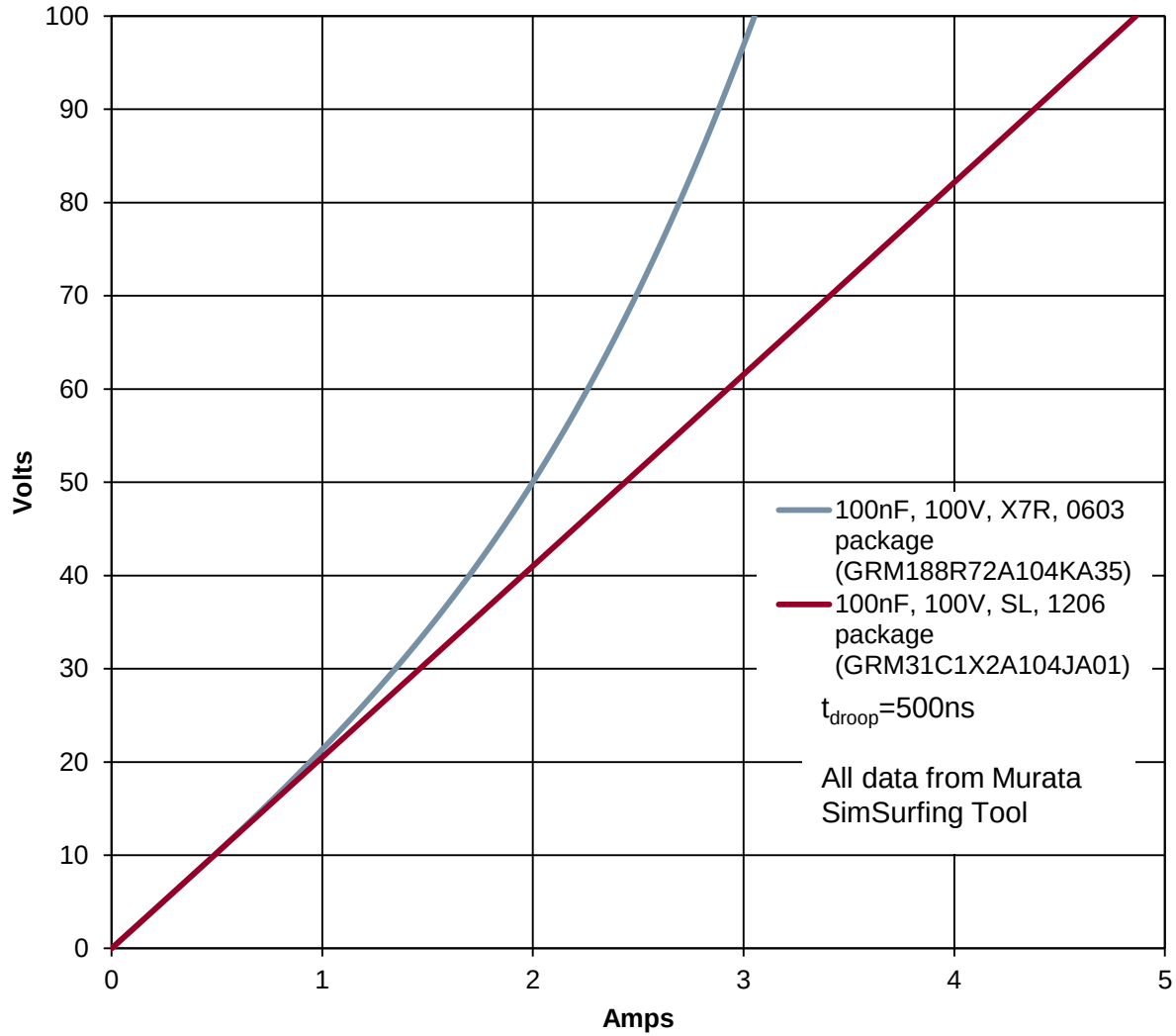
- Ceramic capacitors may exhibit a large negative voltage coefficient (see Annex for more info).
- Example: PoDL inductor I_{SAT}=3A may result in ~61V of stress across a 100nF 100V rated SL capacitor after a short, but a 100nF 100V rated X7R capacitor would be stressed to ~100V.



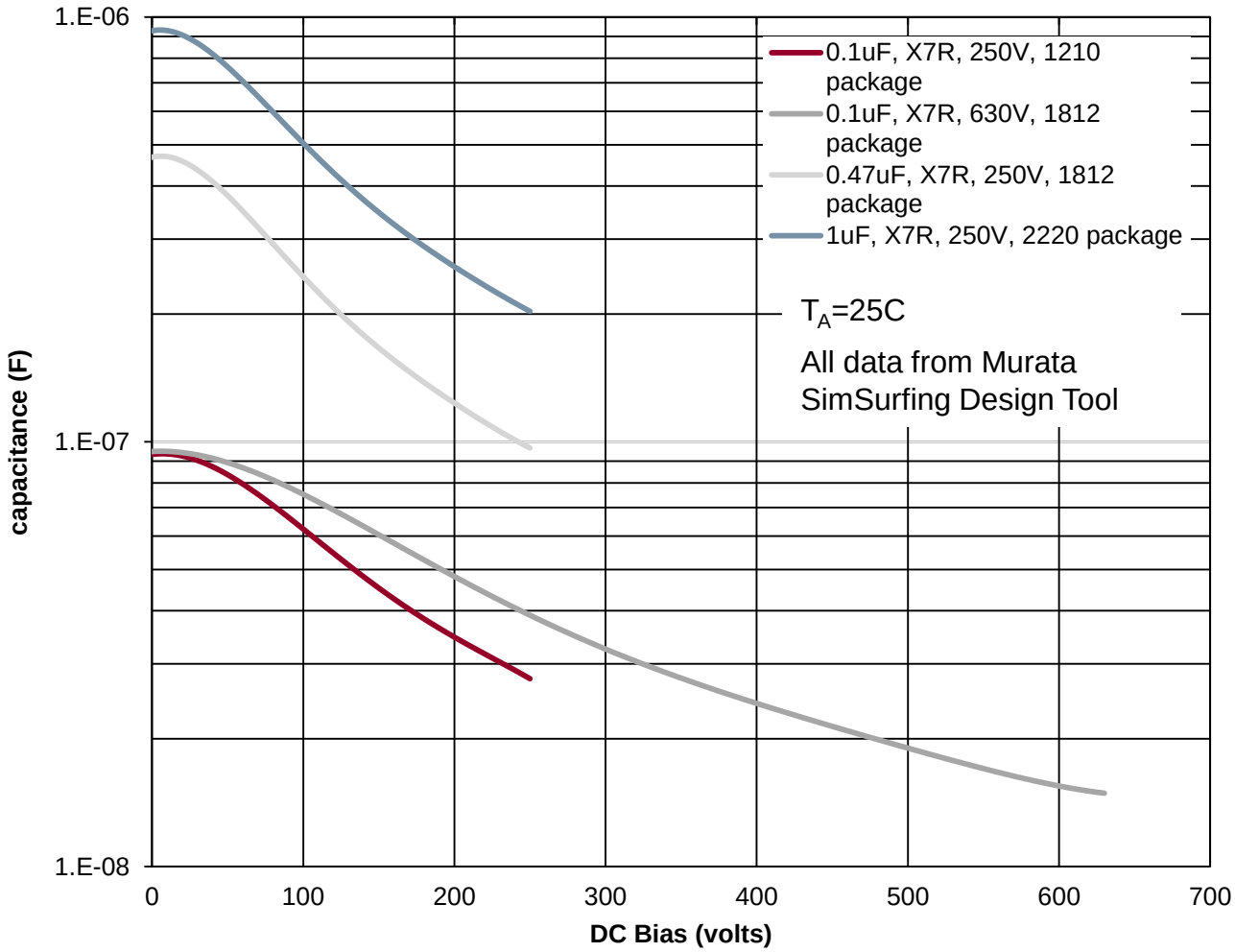
Conclusions

- Energy discharge into the PHYs greater than 1 mJ after a momentary connector or cable short may occur in PoDL with inductor saturation currents greater than 3A for t_{droop}=500ns.
- The energy discharge is proportional to t_{droop} and the square of PoDL inductor saturation current.
- PHY DC blocking capacitor voltage rating should account for peak voltage transients subsequent to the short.
- Ceramic capacitors may exhibit a large negative voltage coefficient that can significantly increase the magnitude of the voltage transients.
- Boosting PSE voltage and/or minimizing t_{droop} may be necessary for high power PoDL applications.
- Additional analysis of this problem may be warranted.

Annex - Post Short Circuit PHY DC Block Capacitor Stress Voltage vs. Inductor I_{SAT}



Annex Cont'd – High Voltage Ceramic Capacitance vs. Bias Voltage



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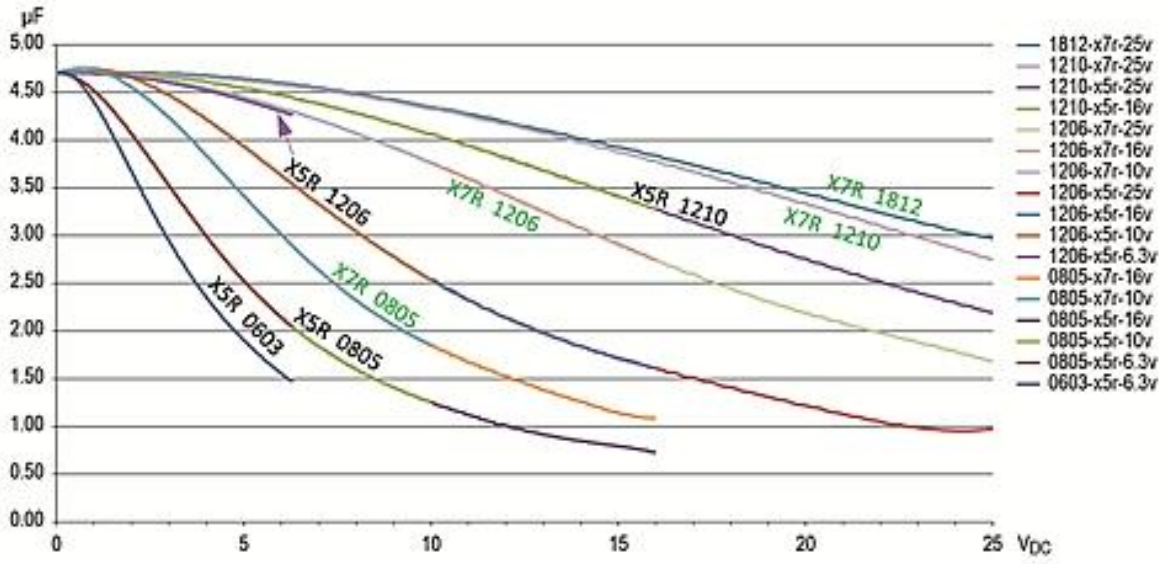
Annex Cont'd – Low Voltage 4.7μF Ceramic Capacitance vs. DC Bias*



Data excerpted from EDN article "Temp and voltage variation of ceramic caps, or why your 4.7μF part becomes 0.33 μF" by Mark Fortunato, November 26, 2012

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