Analysis and Proposal for PoDL Noise Limits

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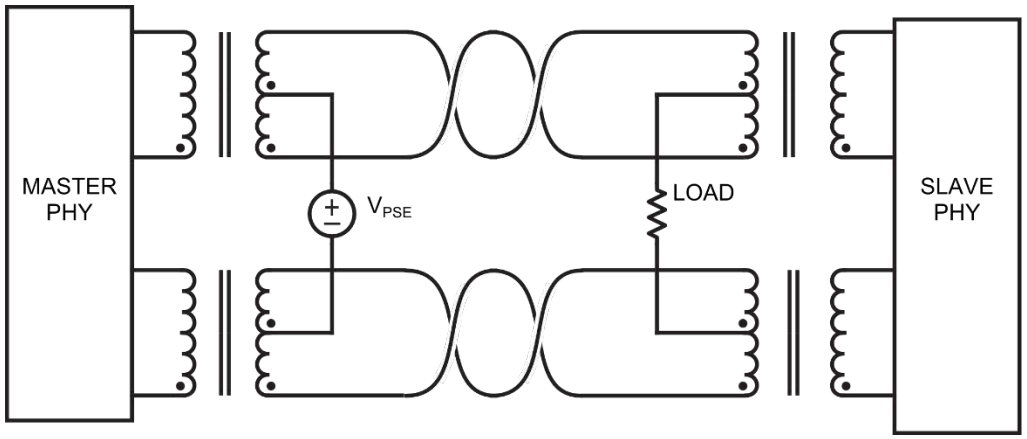
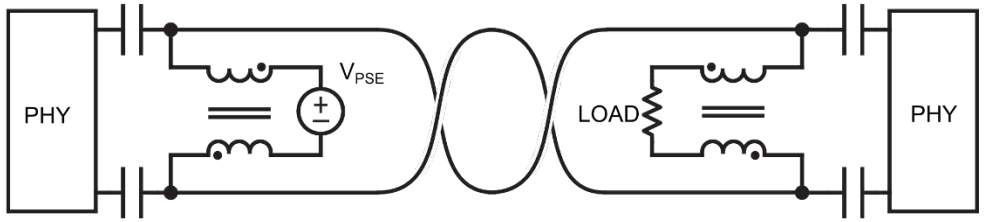
Presentation Objectives

- Overview
- Present analysis of PSE and PD induced ripple and transient noise and propose limits
- Conclusion

Differences between PoE and PoDL



2-Pair PoE Circuit Architecture

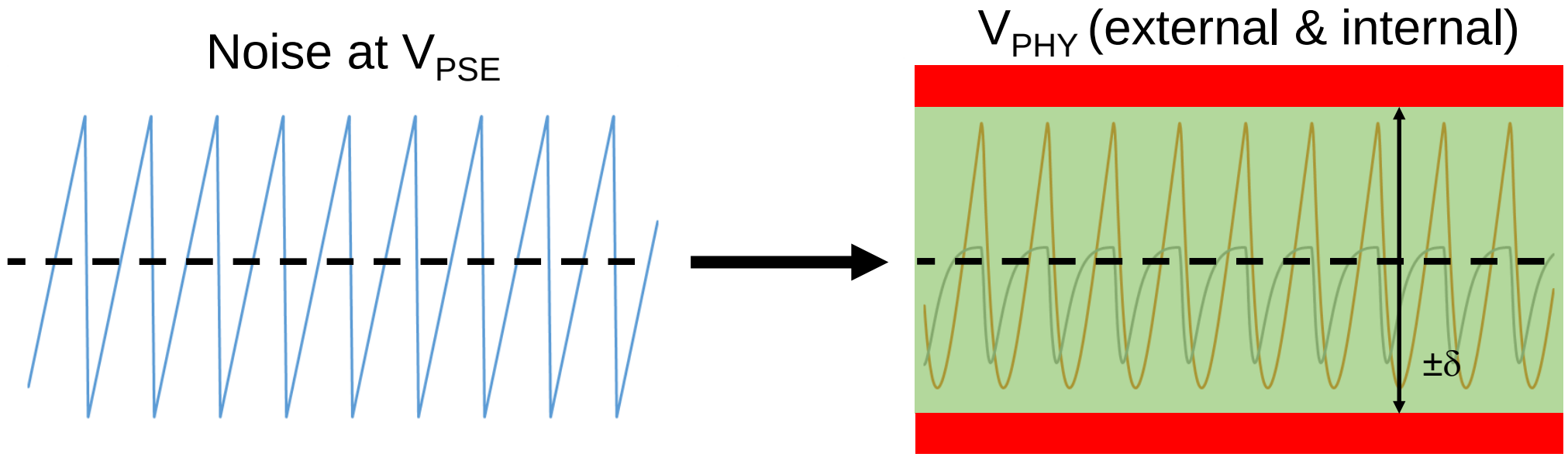


PoDL Circuit Architecture

- For PoE, noise introduced by a PSE or PD into the MDI/PI is inherently common mode to the data.
- For PoDL, noise introduced by a PSE or PD into the MDI/PI shares the same differential path as the PHYs.
  - The coupling networks act as band-pass filters for PSE V_n and PD I_n, but of itself this attenuation may be insufficient to ensure data integrity of the PHYs.

PSE and PD Noise Limit Criteria

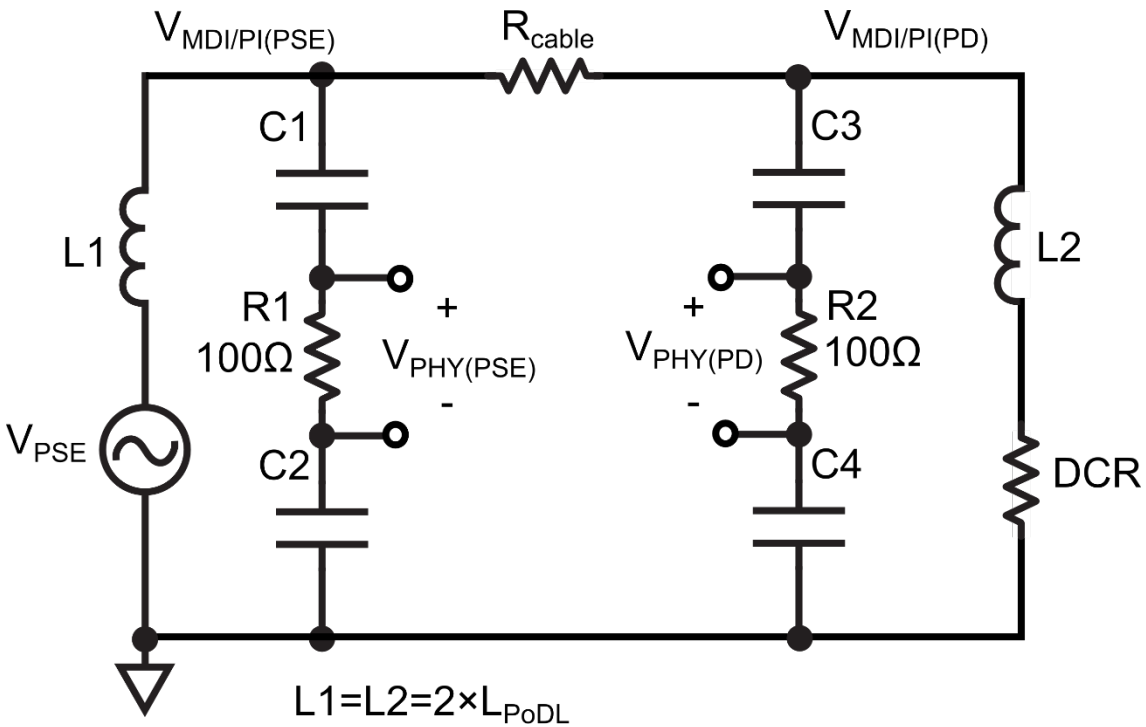
- Basically any noise introduced by the PSE or PD into the MDI/PI should not exceed a predefined envelope of $\pm\delta$ Volts referenced to the input of either PHY.
- The PHY has a high-pass filtered internal input, and the noise referenced to this port must also be considered.
- All PSE and PD noise limits shall be specified and measured at there respective MDI/PIs.



Simplified Circuit Model for Analyzing V_{PSE} Induced Noise

- The simplified circuit model shown here was used to perform the PSE noise analysis.
- Total PD DCR was assumed to be 4Ω, and R_{Cable} was assumed to be 6.5Ω.
  - These parameters have no impact on a PSE noise specification at the MDI/PI, but they do impact the requirements on the PSE power supply.
- The following parameters were assumed for the PHYs and are consistent with their MDI RL requirements:

	100BASE-T1	1000BASE-T1
L_{PoDL}	20µH	3µH
C_{PHY}	100nF	10nF
f_{HPF}	1MHz	10MHz

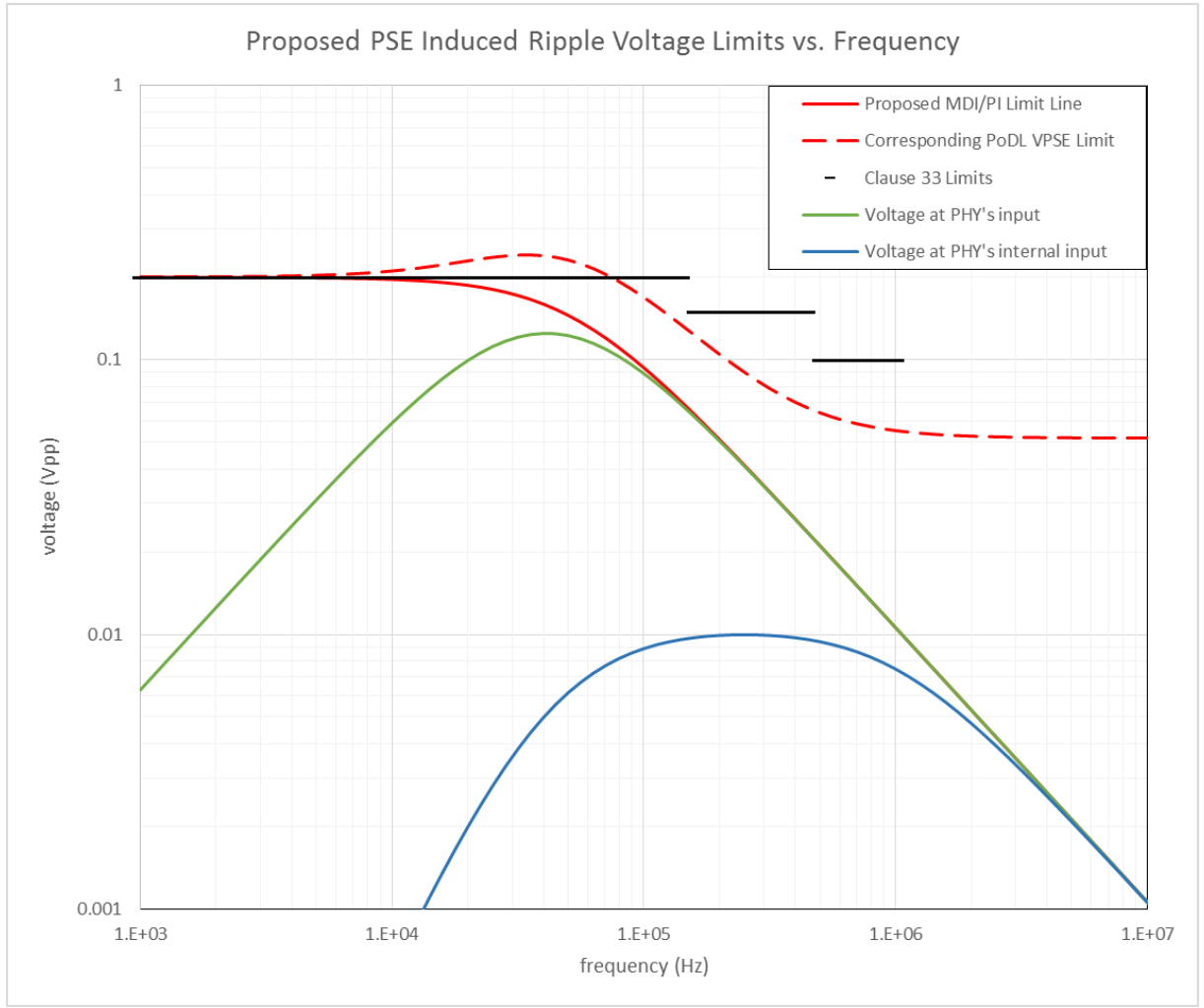


V_{PHY}/V_{PSE} Simplified Circuit Model

100BASE-T1 PoDL PSE Ripple Noise Analysis Results

- A MDI/RL limit line was determined such that the maximum ripple voltage at the PHY's internal input was less than 10mVpp.
  - This yielded ~125mVpp at the PHY's physical input.
- The corresponding requirements for a PoDL PSE voltage source are significantly more stringent than Clause 33.
- Propose the following PSE ripple voltage limit line referred to MDI/PI for f>1kHz and f<10MHz:

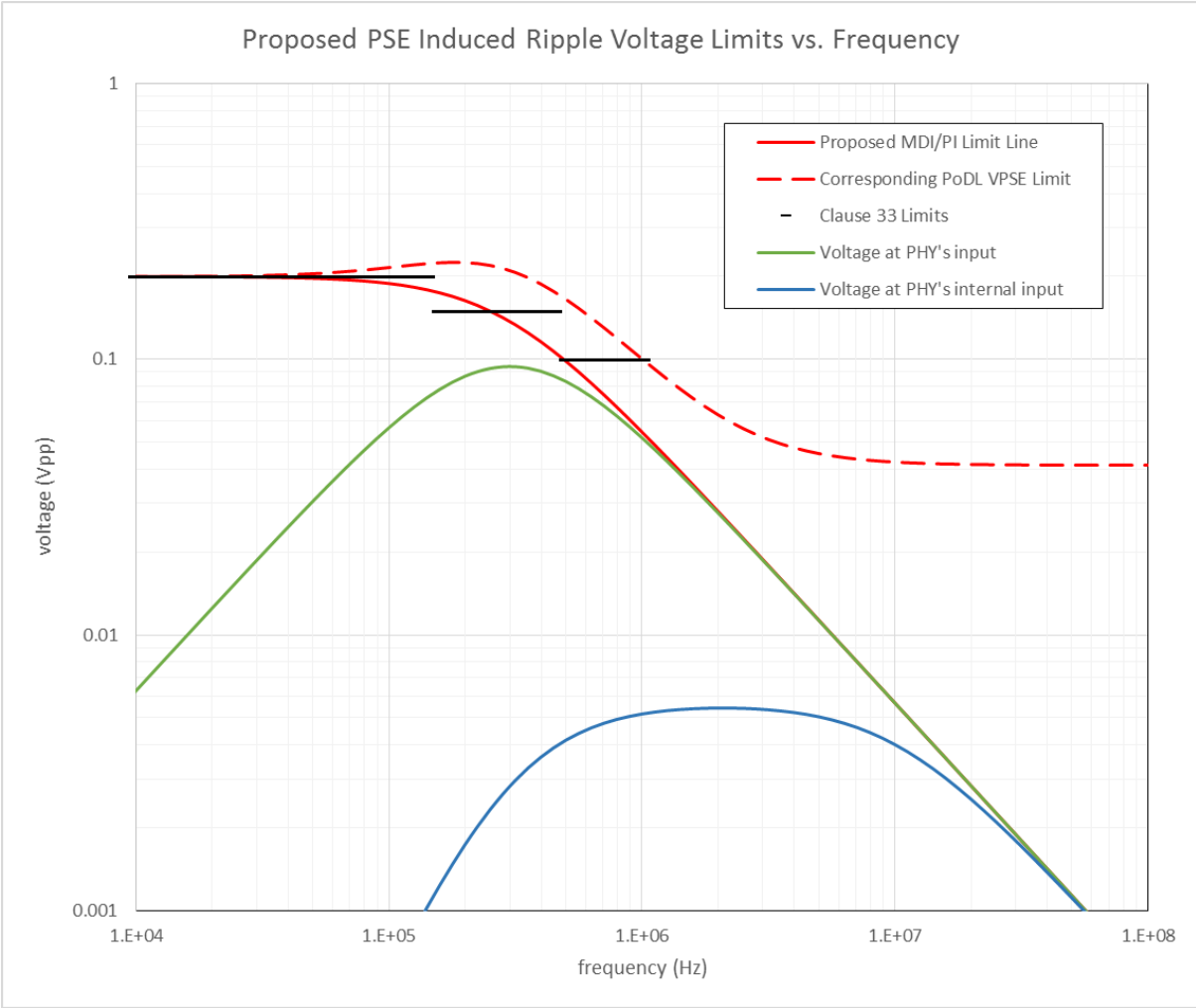
$$V_{MDI(PSE)} \leq \frac{0.2Vpp}{\sqrt{1+(f/50kHz)^2}}$$



1000BASE-T1 PoDL PSE Ripple Noise Analysis Results

- A MDI/RL limit line was determined in order to be consistent with the requirements of a Clause 33 PSE power supply.
  - This yielded 94mVpp and 5.4mVpp of ripple at the PHY's external and internal inputs, respectively.
- Propose the following PSE ripple voltage limit line referred to the MDI/PI for f>1kHz and f<10MHz:

$$V_{MDI(PSE)} \leq \frac{0.2Vpp}{\sqrt{1+(f/280kHz)^2}}$$



PSE Induced Transient Noise

- Define a maximum dV/dt at the PSE MDI/PI that will result in an δ Volts impulse referenced to the external input of the PHY.
- For a given MDI/PI slew rate of *A* V/s, the impulse voltage δ at steady-state referenced to the external input of the PHY is:

$$\delta = 50\Omega \times C_{PHY} \times A\ (Volts)$$

$$\rightarrow A = \frac{\delta}{50\Omega \times C_{PHY}}\ (Volts/s)$$

- The resulting peak impulse voltage at the internal input of the PHY is*:

$$V_{PHY,internal(max)} = \frac{\delta \times a}{(b-a)} \times \left\{ exp\left[\frac{a \times ln\left(\frac{a}{b}\right)}{b-a}\right] - exp\left[\frac{b \times ln\left(\frac{a}{b}\right)}{b-a}\right] \right\}\ (Volts)$$

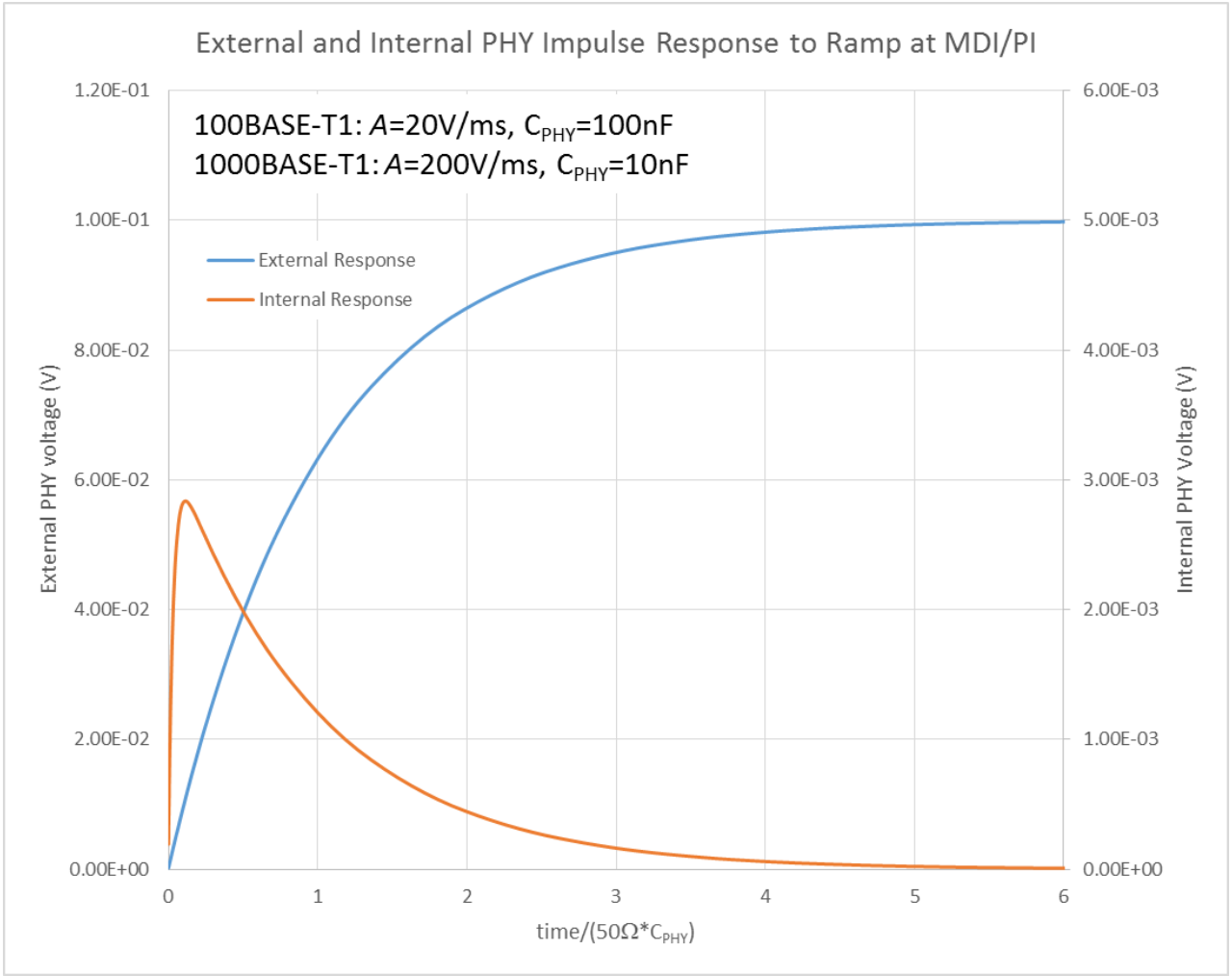
$$\text{where } a = \frac{1}{50\Omega \times C_{PHY}}\ and\ b = 2 \times \pi \times f_{HPF}$$

- Example: for the 100BASE-T1 parameters from slide 5, δ=100mV yields *A*=20V/ms and a peak impulse of 2.84mV at the PHY's internal input.

*See Annex A for derivation.

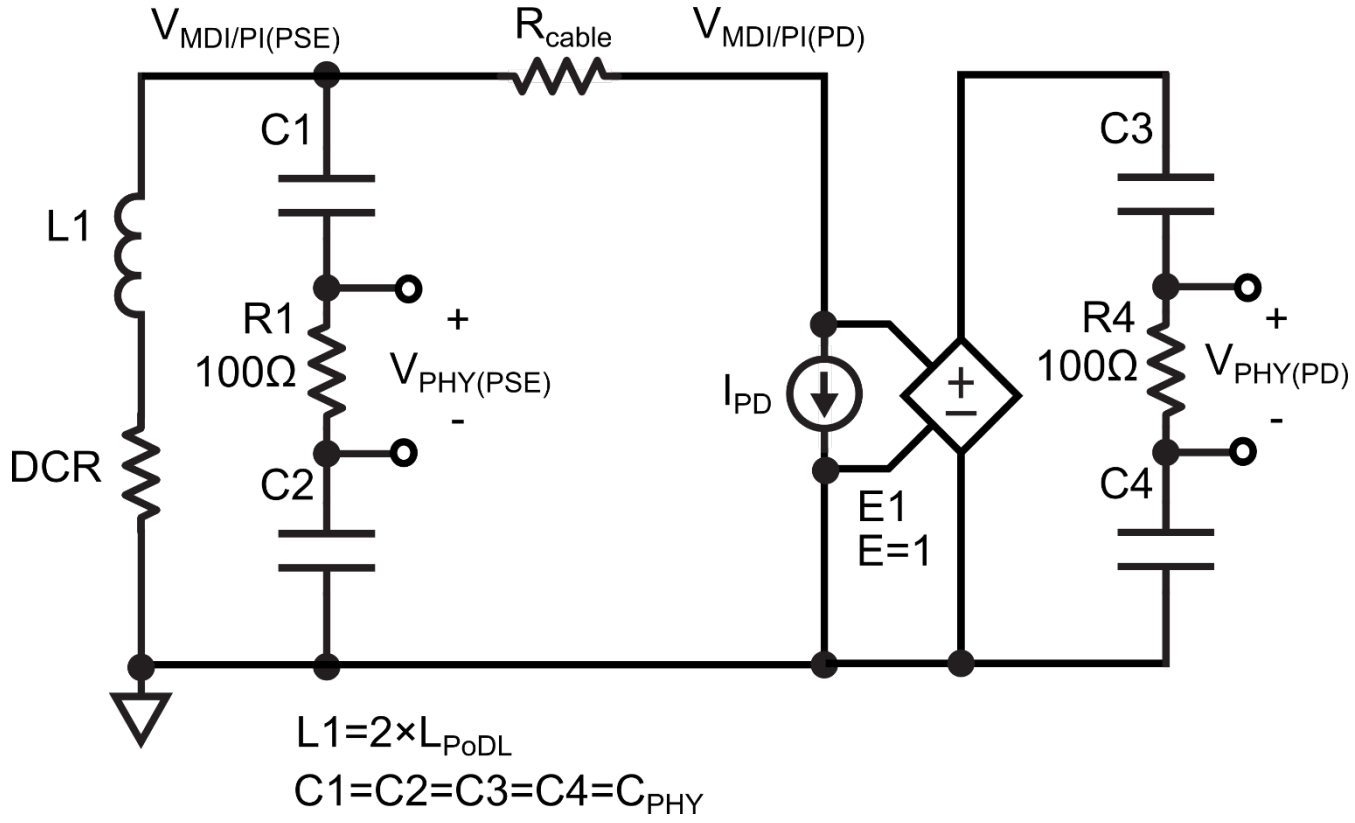
Proposal for PSE Slew Rate Limits

- For 100BASE-T1, the PSE induced voltage slew-rate at the MDI/PI shall not exceed 20V/ms.
- For 1000BASE-T1, the PSE induced voltage slew-rate at the MDI/PI shall not exceed 200V/ms.
- These limits yields a maximum impulse of 100mV and 2.84mV at the PHY's external and internal inputs, respectively.



Simplified Circuit Model for Analyzing I_{PD} Induced Noise

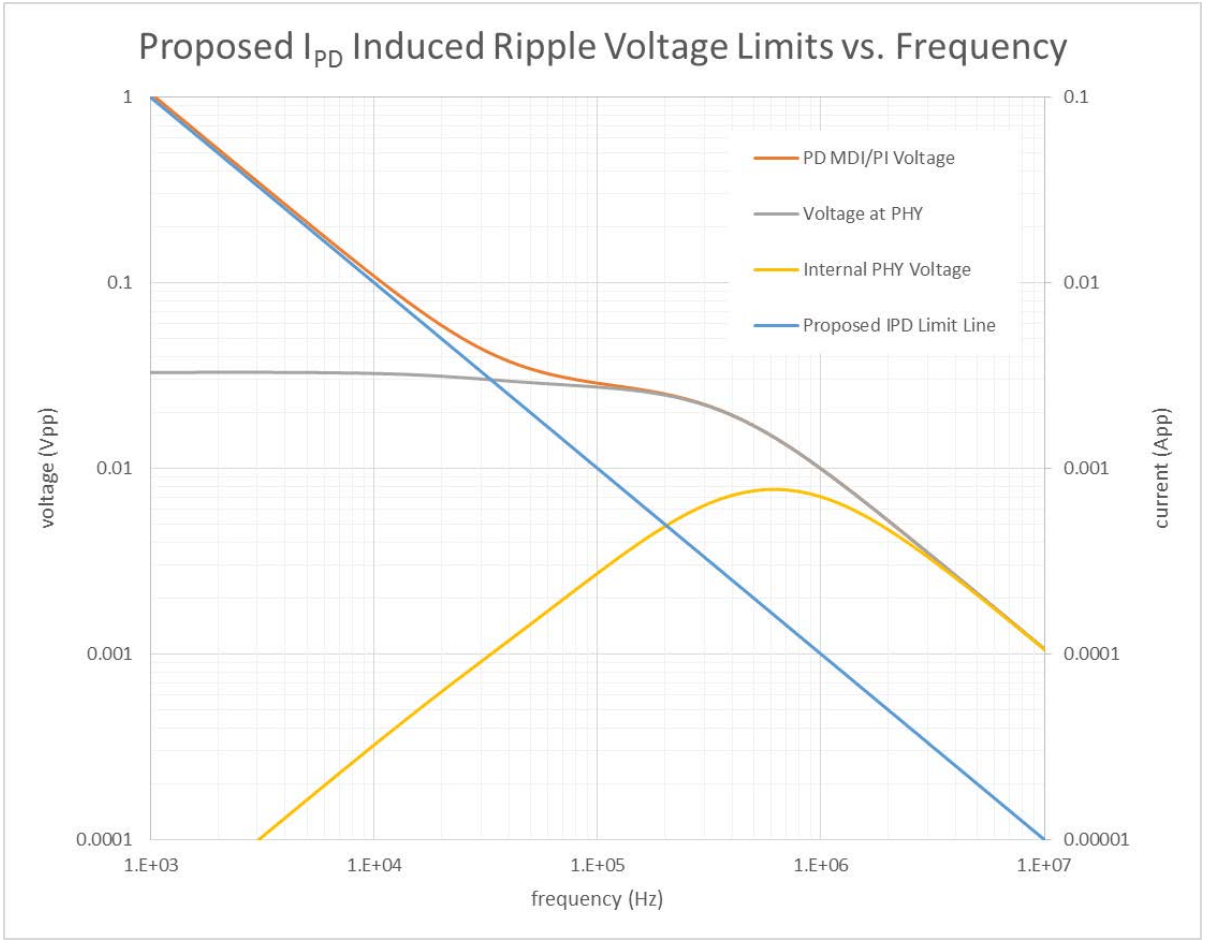
- The simplified circuit model shown here was used to analyze PD induced current noise.
- PD current noise is specified as MDI/PI port current.
- R_{cable} and PSE DCR were assumed to be 6.5Ω and 4Ω, respectively.
  - Maximizing impedance in shunt with the PD MDI/PI is the worst case scenario for current noise.



100BASE-T1 PoDL PD Ripple Noise Analysis Results

- A MDI/PI port current limit line was determined that limited the voltage at the internal input of the PHY to less than $10mV_{pp}$.
  - The subsequent voltage at the external input of the PHY was less than $35mV_{pp}$.
- Propose the following limit line for frequencies between 1kHz and 10MHz:

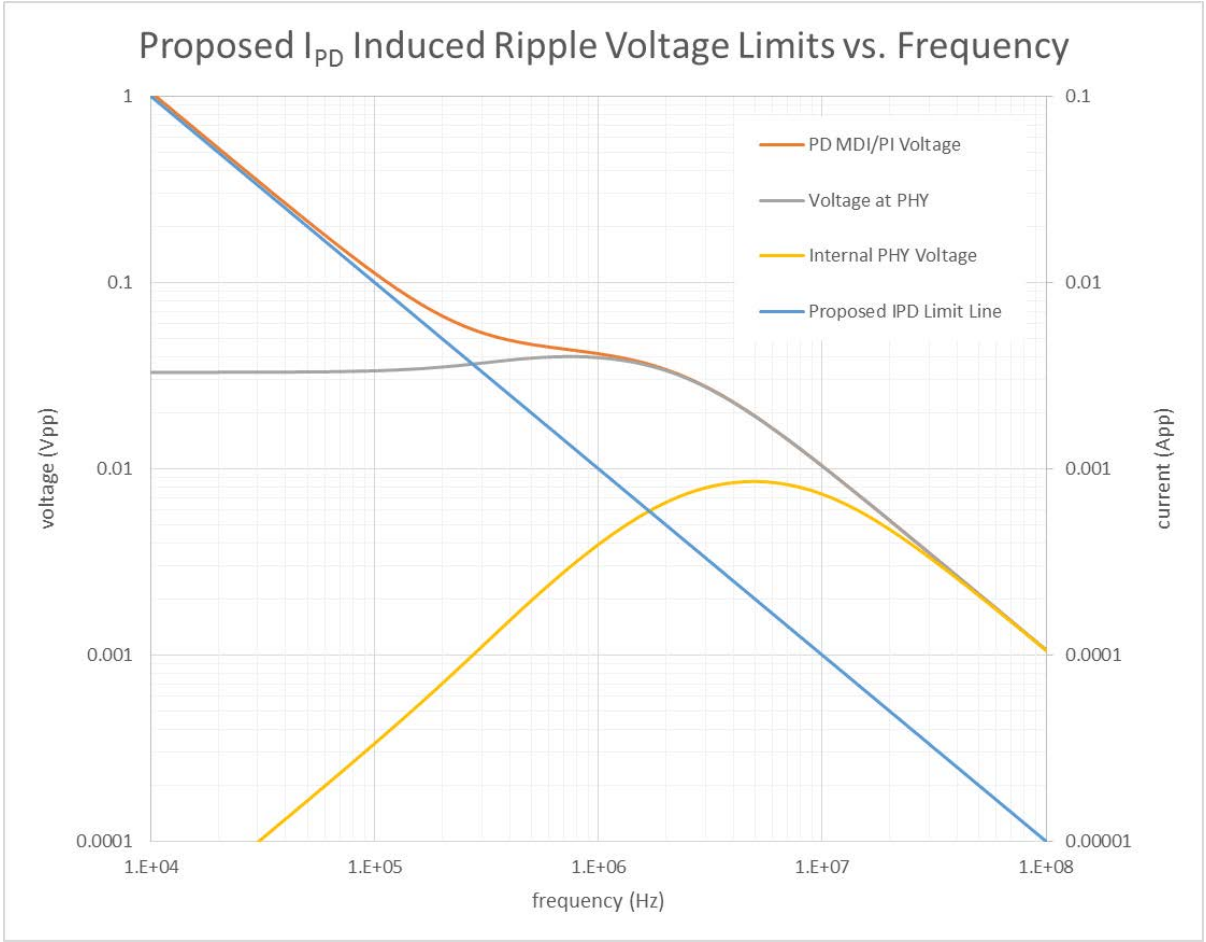
$$I_{PD,ripple} \leq \frac{100mA_{pp}}{(f/1kHz)}$$



1000BASE-T1 PoDL PD Ripple Noise Analysis Results

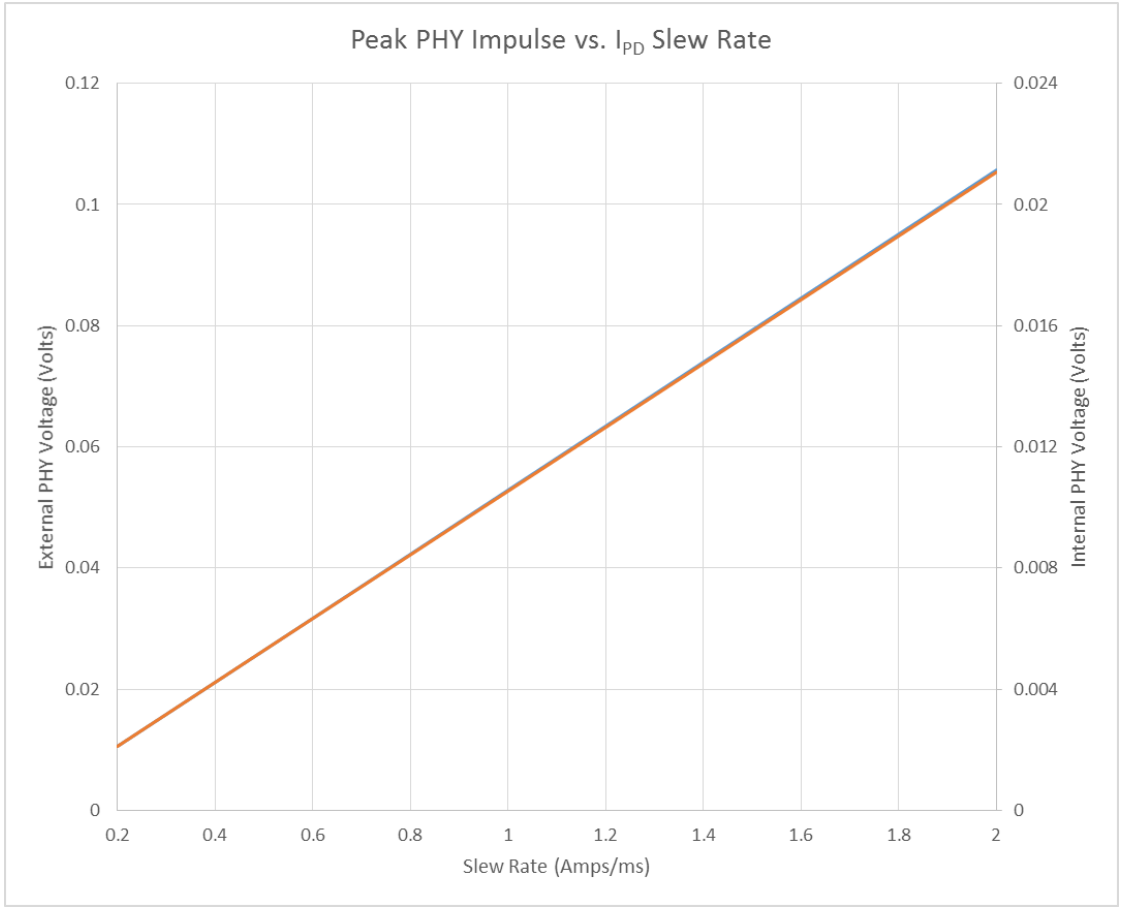
- A MDI/PI port current limit line was determined that limited the voltage at the internal input of the PHY to less than $10mV_{pp}$.
  - The subsequent voltage at the external input of the PHY was less than $40mV_{pp}$.
- Propose the following limit line for frequencies between 10kHz and 100MHz:

$$I_{PD,ripple} \leq \frac{100mA_{pp}}{(f/10kHz)}$$



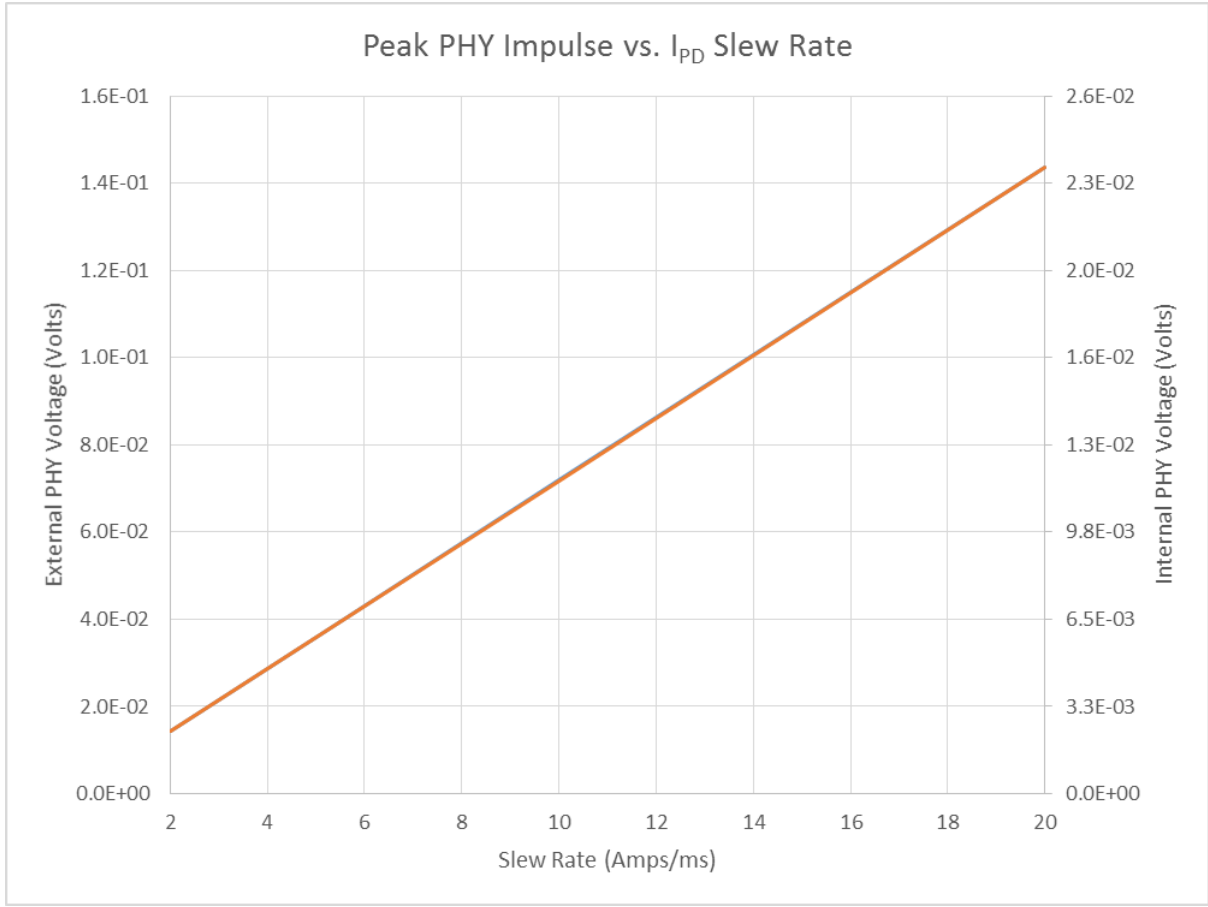
100BASE-T1 I_{PD} Impulse Noise Analysis

- The following worst case parameters were assumed:
  - L_{PoDL}=30uH
  - R_{PSE}=4Ω
  - R_{cable}=6.5Ω
  - PHY f_{HPF}=1MHz
- Analysis indicates that PD current slew rate should be limited to less than **1A/ms** in order to limit external and internal impulses to less than 53mV and 11mV, respectively.



1000BASE-T1 I_{PD} Impulse Noise Analysis

- PD current was ramped from zero initial conditions at a constant slew rate.
- The following worst case parameters were assumed:
  - L_{PoDL}=4.5uH
  - R_{PSE}=4Ω
  - R_{cable}=6.5Ω
  - PHY f_{HPF}=10MHz
- Analysis indicates that I_{PD} slew rate should be limited to less than **10A/ms** in order to limit external and internal impulses to less than 72mV and 12mV, respectively.



Summary

- Propose PSE and PD Noise Limits as follows:

	100BASE-T1	*1000BASE-T1*
PSE power feeding and ripple noise for frequencies from 1kHz to 10MHz	$V_{MDI(PSE)} \leq \frac{0.2Vpp}{\sqrt{1+(f/50kHz)^2}}$	$V_{MDI(PSE)} \leq \frac{0.2Vpp}{\sqrt{1+(f/280kHz)^2}}$
PSE slew rate	*<20V/ms*	*<200V/ms*
PD current ripple noise for frequencies from 1kHz to 10MHz	$I_{PD,ripple} \leq \frac{100mA_{pp}}{(f/1kHz)}$	$I_{PD,ripple} \leq \frac{100mA_{pp}}{(f/10kHz)}$
PD slew rate	*<1A/ms*	*<10A/ms*

- In general, each limit attempted to keep ripple and impulse noise at the PHY's external and internal inputs to less than 100mV peak and 10mV peak, respectively.

Conclusion

- The effects of PSE and PD induced ripple and transient noise on 100BASE-T1 and 1000BASE-T1 PHYs was presented.
- Coupled noise is highly dependent on the PHY DC blocking capacitance and HPF pole frequency.
  - There are currently no 802.3bw or bp limits on $C_{PHY,max}$!
- Different limits were proposed for 100BASE-T1 and 1000BASE-T1.
  - Power delivery for 100BASE-T1 is more challenging because the bandpass and high-pass frequency responses of the coupling networks and internal PHY filter, respectively, are much lower.

Questions?

Annex A – Derivation of PSE Induced Maximum Impulse Noise Referred to the PHYs' Intrinsic Inputs

The Laplace transform for a second order high-pass response with poles at *a* and *b* radians/second is:

$$\frac{1}{(b-a)} \times \left(a^2 \times e^{-at} - b^2 \times e^{-bt}\right) \leftrightarrow \frac{s^2}{(s+a) \times (s+b)}$$

Integrating the impulse response twice yields the following for the PHYs' unit ramp response:

$$V_{PHY,intrinsic}(t) = \frac{1}{(b-a)} \times \left(e^{-at} - e^{-bt}\right)$$

Setting $dV_{PHY,extrinsic}(t)/dt=0$ yields:

$$\frac{dV_{PHY,intrinsic}(t)}{dt} = 0$$

$$\rightarrow a \times e^{-at} = be^{-bt}$$

$$\rightarrow t = \frac{\ln(a/b)}{a-b}$$

$$\rightarrow V_{PHY,intrinsic(max)} = \frac{1}{(b-a)} \times \left\{exp\left[\frac{-a \times ln(a/b)}{(b-a)}\right] - exp\left[\frac{-b \times ln(a/b)}{(b-a)}\right]\right\}$$