

# AM0 SELECTION in 802.3by

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## BACKGROUND

- January 2015 (baden\_3by\_01b\_0115.pdf):
- **PCS and FEC Baseline Approved** (Y: 62 , N: 3 , A: 16)
  - CWMs are used for RS FEC locking
  - Constructed from concatenation of CL82 **40G** AM0, AM1, AM2, AM3
- March Plenary 2015 (slavick\_3by\_01a\_0315.pdf):
- **Amendment proposed and accepted** (Y: 25 , N: 8 , A: 44 ):
  - Change AM0 to 100G AM0 from 40G AM0
  - CWMs are used for RS FEC locking
  - Constructed from concatenation of CL82 **100G** AM0, and CL82 40G, AM1, AM2, AM3
- 1. Estimated savings of 10K gates **per PHY**.
  - “Implementations doing 400GE, 100GE and 4x25GE use the same logic to align to the codeword, saving ~10k gates”
  - “For EEE use same AM0 RAMs as 100GE with a codeword spacing of 1 instead of 2 to provide the highest frequency of markers as possible. 100G provides markers every 100ns while 25G would be 200ns.”

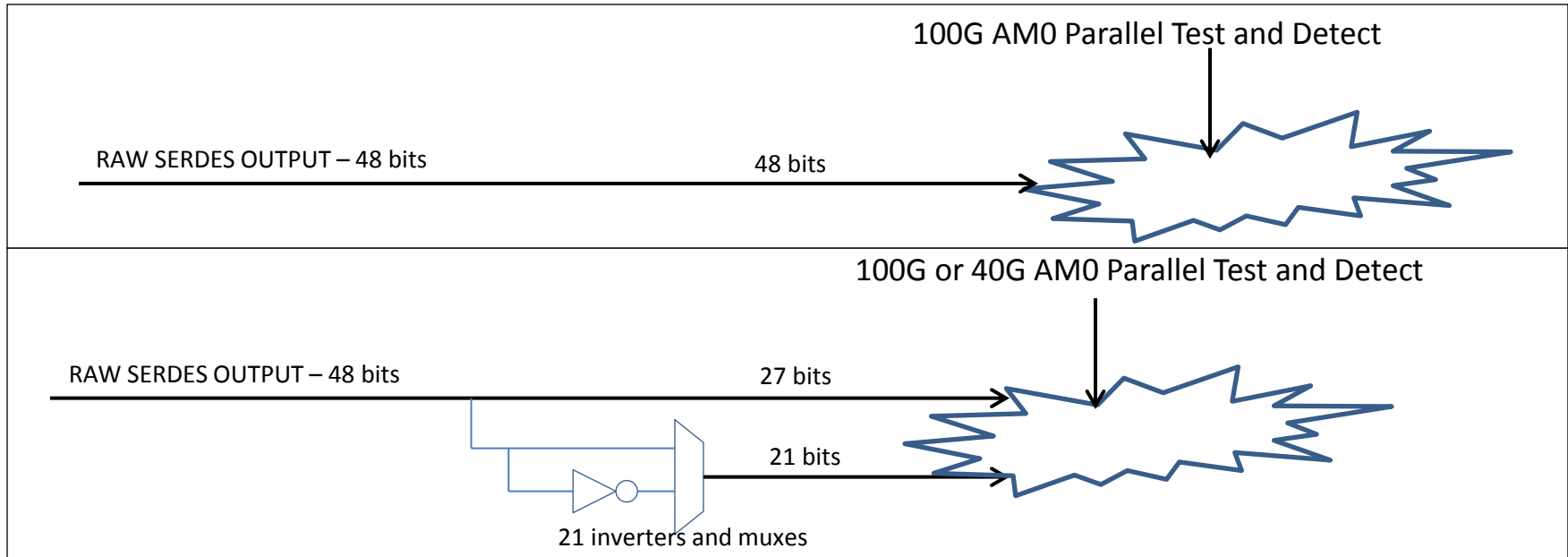
## TALKING POINTS

- The predicted area savings can be improved.
  - This presentation will demonstrate that the cost per 25G PHY is on the order of 1K gates in total.
- Both 1K and 10K gates are insignificant for a 35M gates NIC or a 1B gate Switch.
- IEEE Task Forces does not have time to consider miniscule savings of even 10K gates on such devices.
- The following addresses each of the items listed as justifications for this change:
  1. *Estimated savings of 10K gates per PHY.*
    - *“Implementations doing 400GE, 100GE and 4x25GE use the same logic to align to the code-word, saving ~10k gates”*
      - The logic which implements the “parallel test and detect” mechanism is required on each lane of a 100G port.
      - That logic may be optimized for the specific pattern (“comparing to a constant is cheaper than to a programmable value”).
      - Out of the 12 nibbles, or 48 bits, that are validated when testing for an AM0 match, only 21 bits differ between the 100G AM0 and the 40G AM0.
      - Therefore, only 21 – 2 to 1 muxes (3 gates each) are needed to select between a 40G and a 100G AM0 compare.
      - For 48 “parallel and test” mechanisms, the total difference is less than 1K gates (984)
        - See following page for details and summary.
  2. *“For EEE use same AM0 RAMs as 100GE with a code-word spacing of 1 instead of 2 to provide the highest frequency of markers as possible. 100G provides markers every 100ns while 25G would be 200ns.”*
    - It can be shown that the same AM0 format can be used for ‘normal’ vs. ‘rapid’ CWMs
      1. [http://www.ieee802.org/3/by/public/adhoc/architecture/cober\\_050615\\_25GE\\_adhoc.pdf](http://www.ieee802.org/3/by/public/adhoc/architecture/cober_050615_25GE_adhoc.pdf)
      2. [http://www.ieee802.org/3/by/public/adhoc/architecture/wertheim\\_050615\\_25GE\\_adhoc.pdf](http://www.ieee802.org/3/by/public/adhoc/architecture/wertheim_050615_25GE_adhoc.pdf)

# AM0 SELECTION in 802.3by

40G AM0	0x90, 0x76, 0x47, BIP3, 0x6F, 0x89, 0xB8, BIP7
100G AM0	0xC1, 0x68, 0x21, BIP3, 0x3E, 0x97, 0xDE, BIP7

1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	0	0	1	1	1	0	1	1	0	1	1	1	1	0	0	0	1	0	0	1	1	0	1	1	1	0	0	0
1	1	0	1	0	0	0	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	1	1	0	1	0	0	1	0	1	1	1	1	0	1	1	1	1	0
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## Synthesis results:

- 1) Match only 100G AM0 : 41.040001 (total cell area)
- 2) Match 40G AM0 or 100G AM0 based on a select bit : 52.110001;
- 3) From the .lib files, 2-input AND gate area : 0.54;

## SUMMARY:

100G AM0 logic is  $41.04/.54 = 76$  gates

100G OR 40G AM0 logic is  $52.11/.54 = 96.5$  gates.

Differences is 20.5 gates per comparator.

Assume 48 compares per lane =  $20.5 * 48 = 984$  gates per PHY.

### **MORE AND SUMMARY.**

- **AM0 from 40G MLD running at 25G line rate reduces confusion:**
  - **AM0 from 100G MLD is the CW boundary definition for 100G FECs.**
- **PUT THE AM0 BACK TO THE 40G FORMAT**
  - **The area cost is negligible.**
  - **No effect on EEE**

**THANK YOU!**