45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the identified rows in Table 45-3 (as modified by IEEE Std 802.cd-TBD) and insert new rows immediately below the changed rows as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register Address	Title	Clause
1.29	~~Reserved~~ PMA/PMD control 3	45.2.1.23a
1.901 to 1.999 ~~1.1099~~	Reserved	
1.1000 through 1.1002	Nx25G-EPON PMA/PMD extended ability	45.2.1.134a
1.1003 through 1.1099	Reserved	-
1.2309 through 1.2399 ~~1.32767~~	Reserved	
1.2400 through 1.2537	Nx25G-EPON Synchronization Pattern	45.2.1.192
1.2538 through 1.32767	Reserved	-

Insert 45.2.1.23a after 45.2.1.23 as follows:

45.2.1.23a PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–26a.

Table 45–26a—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.29.15:6	Reserved	Value always 0	RO
1.29.5:0	PMA/PMD type selection	543210 11xxxx = Reserved 101xxx = Reserved 100111 = 50GBASE-PQX-U3 100110 = 50GBASE-PQX-U2 100101 = 50GBASE-PQX-D3 100100 = 50GBASE-PQX-D2 100011 = 50GBASE-PQG-U3	R/W

		100010 = 50GBASE-PQG-U2 100001 = 50GBASE-PQG-D3 100000 = 50GBASE-PQG-D2 011111 = 50/25GBASE-PQX-U3 011110 = 50/25GBASE-PQX-U2 011101 = 50/25GBASE-PQX-D3 011100 = 50/25GBASE-PQX-D2 011011 = 50/25GBASE-PQG-U3 011010 = 50/25GBASE-PQG-U2 011001 = 50/25GBASE-PQG-D3 011000 = 50/25GBASE-PQG-D2 010111 = 50/10GBASE-PQX-U3 010110 = 50/10GBASE-PQX-U2 010101 = 50/10GBASE-PQX-D3 010100 = 50/10GBASE-PQX-D2 010011 = 50/10GBASE-PQG-U3 010010 = 50/10GBASE-PQG-U2 010001 = 50/10GBASE-PQG-D3 010000 = 50/10GBASE-PQG-D2 001111 = 25GBASE-PQX-U3 001110 = 25GBASE-PQX-U2 001101 = 25GBASE-PQX-D3 001100 = 25GBASE-PQX-D2 001011 = 25GBASE-PQG-U3 001010 = 25GBASE-PQG-U2 001001 = 25GBASE-PQG-D3 001000 = 25GBASE-PQG-D2 000111 = 25/10GBASE-PQX-U3 000110 = 25/10GBASE-PQX-U2 000101 = 25/10GBASE-PQX-D3 000100 = 25/10GBASE-PQX-D2 000011 = 25/10GBASE-PQG-U3 000010 = 25/10GBASE-PQG-U2 000001 = 25/10GBASE-PQG-D3 000000 = 25/10GBASE-PQG-D2	

[a]R/W = Read/Write, RO = Read only

45.2.1.23a.1 Bits name (1.xxx.1:0)

Bits 1.xxx.1:0 are used to

Insert 45.2.1.134a after 45.2.1.134 as follows:

45.2.1.134a Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002)

The assignment of bits in the Nx25G-EPON PMA/PMD extended ability register is shown in Table 45–103a.

Table 45–103a—Nx25G-EPON PMA/PMD extended ability registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.1000.15	25GBASE-PQX-U3	1 = is 25GBASE-PQX-U3 compliant 0 = is not 25GBASE-PQX-U3 compliant	RO
1.1000.14	25GBASE-PQX-U2	1 = is 25GBASE-PQX-U2 compliant 0 = is not 25GBASE-PQX-U2 compliant	RO
1.1000.13	25GBASE-PQX-D3	1 = is 25GBASE-PQX-D3 compliant 0 = is not 25GBASE-PQX-D3 compliant	RO
1.1000.12	25GBASE-PQX-D2	1 = is 25GBASE-PQX-D2 compliant 0 = is not 25GBASE-PQX-D2 compliant	RO
1.1000.11	25GBASE-PQG-U3	1 = is 25GBASE-PQG-U3 compliant 0 = is not 25GBASE-PQG-U3 compliant	RO
1.1000.10	25GBASE-PQG-U2	1 = is 25GBASE-PQG-U2 compliant 0 = is not 25GBASE-PQG-U2 compliant	RO
1.1000.9	25GBASE-PQG-D3	1 = is 25GBASE-PQG-D3 compliant 0 = is not 25GBASE-PQG-D3 compliant	RO
1.1000.8	25GBASE-PQG-D2	1 = is 25GBASE-PQG-D2 compliant 0 = is not 25GBASE-PQG-D2 compliant	RO
1.1000.7	25/10GBASE-PQX-U3	1 = is 25/10GBASE-PQX-U3 compliant 0 = is not 25/10GBASE-PQX-U3 compliant	RO
1.1000.6	25/10GBASE-PQX-U2	1 = is 25/10GBASE-PQX-U2 compliant 0 = is not 25/10GBASE-PQX-U2 compliant	RO
1.1000.5	25/10GBASE-PQX-D3	1 = is 25/10GBASE-PQX-D3 compliant 0 = is not 25/10GBASE-PQX-D3 compliant	RO
1.1000.4	25/10GBASE-PQX-D2	1 = is 25/10GBASE-PQX-D2 compliant 0 = is not 25/10GBASE-PQX-D2 compliant	RO
1.1000.3	25/10GBASE-PQG-U3	1 = is 25/10GBASE-PQG-U3 compliant 0 = is not 25/10GBASE-PQG-U3 compliant	RO
1.1000.2	25/10GBASE-PQG-U2	1 = is 25/10GBASE-PQG-U2 compliant 0 = is not 25/10GBASE-PQG-U2 compliant	RO
1.1000.1	25/10GBASE-PQG-D3	1 = is 25/10GBASE-PQG-D3 compliant 0 = is not 25/10GBASE-PQG-D3 compliant	RO
1.1000.0	25/10GBASE-PQG-D2	1 = is 25/10GBASE-PQG-D2 compliant 0 = is not 25/10GBASE-PQG-D2 compliant	RO
1.1001.15	50/25GBASE-PQX-U3	1 = is 50/25GBASE-PQX-U3 compliant 0 = is not 50/25GBASE-PQX-U3 compliant	RO
1.1001.14	50/25GBASE-PQX-U2	1 = is 50/25GBASE-PQX-U2 compliant 0 = is not 50/25GBASE-PQX-U2 compliant	RO
1.1001.13	50/25GBASE-PQX-D3	1 = is 50/25GBASE-PQX-D3 compliant 0 = is not 50/25GBASE-PQX-D3 compliant	RO
1.1001.12	50/25GBASE-PQX-D2	1 = is 50/25GBASE-PQX-D2 compliant 0 = is not 50/25GBASE-PQX-D2 compliant	RO
1.1001.11	50/25GBASE-PQG-U3	1 = is 50/25GBASE-PQG-U3 compliant 0 = is not 50/25GBASE-PQG-U3 compliant	RO

1.1001.10	50/25GBASE-PQG-U2	1 = is 50/25GBASE-PQG-U2 compliant 0 = is not 50/25GBASE-PQG-U2 compliant	RO
1.1001.9	50/25GBASE-PQG-D3	1 = is 50/25GBASE-PQG-D3 compliant 0 = is not 50/25GBASE-PQG-D3 compliant	RO
1.1001.8	50/25GBASE-PQG-D2	1 = is 50/25GBASE-PQG-D2 compliant 0 = is not 50/25GBASE-PQG-D2 compliant	RO
1.1001.7	50/10GBASE-PQX-U3	1 = is 50/10GBASE-PQX-U3 compliant 0 = is not 50/10GBASE-PQX-U3 compliant	RO
1.1001.6	50/10GBASE-PQX-U2	1 = is 50/10GBASE-PQX-U2 compliant 0 = is not 50/10GBASE-PQX-U2 compliant	RO
1.1001.5	50/10GBASE-PQX-D3	1 = is 50/10GBASE-PQX-D3 compliant 0 = is not 50/10GBASE-PQX-D3 compliant	RO
1.1001.4	50/10GBASE-PQX-D2	1 = is 50/10GBASE-PQX-D2 compliant 0 = is not 50/10GBASE-PQX-D2 compliant	RO
1.1001.3	50/10GBASE-PQG-U3	1 = is 50/10GBASE-PQG-U3 compliant 0 = is not 50/10GBASE-PQG-U3 compliant	RO
1.1001.2	50/10GBASE-PQG-U2	1 = is 50/10GBASE-PQG-U2 compliant 0 = is not 50/10GBASE-PQG-U2 compliant	RO
1.1001.1	50/10GBASE-PQG-D3	1 = is 50/10GBASE-PQG-D3 compliant 0 = is not 50/10GBASE-PQG-D3 compliant	RO
1.1001.0	50/10GBASE-PQG-D2	1 = is 50/10GBASE-PQG-D2 compliant 0 = is not 50/10GBASE-PQG-D2 compliant	RO
1.1002.8:15	Reserved	Value always 0	RO
1.1002.7	50GBASE-PQX-U3	1 = is 50GBASE-PQX-U3 compliant 0 = is not 50GBASE-PQX-U3 compliant	RO
1.1002.6	50GBASE-PQX-U2	1 = is 50GBASE-PQX-U2 compliant 0 = is not 50GBASE-PQX-U2 compliant	RO
1.1002.5	50GBASE-PQX-D3	1 = is 50GBASE-PQX-D3 compliant 0 = is not 50GBASE-PQX-D3 compliant	RO
1.1002.4	50GBASE-PQX-D2	1 = is 50GBASE-PQX-D2 compliant 0 = is not 50GBASE-PQX-D2 compliant	RO
1.1002.3	50GBASE-PQG-U3	1 = is 50GBASE-PQG-U3 compliant 0 = is not 50GBASE-PQG-U3 compliant	RO
1.1002.2	50GBASE-PQG-U2	1 = is 50GBASE-PQG-U2 compliant 0 = is not 50GBASE-PQG-U2 compliant	RO
1.1002.1	50GBASE-PQG-D3	1 = is 50GBASE-PQG-D3 compliant 0 = is not 50GBASE-PQG-D3 compliant	RO
1.1002.0	50GBASE-PQG-D2	1 = is 50GBASE-PQG-D2 compliant 0 = is not 50GBASE-PQG-D2 compliant	RO

[a]RO = Read only

1 **45.2.1.134a.1 Bits name (1.xxx.1:0)**

2 text

3 **45.2.1.134a.2 Bits name (1.xxx.1:0)**

4 text

Insert 45.2.1.192 after 45.2.1.191 as follows:

45.2.1.192 Nx25G-EPON Synchronization Pattern registers (Registers 1.2400 through 1.2534)

The assignment of bits in the Nx25G-EPON Synchronization Pattern registers is shown in Table 45–155a.

Table 45–155a—Nx25G-EPON Synchronization Pattern registers bit definitions

Bit(s)	Name	Description	R/W[a]
Inclusion of Synchronization pattern definition bits is TBD			

[a]R/W = Read/Write, RO = Read only

45.2.1.192.2 Bits name (1.xxx.1:0)

text

45.2.1.192.2 Bits name (1.xxx.1:0)

text

45.2.3 PCS registers

Change the identified rows in Table 45-176 (as modified by IEEE Std 802.cd-TBD) and insert new rows immediately below the changed rows as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
3.812 through 3.899 ~~3.1799~~	Reserved	
3.900 through 3.903	BASE-Q PCS FEC corrected codewords counter	45.2.3.65a
3.904 through 3.934	Reserved	
3.934 to 3.937	BASE-Q PCS FEC uncorrected codewords counter	45.2.3.65b
3.938 to 3.1799	Reserved	

45.2.3.1 PCS control 1 register (Register 3.0)

Change the identified rows in Table 45-177 (as modified by IEEE Std 802.cd-TBD) and insert new rows immediately below the changed rows as follows (unchanged rows not shown):

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.5:2	Speed selection	5432 ~~11xx~~ 111x = reserved 1101 = 50/25 Gb/s 1100 = 50/10 Gb/s 1011 = 25/10 Gb/s 1010 = 400 Gb/s 1001 = 200 Gb/s 1000 = 5 Gb/s 0111 = 2.5 Gb/s 0110 = 50 Gb/s 0101 = 25 Gb/s 0100 = 100 Gb/s 0011 = 40 Gb/s 0010 = 10/1 Gb/s 0001 = 10PASS-TS/2BASE-TL 0000 = 10 Gb/s	R/W

45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45-180 (as modified by IEEE Std 802.cd-TBD) as follows:

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.7.15:4~~ 3.7.15:5	Reserved	Value always 0	RO
~~3.7.3:0~~ 3.7.4:0	PCS type selection	~~3210~~ 43210 10100 = Select 50GBASE-Q PCS type 10011 = Select 50/25GBASE-Q PCS type 10010 = Select 50/10GBASE-Q PCS type 10001 = Select 25GBASE-Q PCS type 10000 = Select 25/10GBASE-Q PCS type 0111x = reserved 01101 = Select 400GBASE-R PCS type 01100 = Select 200GBASE-R PCS type 01011 = Select 5GBASE-T PCS type 01010 = Select 2.5GBASE-T PCS type 01001 = Select 25GBASE-T PCS type 01000 = Select 50GBASE-R PCS type 00111 = Select 25GBASE-R PCS type 00110 = Select 40GBASE-T PCS type 00101 = Select 100GBASE-R PCS type 00100 = Select 40GBASE-R PCS type 00011 = Select 10GBASE-T PCS type 00010 = Select 10GBASE-W PCS type 00001 = Select 10GBASE-X PCS type 00000 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

Change subclause 45.2.3.6.1 as follows:

45.2.3.6.1 PCS type selection (~~3.7.3:0~~ 3.7.4:0)

The PCS type shall be selected using bits ~~3~~4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9, 3.8.7:0, and ~~3.9.1:0~~ 3.9.4:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.8 PCS status 3 register (Register 3.9)

Change Table 45-182 (as modified by IEEE Std 802.cd-TBD) as follows:

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.9.15:2~~ 3.9.15:5	Reserved	Value always 0	RO
3.9.4	2x25GBASE-Q capable	1 = PCS is able to support 2x25GBASE-Q PCS type 0 = PCS is not able to support 2x25GBASE-Q PCS type	RO
3.9.3	25GBASE-Q capable	1 = PCS is able to support 25GBASE-Q PCS type 0 = PCS is not able to support 25GBASE-Q PCS type	RO
3.9.2	10GBASE-Q capable	1 = PCS is able to support10GBASE-Q PCS type 0 = PCS is not able to support 10GBASE-Q PCS type	RO
3.9.1	400GBASE-R capable	1 = PCS is able to support 400GBASE-R PCS type 0 = PCS is not able to support 400GBASE-R PCS type	RO
3.9.0	200GBASE-R capable	1 = PCS is able to support 200GBASE-R PCS type 0 = PCS is not able to support 200GBASE-R PCS type	RO

aRO = Read only

45.2.3.8.3 Bits name (3.xxx.1:0)

Text

45.2.3.8.4 Bits name (3.xxx.1:0)

Text

Insert 45.2.3.65a, 45.2.3.65b and associated Tables and subclauses as follows:

45.2.3.65a BASE-Q PCS FEC corrected codewords counter registers (Registers 3.900 through 3.903)

The assignment of bits in the XXXXXX register is shown in Table 45–234a. XXX Text XXX

Table 45-234a—BASE-Q PCS FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.900.15:0	FEC corrected codewords lower	PCS FEC corrected codewords counter ch0 (15:0)	RO, NR
3.901.15:0	FEC corrected codewords upper	PCS FEC corrected codewords counter ch0 (31:16)	RO, NR
3.902.15:0	FEC corrected codewords lower	PCS FEC corrected codewords counter ch1 (15:0)	RO, NR
3.903.15:0	FEC corrected codewords upper	PCS FEC corrected codewords counter ch1 (31:16)	RO, NR

aRO = Read only, NR = Non Roll-over

45.2.3.65a.1 Bits name (3.xxx.1:0)

Text

45.2.3.65a.2 Bits name (3.xxx.1:0)

Text

Table 45-65b BASE-Q PCS FEC uncorrected codewords counter registers (Registers 3.904 through 3.935)

The assignment of bits in the XXXXXX register is shown in Table 45–234b. XXX Text XXX

Table 45–234b—BASE-Q PCS FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.932.15:0	FEC uncorrected codewords lower	PCS FEC corrected codewords counter ch0 (15:0)	RO, NR
3.933.15:0	FEC uncorrected codewords upper	PCS FEC corrected codewords counter ch0 (31:16)	RO, NR
3.934.15:1	FEC uncorrected codewords lower	PCS FEC corrected codewords counter ch1 (15:0)	RO, NR
3.935.15:1	FEC uncorrected codewords upper	PCS FEC corrected codewords counter ch1 (31:16)	RO, NR

aRO = Read only, NR = Non Roll-over

45.2.3.65b.1 Bits name (3.xxx.1:0)

Text

45.2.3.65b.2 Bits name (3.xxx.1:0)

Text