

# Considerations for Recovering Frame Sequence on MPCP+

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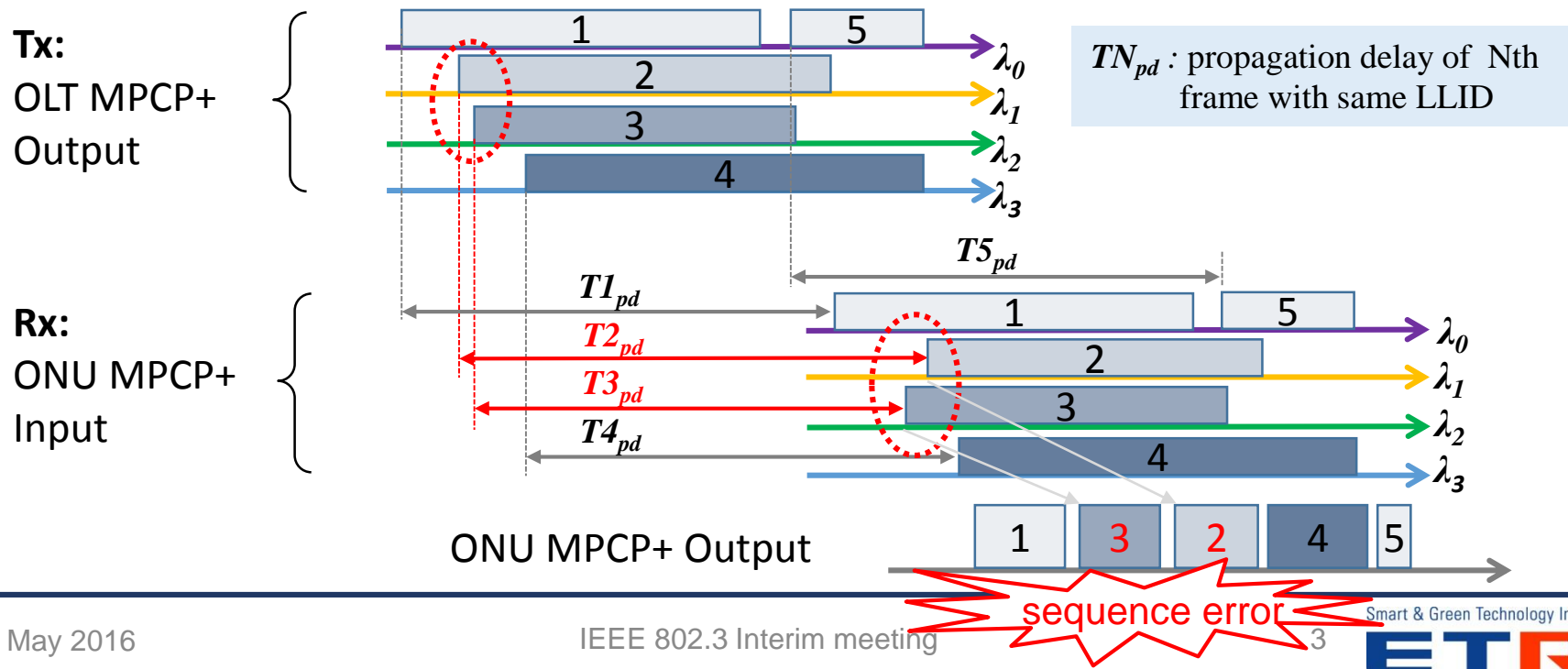
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# Background

- “MPCP+” was proposed in Macao meeting by G. Kramer
- A proposal for channel bonding at MAC control sublayer  
[http://www.ieee802.org/3/ca/public/meeting\\_archive/2016/03/kramer\\_3ca\\_2a\\_0316.pdf](http://www.ieee802.org/3/ca/public/meeting_archive/2016/03/kramer_3ca_2a_0316.pdf)
  - According to the proposed method, a frame sequence is recovered by a first bit arrival time of frame in the downstream.
  - A propagation delay on PHY layer influences the frame arrival time on all lanes.

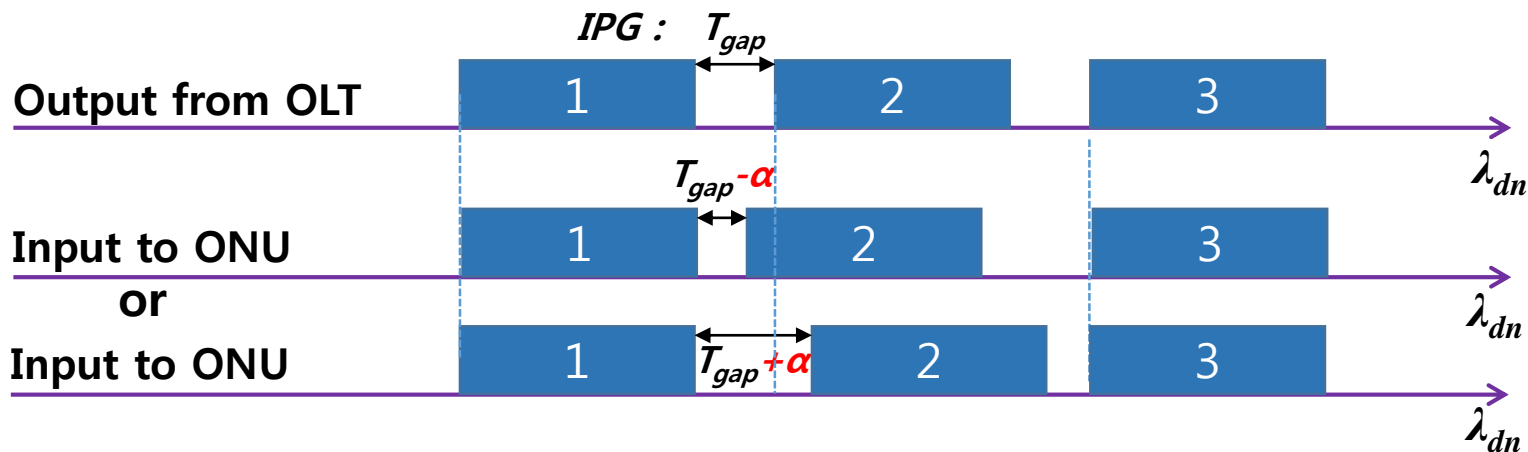
# Frame Sequence Error Caused by Drift

- If the propagation delay is not constant, namely, drift is generated, the frame sequence could be reversed.
- Example to explain the drift
  - Frame#2 starts earlier than frame#3.
  - But, frame#2 will arrive later than frame#3, when  $T2_{pd}$  is longer than  $T3_{pd}$ .
  - As a result, frame sequence error will be caused at ONU MPCP+ output.



# Is Drift Caused in 10G-EPON ?

- The drift is caused on PCS sublayer of OLT and ONU in 10G-EPON (refer to page 7-8).
  - If IPG between adjacent frames is changed in the process of IDLE deletion and IDLE insertion, drift ( $\pm\alpha$ ) is caused.



- The IEEE802.3 Spec. (77.2.2.1) defines **guardThresholdONU (128ns)**.
  - This constant holds the maximal amount of drift allowed for a timestamp received at the ONU.
- The drift would be also caused in NG-EPON, if the PCS sublayer of 10G-EPON is adopted as baseline proposal for NG-EPON.

# PCS Layer on 10G-EPON (Clause 76.3)

- IDLE Deletion

- deletes excess Idle characters to allow the parity data to be inserted without increasing the PMD line rate.

- Data Detector

- Contains a delay line (FIFO\_DD buffer) that stores the 66 bit blocks to allow insertion of the FEC parity data into the transmitted data stream.

- IDLE Insertion

- Inserts the Idle control characters to compensate for the removed FEC parity octets.

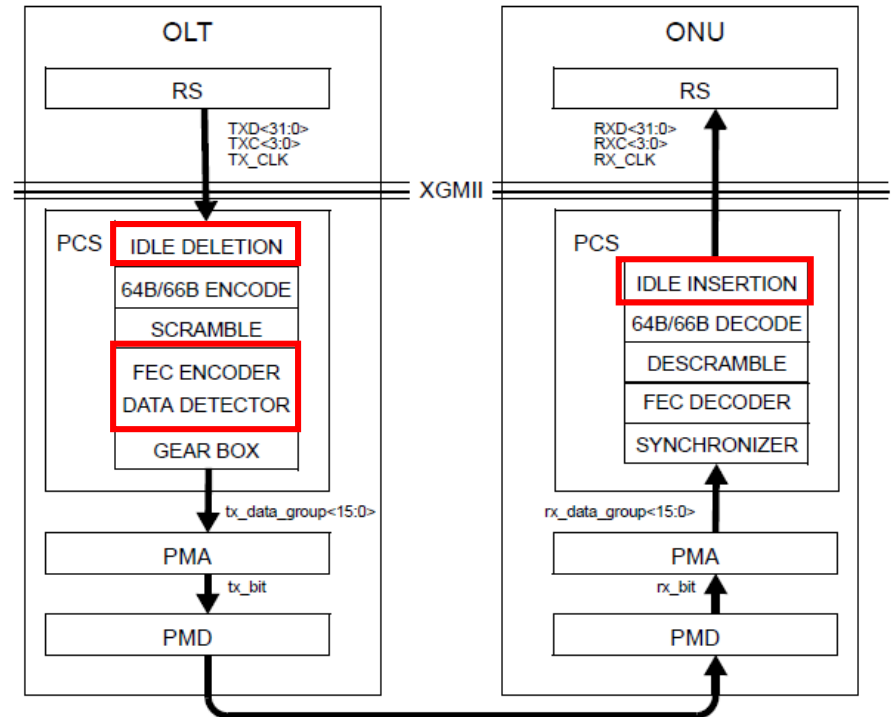
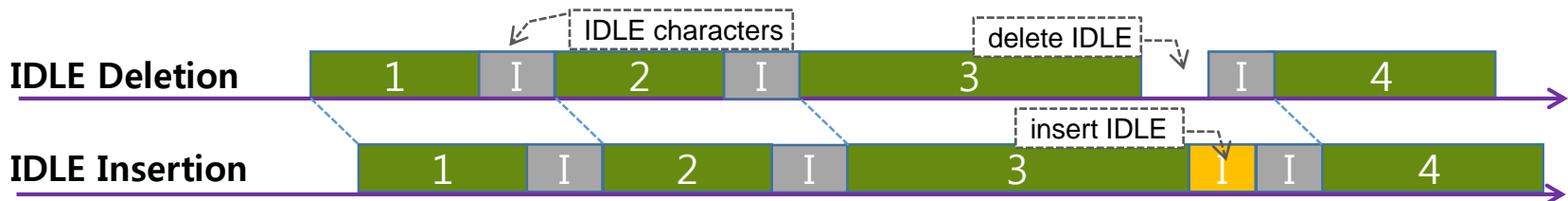


Figure 76-7—PCS functional block diagram, downstream path

# Where is Drift Caused in 10G-EPON ? (1/3)

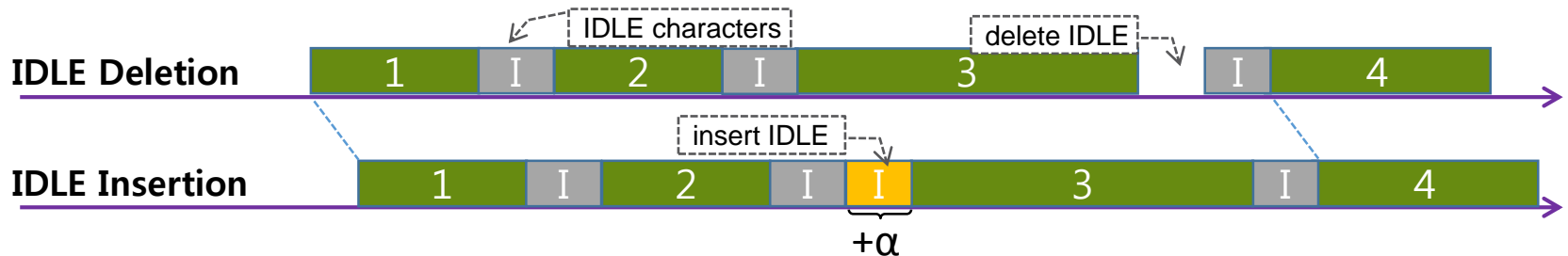
- IDLE characters are not necessarily inserted at the same locations between packets where parity blocks have been removed.  
(IEEE802.3 spec. 76.3.3.7)
  - Rx PCS does not know exactly the deleted size and position of IDLE characters.
- There must be no drift, if IDLE characters are inserted at the same location with the deleted position during on IDLE deletion.
- No drift – deletion and insertion at the same locations



# Where is Drift Caused in 10G-EPON ? (2/3)

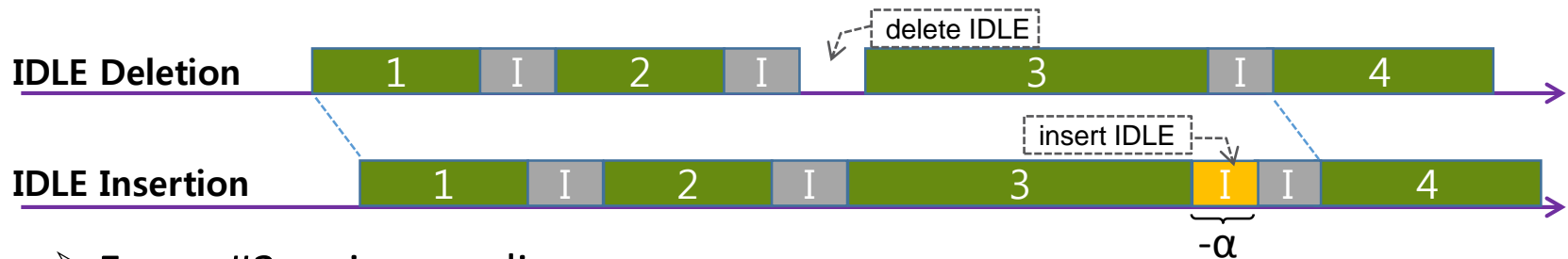
- The drift examples as follows.

Case 1) Deleted in back of frame#3, but inserted in front of frame#3



➤ Frame#3 arrives later

Case 2) Deleted in front of frame#3, but inserted in back of frame#3

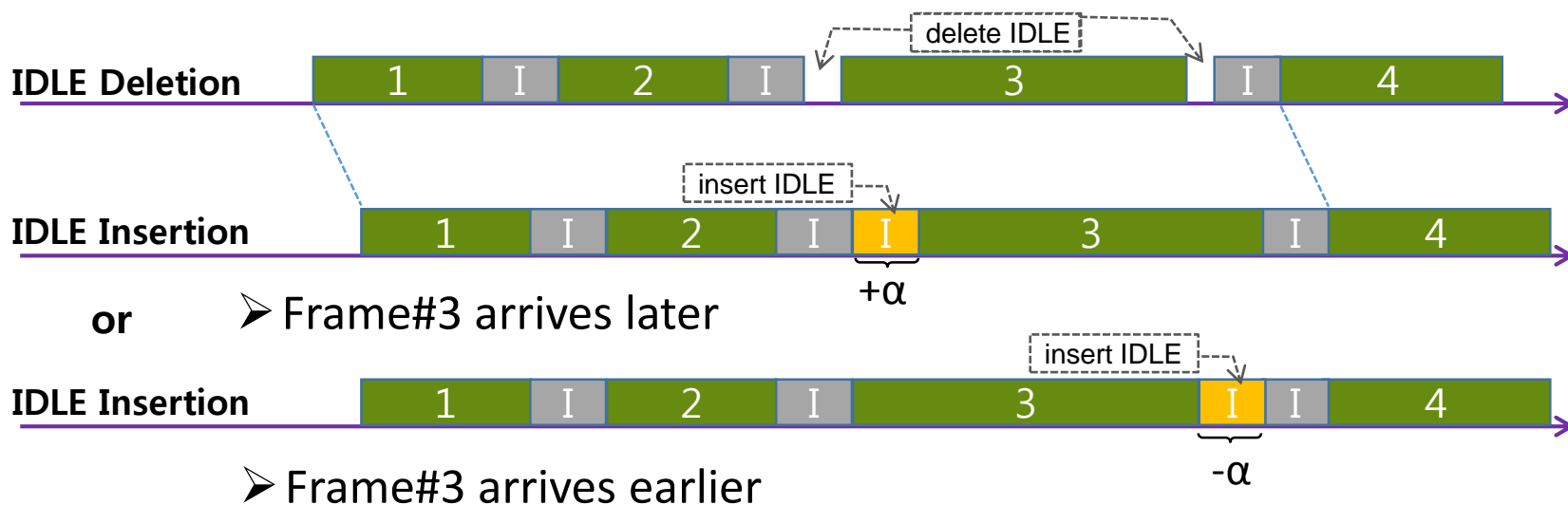


➤ Frame#3 arrives earlier

# Where is Drift Caused in 10G-EPON ? (3/3)

- The drift examples as follows.

Case 3) Deleted partially in front and back of frame#3, then inserted in front or back of frame#3

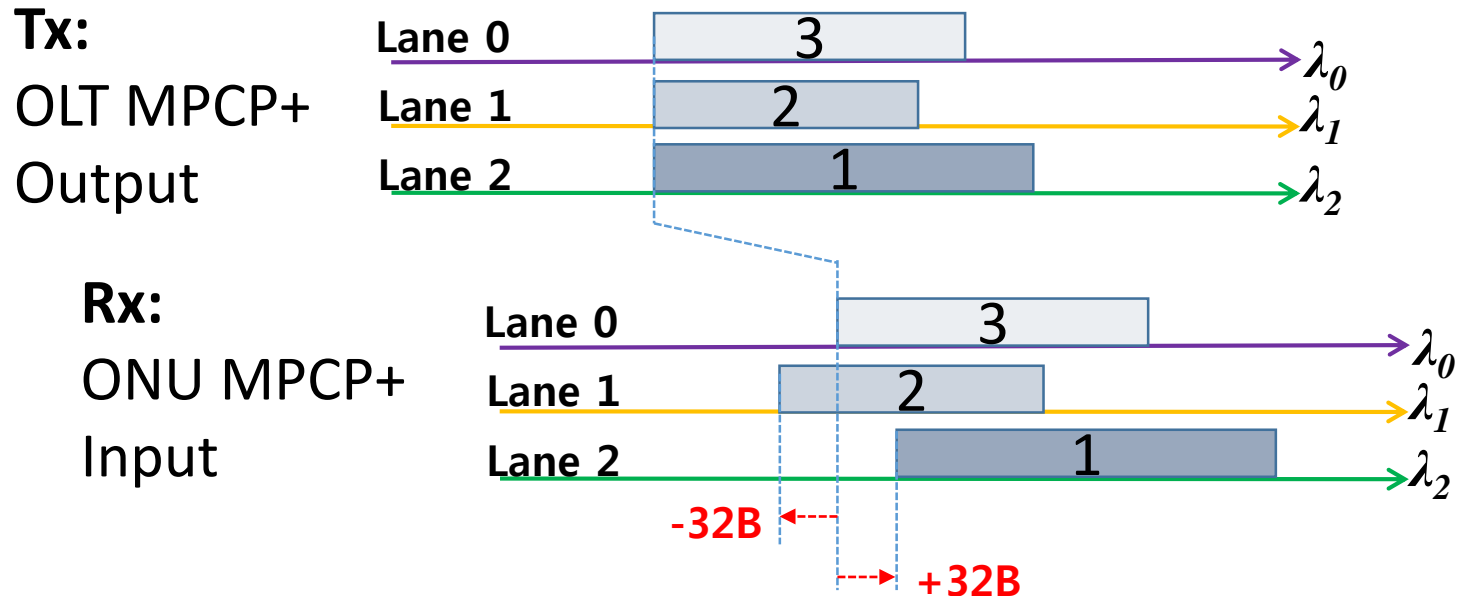


- There must be drift, if IDLE characters are inserted at the different location where these have been deleted.



# Drift between Lanes

- If a drift size is equal to FEC Parity size (32B), the drift size between lanes can be up to 64B
  - lane1 : -32B, lane2: +32B
- The drift of more than 64B would be caused, if 10G-EPON FEC is also applied to NG-EPON FEC



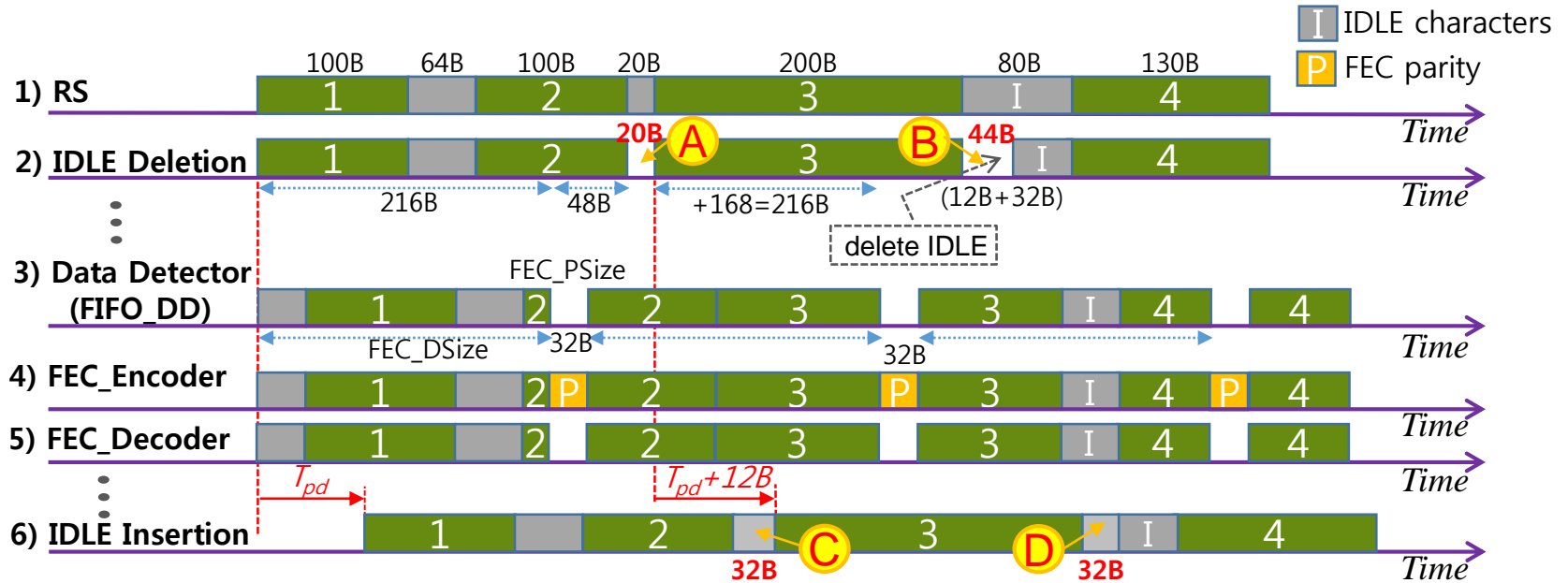
# Summary

- The arrival order of frames could be reversed by the drift on PHY layer.
- Therefore, in NG-EPON, the method to fasten the propagation delay or to get it over should be considered on PHY layer or MPCP+ sublayer.

# Backup

# Where is Drift caused in 10G-EPON ? - Example

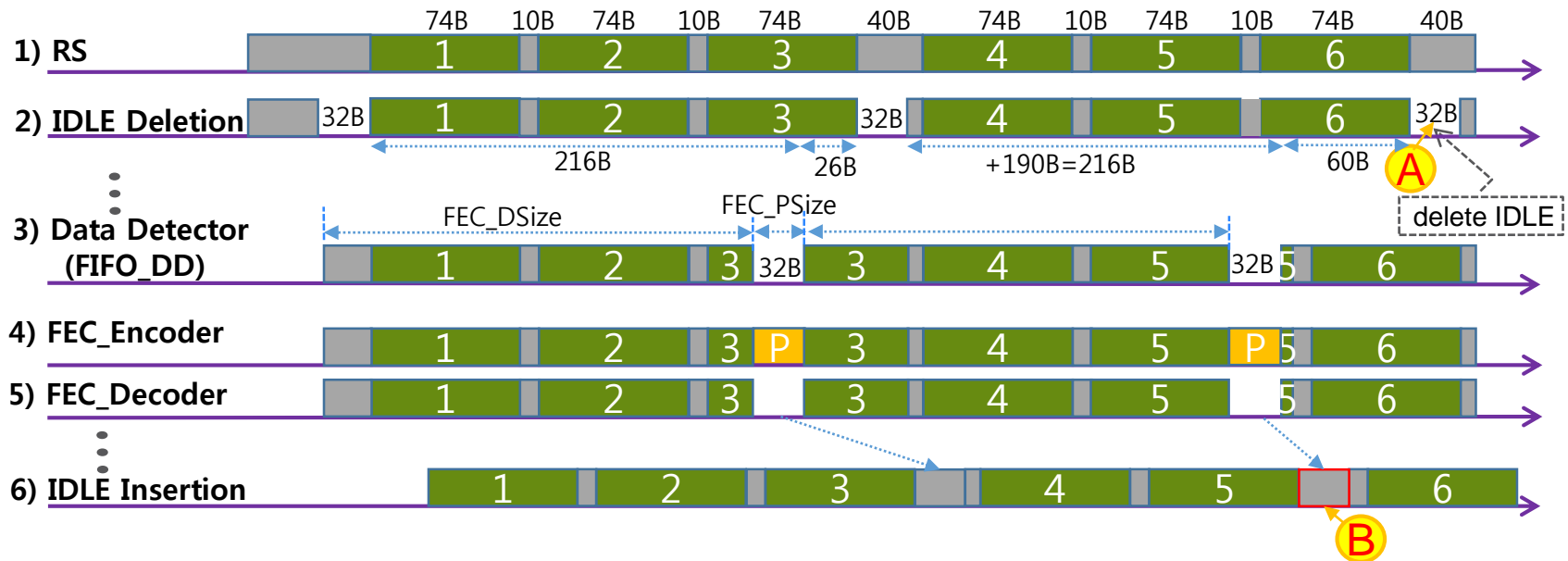
- Data output from each sub-block in OLT and ONU PCS layer (using short frame)



- IPG could be changed, because IDLE characters are not necessarily inserted at the same locations between packets where parity blocks have been removed (76.3.3.7 of IEEE802.3)
  - RS outputs frames of various lengths; sufficient Idle characters occur so that the minimum IPG is always preserved between two adjacent frames
  - IDLE Deletion deletes 20B at A and 44B at B to delete 32B IDLE characters per every 216B data
  - IDLE Insertion inserts 32B at C and D each – Is it possible that 20B are inserted at C ?
  - As a result, processing time of frame3 ( $T_{pd}+12B$ ) is longer than that of frame1 ( $T_{pd}$ )

# Drift Size

- Data output from each sub-block in OLT and ONU PCS layer (using short frame)



- Drift might be caused up to  $\pm 32\text{B}$  (FEC\_Psize) in the process of IDLE deletion and IDLE insertion
  - 32B IDLE characters are deleted at the back of frame #6 (A), but these are inserted in the front of frame #6 (B)
  - Frame #6 arrives 32B later than other frames; drift : +32B
  - If it arrives 32B earlier, then drift is -32B