Support for Time Synchronization Service Interface (TSSI), IEEE Std 802.3, Clause 90

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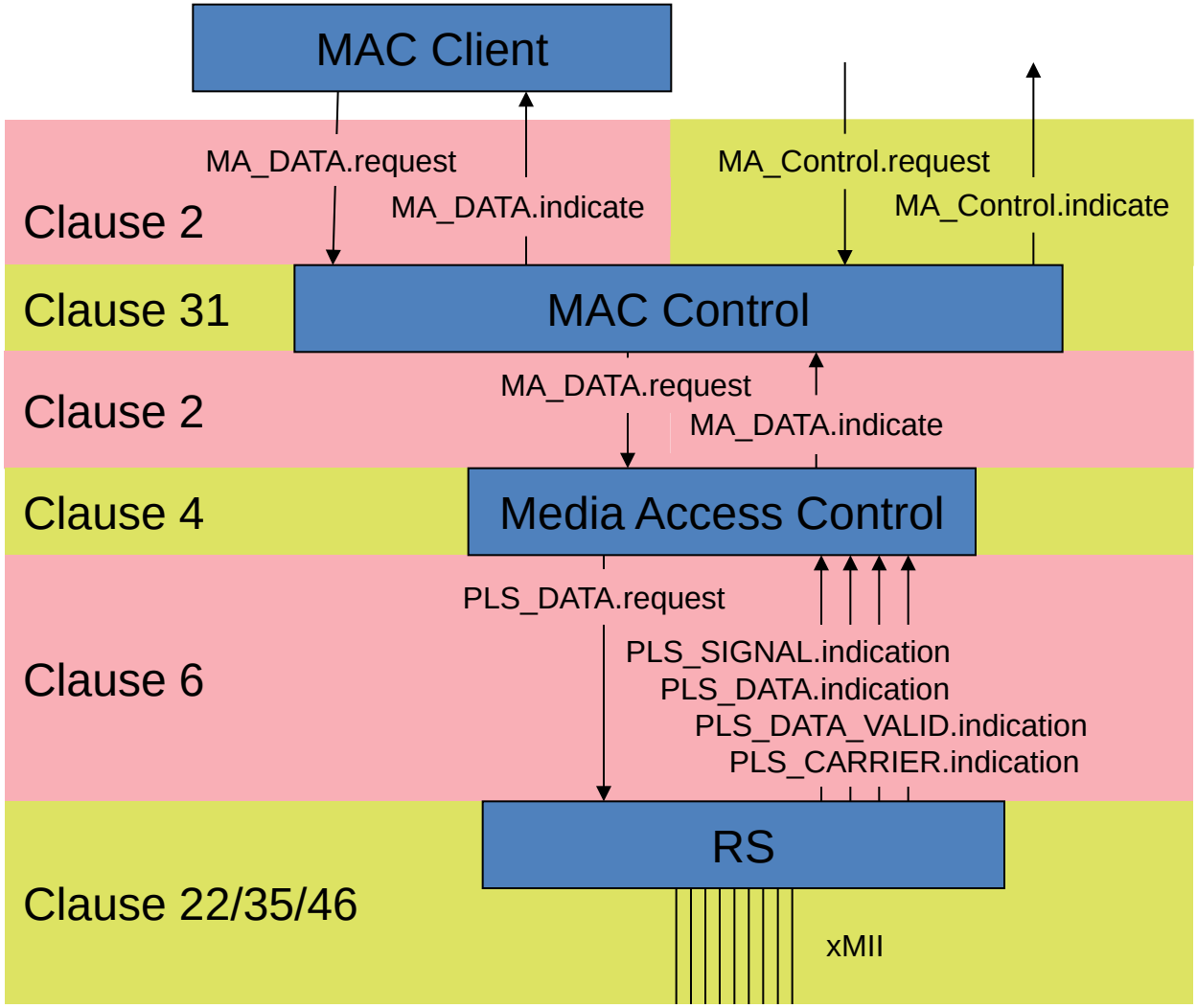
Review of sublayers and interfaces



Abstract Service Interface

- Clause 2 MAC Service Interface example

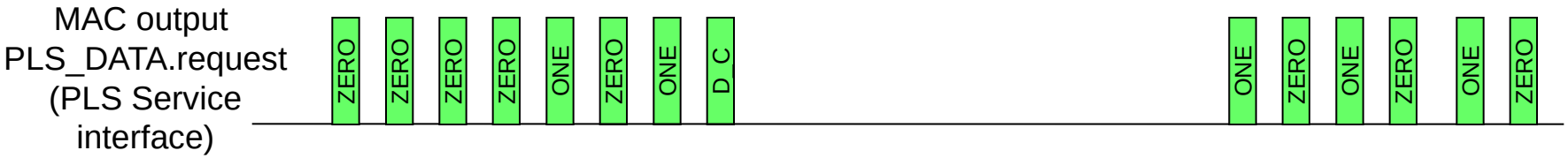
  MA_DATA.request (destination_address, source_address, mac_service_data_unit, frame_check_sequence)

  This primitive defines the transfer of data from a MAC client entity to a single peer entity or multiple peer entities in the case of group addresses.

- Clause 6 Physical Signaling (PLS) service Interface example

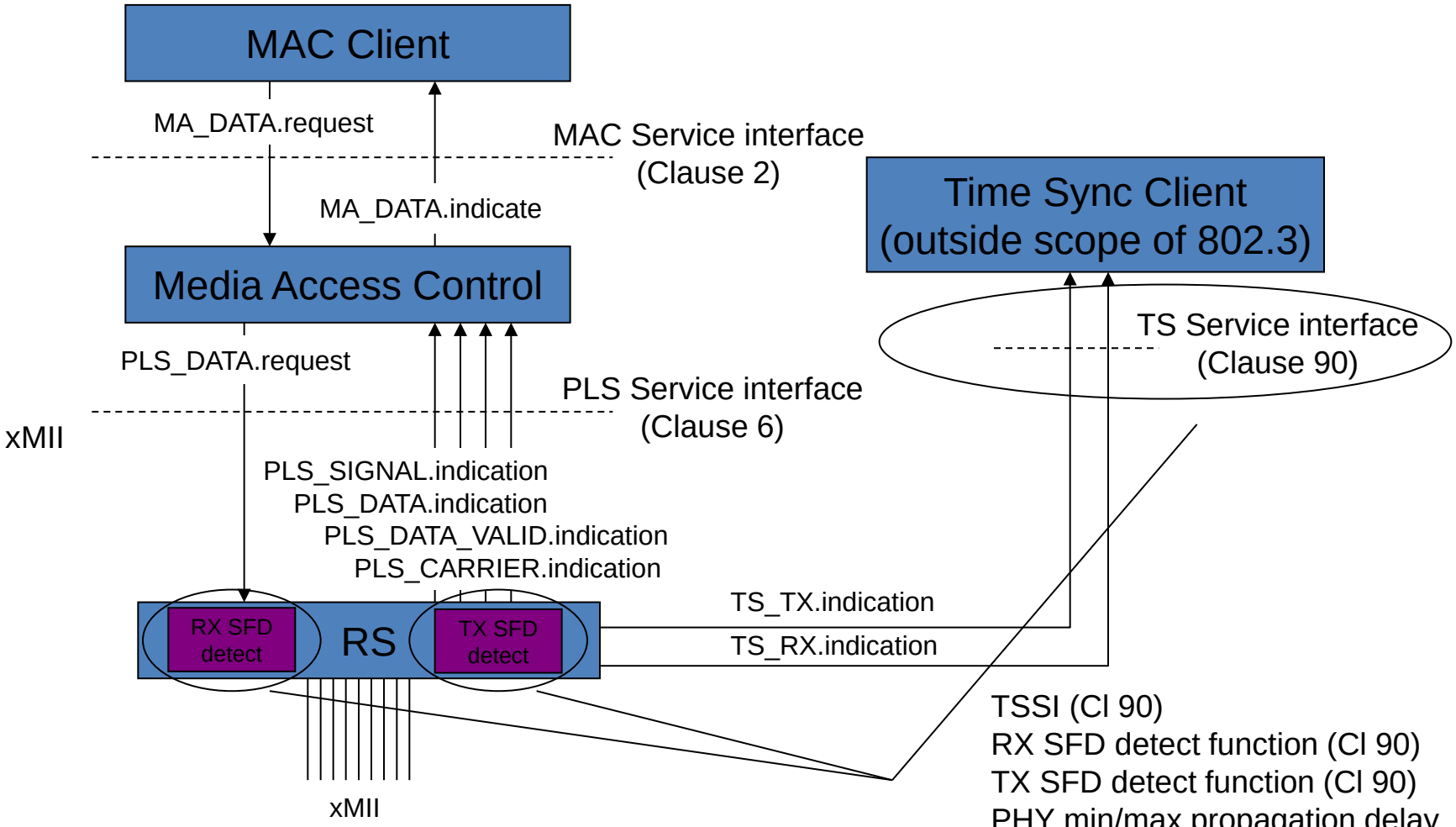
  PLS_DATA.request (OUTPUT_UNIT)

  The OUTPUT_UNIT parameter can take on one of three values: ONE, ZERO, or DATA_COMPLETE and represent a single data bit. The DATA_COMPLETE value signifies that the Media Access Control sublayer has no more data to output.



NOTE – The above is only an **illustration** of the abstract messages passing interface – messages are instantaneous

IEEE 802.3bf (Cl90) architecture



IEEE 802.3bf (Cl90) architecture

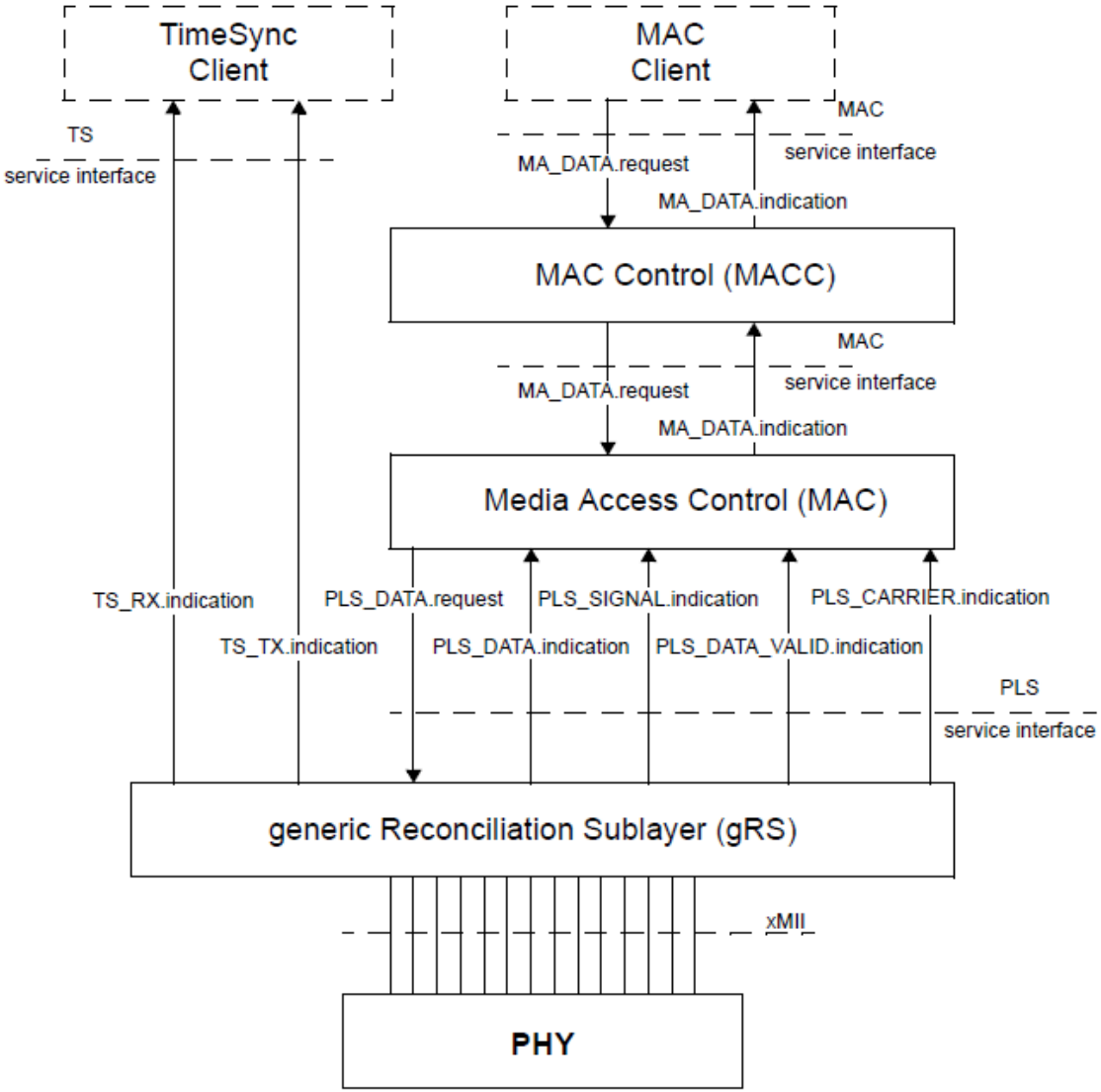
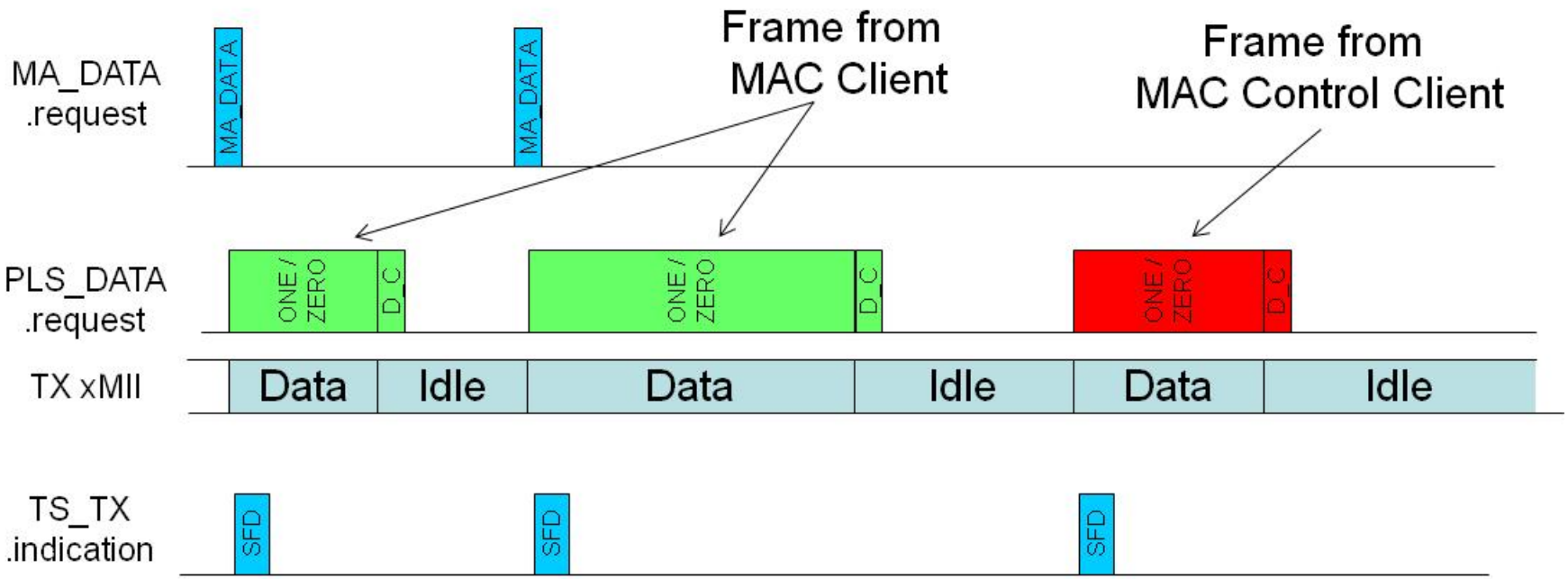


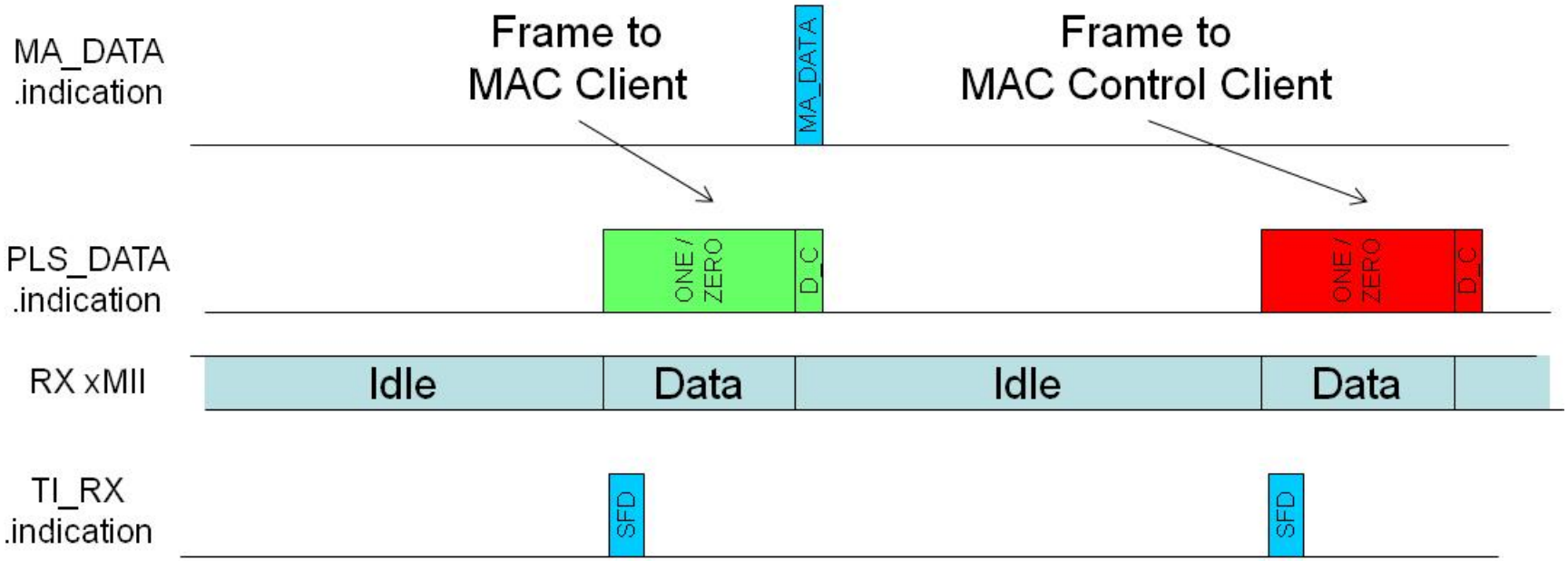
Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Interface operation – TX path



- Represents operation in the transmit direction
- TS_TX.indication is generated for all frames detected at xMII using TS_SFD_Detect_TX function: both data and control frames generate SFD indication
- Correlation between SFD indication and frame transmission is needed in the Synchronization MAC Client

Interface operation – RX path



- Represents operation in the receive direction
- TS_RX.indication is generated for all frames detected at xMII using TS_SFD_Detect_RX function: both data and control frames generate SFD indication
- Correlation between SFD indication and frame transmission is needed in the Synchronization MAC Client

Delay measurement

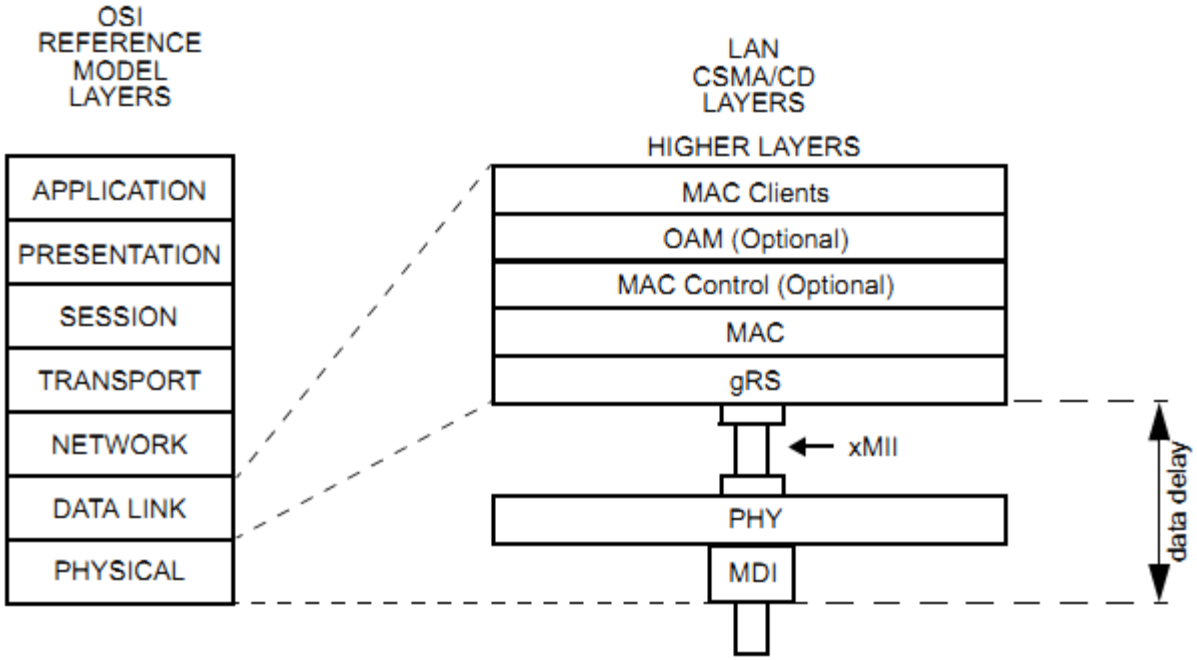


Figure 90–3—Data delay measurement

- Performed between the bottom of MDI and top of xMII
- Covers the absolute min/max delay in transmit/receive path for:
  - Whole path (managed objects in clause 30), representing the total of delays for all instantiated sublayers (registers in Clause 45)
  - Individual instantiated sublayers (registers in Clause 45)

Clause 30 objects

- Added oTimeSync entity in 30.13 (optional), containing a series of object class attributes
  - **aTimeSyncCapabilityTX / aTimeSyncCapabilityRX**: true if the TimeSync capability is supported in the transmit / receive path and false otherwise. Calculated based on the status of TimeSync support for instantiated MDIO registers in existing sublayers
  - **aTimeSyncDelayTXmax / aTimeSyncDelayTXmin**: the maximum / minimum transmit data delay as specified in 90.7, expressed in units of ns. Corresponds to the total maximum / minimum for transmit path delay for PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC sublayers, when present.
  - **aTimeSyncDelayRXmax / aTimeSyncDelayRXmin**: the maximum / minimum receive data delay as specified in 90.7, expressed in units of ns. Corresponds to the total maximum / minimum for receive path delay for PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC sublayers, when present

Clause 45 registers

- Implemented in all PMD sublayers, i.e. PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC
- Register set for each sublayer is composed of the following elements:
  - Capability register X.1800 (2 octets), with independent indication for receive and transmit data path
  - Transmit path data delay register X.1801 – X.1804 (2 × 4 octets), which stores 4 octets representing maximum and 4 octets representing minimum transmit path data delay for the given sublayer
  - Receive path data delay register X.1805 – X.1808 (2 × 4 octets), which stores 4 octets representing maximum and 4 octets representing minimum receive path data delay for the given sublayer
- Clause 45 registers and Clause 30 objects map into each other as defined in Clause 30 object definitions

Clause 45 registers (Summary)

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Table 90–1—Summary of TimeSync features in Clause 45

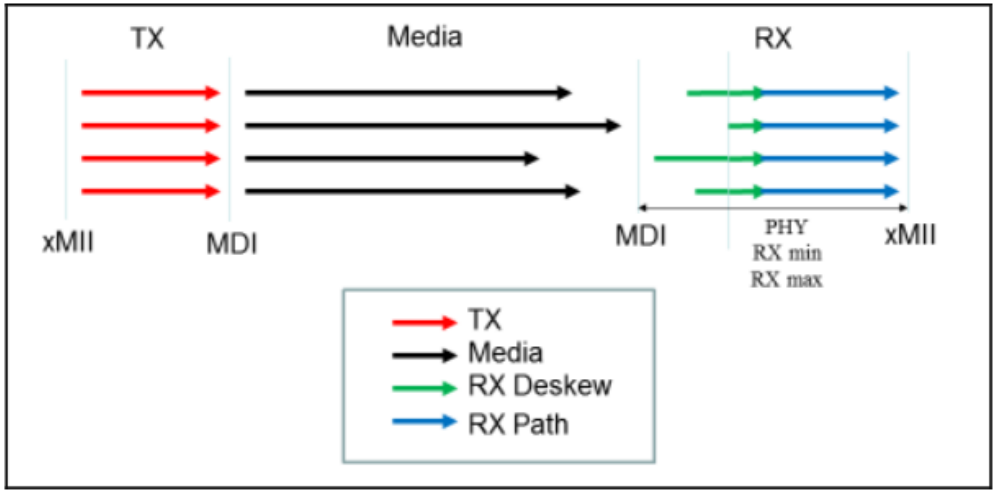
Register	Name	Reference
1.1800	TimeSync PMA/PMD capability register	45.2.1.100
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.101
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.102
2.1800	TimeSync WIS capability register	45.2.2.20
2.1801 through 2.1804	TimeSync WIS transmit path data delay	45.2.2.21
2.1805 through 2.1808	TimeSync WIS receive path data delay	45.2.2.22
3.1800	TimeSync PCS capability register	45.2.3.40
3.1801 through 3.1804	TimeSync PCS transmit path data delay	45.2.3.41
3.1805 through 3.1808	TimeSync PCS receive path data delay	45.2.3.42
4.1800	TimeSync PHY XS capability register	45.2.4.10
4.1801 through 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.11
4.1805 through 4.1808	TimeSync PHY XS receive path data delay	45.2.4.12
5.1800	TimeSync DTE XS capability register	45.2.5.10
5.1801 through 5.1804	TimeSync DTE XS transmit path data delay	45.2.5.11
5.1805 through 5.1808	TimeSync DTE XS receive path data delay	45.2.5.12
6.1800	TimeSync TC capability register	45.2.6.14
6.1801 through 6.1804	TimeSync TC transmit path data delay	45.2.6.15
6.1805 through 6.1808	TimeSync TC receive path data delay	45.2.6.16

Support for 802.3bf in 100G-EPON

- **The WHY**:
  - provides standardized support for PHY-level latency measurements for precision time and/or frequency distribution, including IEEE 1588v2/3, IEEE 802.1AS, and others
- **The HOW**:
  - add mandatory support for Clause 45 register set in PMA/PMD and PCS sublayers (see previous slides for registers) to allow vendors report min/max latency through the given sublayer
  - all latency calculations are performed in MAC Clients above 802.3 layers – no added complexity for IEEE P802.3ca standard
  - latency updates can be performed statically (fixed values provided at manufacturing time) or dynamically (updated periodically by device) – decision is at vendor discretion, no need for standard specification
  - RS layer specification needs to reference TS_TX.indication and TS_RX.indication signals, pointing back to IEEE Std 802.3, Clause 90 (specifically, 90.5.1 and 90.5.2, respectively)

Support for multi-lane PHYs (1)

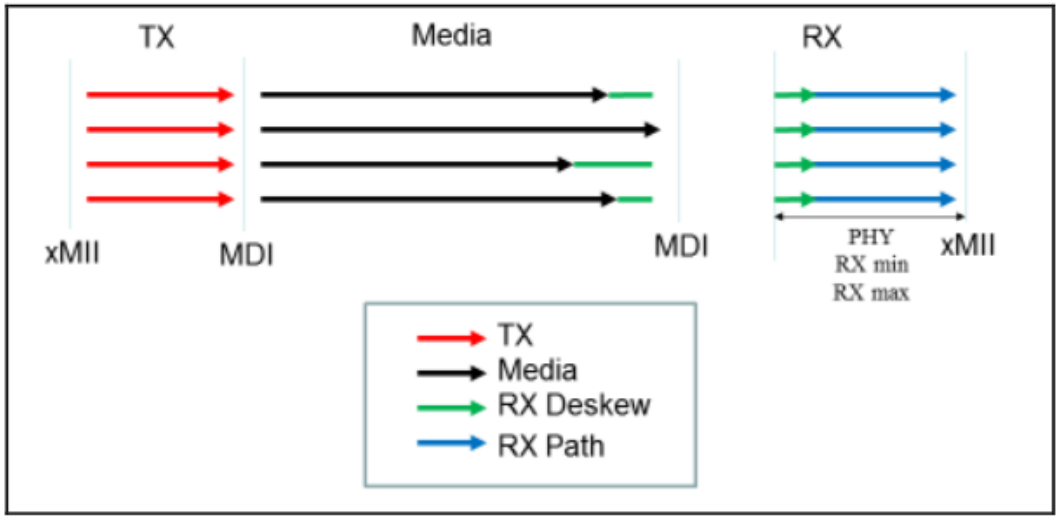
- **The PROBLEM**:
  - in existing 802.3 multi-lane PHYs, packets are striped bit-wise across multiple lanes, causing additional jitter for time-sensitive packets used to perform delay measurement
  - Without a definition of which lane of the MDI is used as the timing reference point, the entire inter-lane skew may need to be accounted for in the receive minimum and receive maximum path data delay register values.



  - For detailed description of the problem, see: http://www.ieee802.org/3/ad_hoc/timestamp/timestamping_V1p0.pdf

Support for multi-lane PHYs (2)

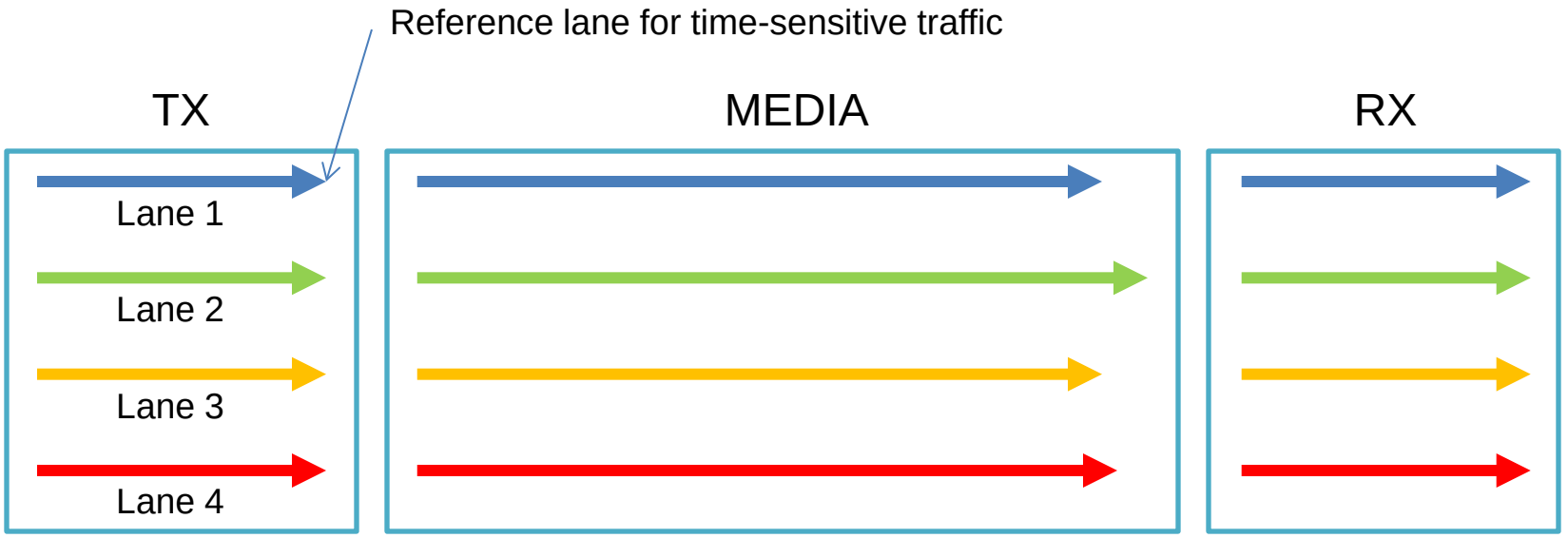
- **The SOLUTION**:
  - Use the arrival of the SFD on the slowest lane of the MDI as the receive path reference point. This will have the effect of associating alignment delay in excess of the slowest lane on the other lanes to the media, and reducing the delay uncertainly to that of the maximum skew variation of 4ns.



  - For detailed description of the problem, see: http://www.ieee802.org/3/ad_hoc/timestamp/timestamping_V1p0.pdf
  - For approved maintenance request, see: http://www.ieee802.org/3/maint/requests/maint_1286.pdf

Support for multi-lane PHYs (3)

- **<u>The 100G-EPON CASE</u>**:
  - The issue does not affect 100G-EPON under development. Each data lane (wavelength) carries complete frames. No bit-wise striping across all available data lanes is even considered for 100G-EPON.
  - For delay measurement consistency, it is suggested that a single lane is *always* used for transmission of all time-sensitive data, e.g., lane 1, shared by all ONUs on the PON (if such wavelength allocation is selected)



Motion

Adopt the mandatory support for Time Synchronization Service Interface (TSSI) defined in IEEE Std 802.3, Clause 90 and register set for PMA/PMD (1.1800-1.1808) and PCS (3.1800-3.1808) defined in IEEE Std 802.3 Clause 45, as outlined in slide 11.

Moved by:

Seconded by:

Yes

No

Abstain

THANK YOU!