Security Level:

# Feasibility and economy analysis on 25G in C-band assisted with DSP

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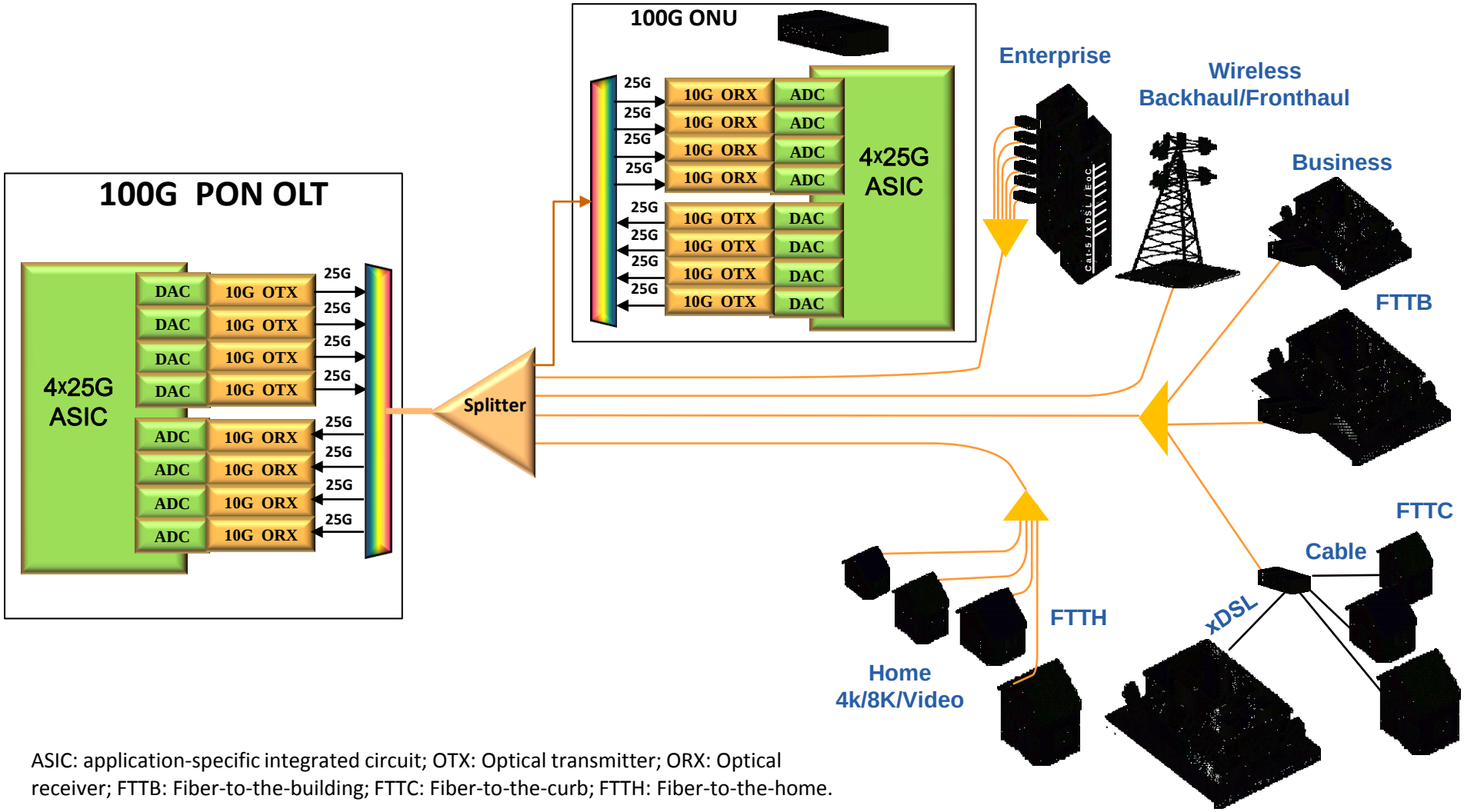
# Introduction

- Put all wavelength in O-band will result in very narrow channel width for all channels, small downstream/upstream separation, which will increase the cost of optics distinctly.

- Plan D , which puts the downstream channels in S/C band, can overcome these issues but brings the dispersion migration issue.

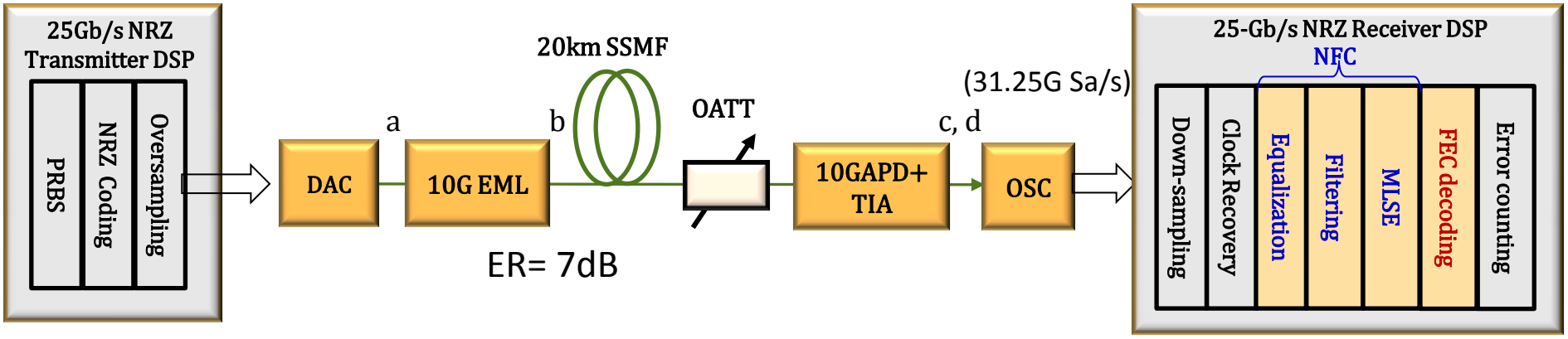
- This contribution analyzes the technical feasibility and economy of dispersion migration in C-band based on DSP.

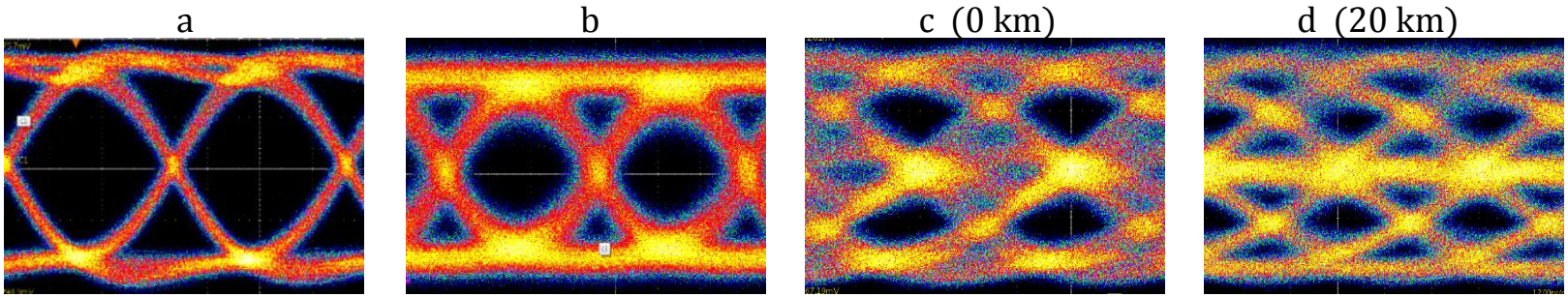
# oDSP-assisted 100G-PON system




ASIC: application-specific integrated circuit; OTX: Optical transmitter; ORX: Optical receiver; FTTB: Fiber-to-the-building; FTTC: Fiber-to-the-curb; FTTH: Fiber-to-the-home.

# 25G oDSP PON Proof-of-Concept

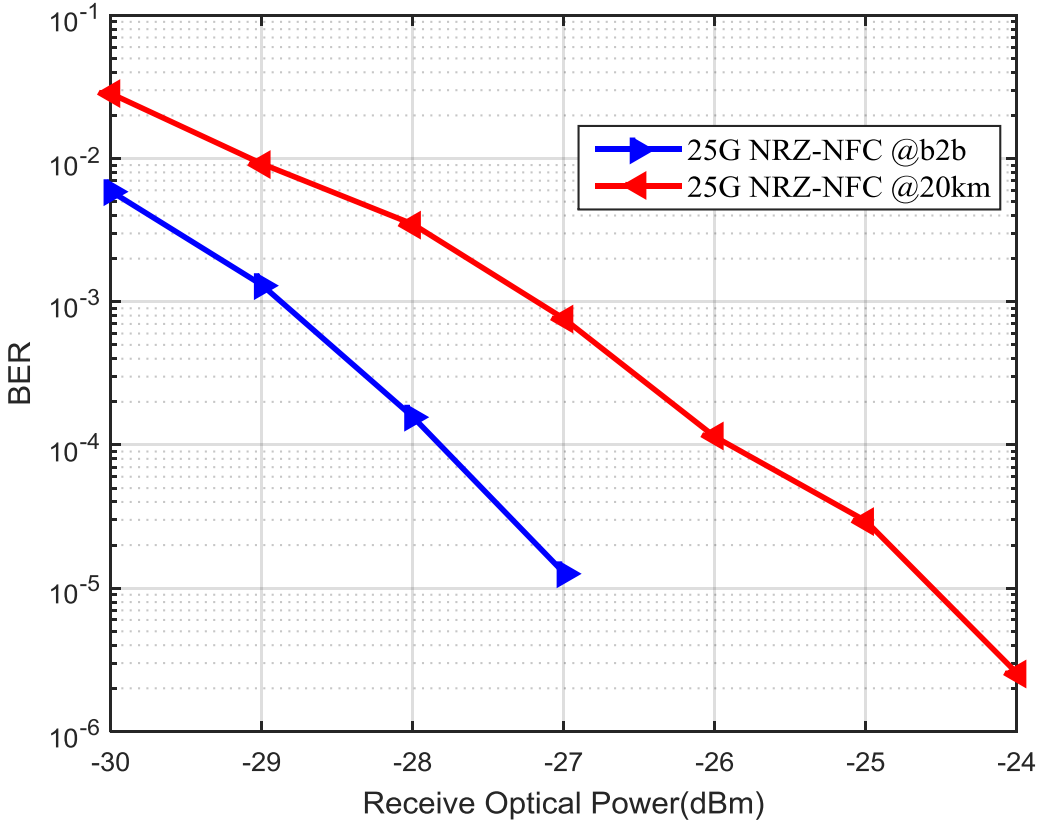



| Optics and Electronics Design | |
|---|---|
| Component | BW @ 3dB |
| DAC | 15 GHz |
| 10G EML | 14 GHz |
| 10G APD | 7.5 GHz |
| Wavelength band | C band |

- NRZ-NFC is implemented to compensate/mitigate the inter-symbol interference (ISI) caused bandwidth limitations and fiber dispersion
- Commercially available 10G EML/APD are used for low-cost implementation
- NFC： Narrow band filter compensation

# 25G DSP PON Performance




**Key Performance**

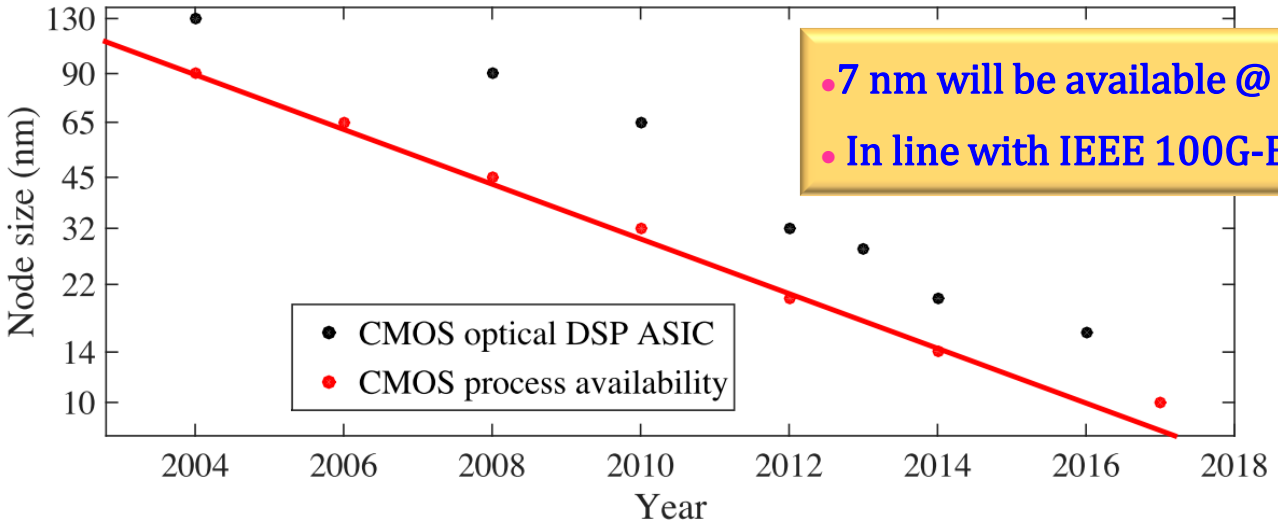
- ❑ Raw data rate: 25Gb/s
- ❑ Receiver Sensitivity :
- ❑ - 28.8dBm @ $1X10^{-3}$ , OBTB
  - 27.3dBm @ $1X10^{-3}$ , 20km fiber
- ❑ Optical Power Budget (with 5-dBm EML power)
  32.3dB @ 20km, C-Band

**Advantages:**

- ❑ **High receiver sensitivity**
  via advanced DSP and optics
- ❑ **High optical power**
  32.3dB
- ❑ **Low CD penalty**
  via channel equalization in DSP

# Development of CMOS Tech

## Predicting the future – node size




- 7 nm will be available @ 2019
- In line with IEEE 100G-EPON Standard

- Moore's law slowing up – 10 nm now expected 2017 Update with 20 nm for 2015 and 16 nm for 2016 (NEC) – projection is 10 nm for 2017, 7 nm 2019, 5 nm 2021

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S. J. Savory, "*Digital Signal Processing for Multilevel Modulation Formats*," in Proc. European Conference on Optical Communication, Tu.2.A.1 (2016).

# Power Consumption vs. CMOS Tech

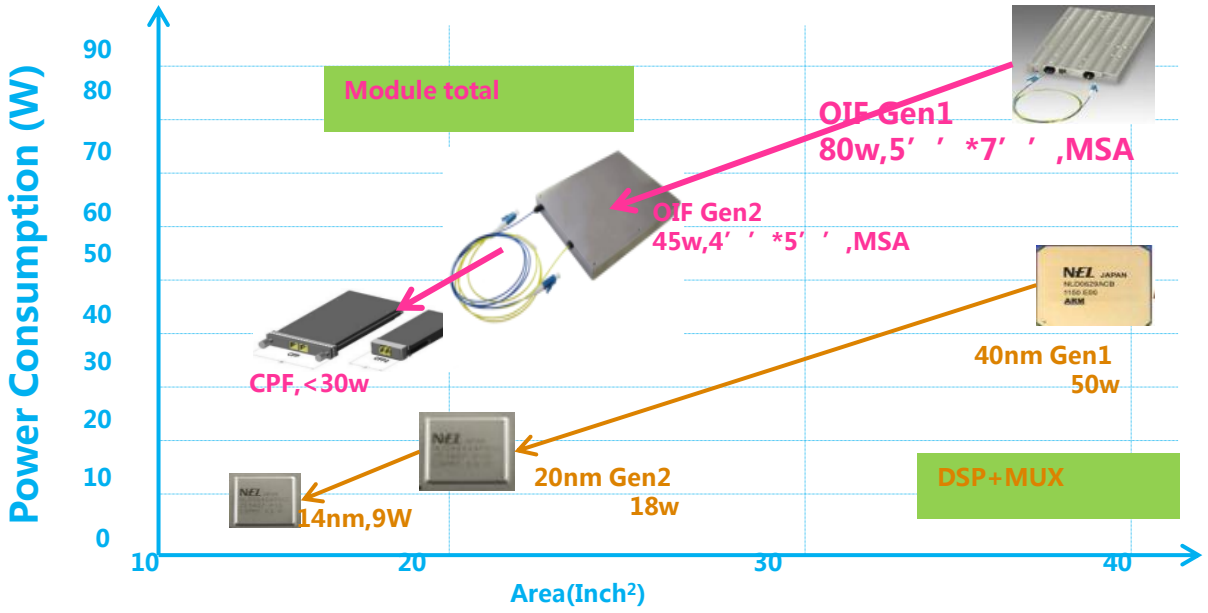
100G coherent DSP evolution (From NTT)

| | | Gen1 | Gen2 | Gen3 |
|---|---|---|---|---|
| CMOS process | | 40-nm | 20-nm | 16-nm |
| Sample release | | 2011 | 2014 | 2016 |
| Power consumption for 100Gbs | | 60 W * | 18 W | 9 W |
| OSNR Tolerance | 100G DP QPSK | 12 dB | 12 dB | 10 ~ 11 dB* |
| | 200G DP 16QAM | N. A. | N. A. | 17 ~ 18 dB* |
| CD compensation capability | | 40,000 ps/nm | 55,000 ps/nm | 80,000 ps/nm |
| Line-side features | 4ch ADC | ✓ | ✓ | ✓ |
| | 4ch DAC, Nyquist | | ✓ | ✓ |
| | NL Compensation | | | ✓ |
| Client-side features | 10x 10/11G | ✓ | ✓ | ✓ |
| | OTU4 GFEC | | ✓ | ✓ |
| | 4x 25/28G | | | ✓ |
| | 100GE bj FEC | | | ✓ |

*http://www.ntt-electronics.com.html

- For 4*25 G coherent DSP:
  - Power consumption<10W
- Coherent DSP algorithm is much more complex with that of 25G DSP-PON, such as higher complexity in polarization multiplexing detection, equalization, and FEC.
- It is estimated that 25G DSP-PON only need less than quarter logic gates of that Gen3 coherent DSP.
- **Believe that, with the driving of CMOS process, when using *7nm* CMOS technology, 25G DSP-PON's power consumption would be less than *1W*.**

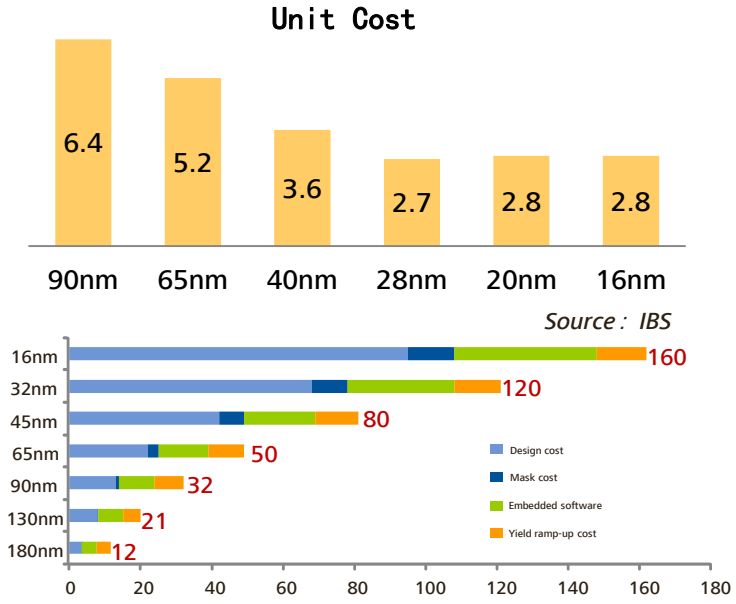
# Area vs. CMOS Tech

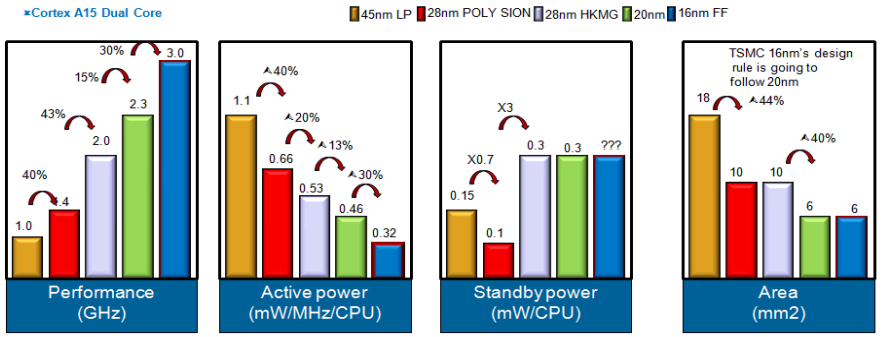


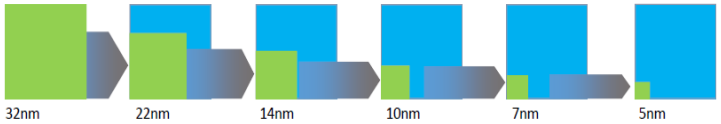

*http://www.ntt-electronics.com.html

- For 4*25 G coherent DSP:
  - Package-dimension<13.4 inch2 based on 16nm
- With the using of *7nm* CMOS technology and low complex DSP algorithm, 25G DSP ASIC area will be accepted in PON application.

# Cost vs. CMOS Tech



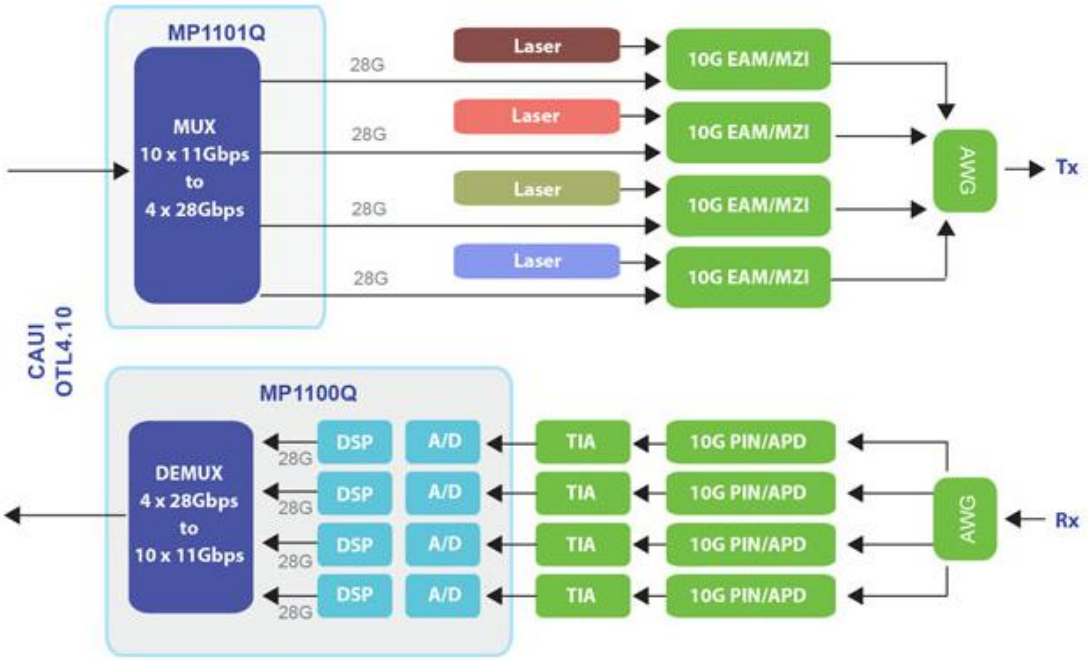




Same circuitry ~ half the space (cost reduction) OR Twice the circuitry in the ~ same space (architectural innovation) = Optimized by design for best performance/cost

- Moore's law is the first failure in the cost , the main driver is the power / density.
- The present high price of oDSP chip are due to lacking of volume, design cost is still a considerable cost in the price.
- Design cost will be shared by the large volume application of PON, so the cost will decrease dramatically when volume goes into million unit, It is estimated that cost of 25G DSP ASIC in volume would be comparable with current 10G APD chip.

# Commercial oDSP Application in 100G Metro

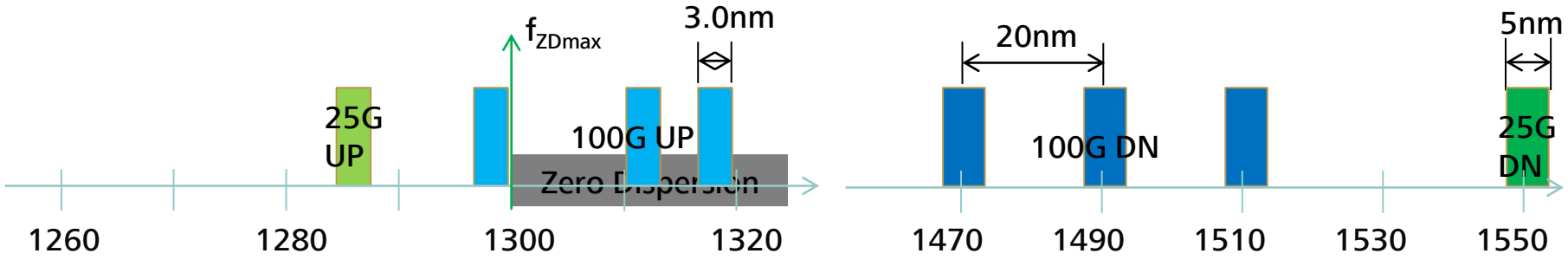



***100G Transceiver Chipset***


http://www.multi-phy.com/en-us/home.aspx

- The MP1100Q/MP1101Q from MultiPhy has successfully solved the problem of inter-symbol interference (ISI) caused by bandwidth limitations and fiber dispersion in metro and data center applications.

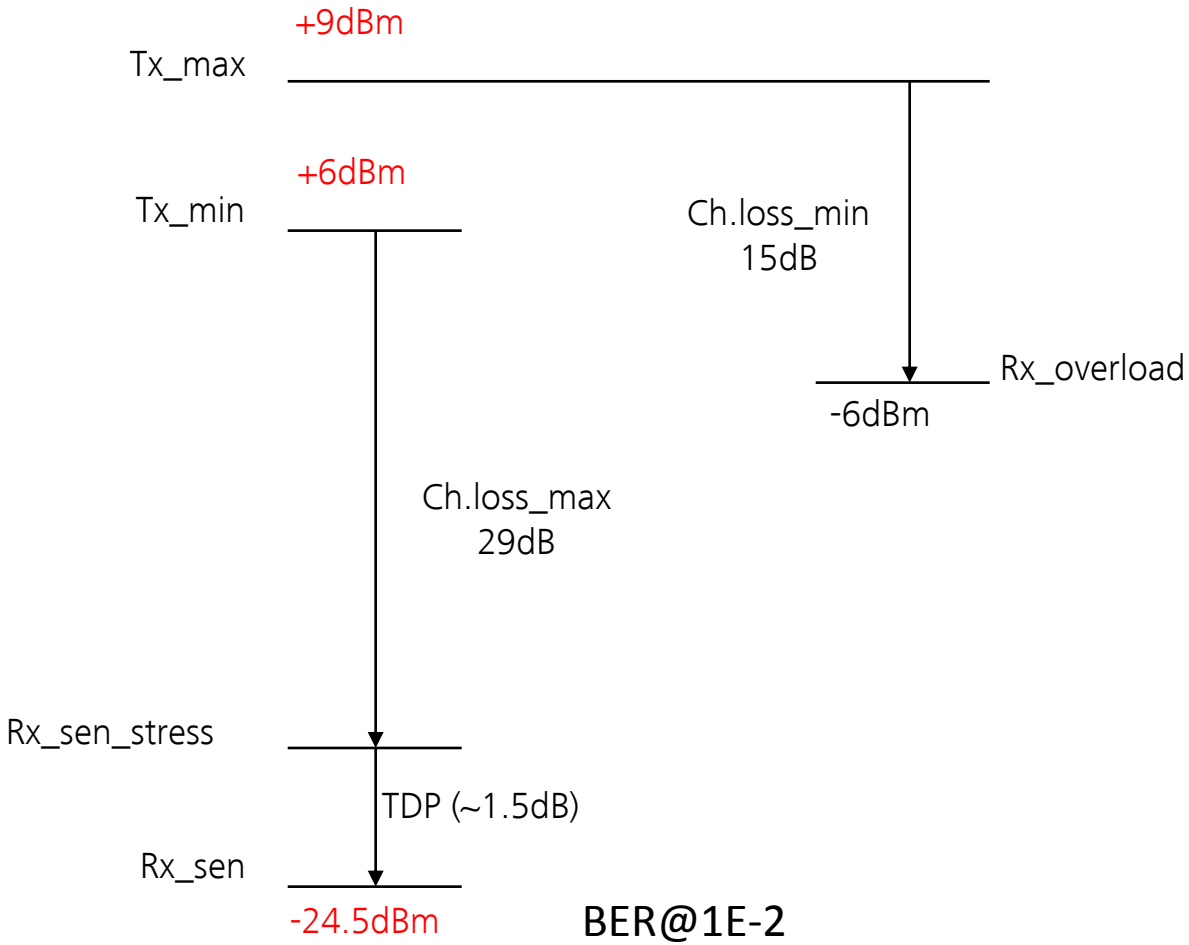
# Plan D’ wavelength plan




- Downstream are 20nm channel spacing, 5nm channel width, more than 150nm DS/US gap.
- 1524~1544nm are intentionally kept unoccupied, enabling coexistence with NG-PON2 , which will help the next generation EPON/GPON standard convergence.
- 3nm width for each upstream channel, much wider guard band, which will help to lower down the ONU cost.
- If the maximal ONU launch power can be limited to less than 5dBm, wider channel width can be further allowed.
- The chromatic dispersion of the downstream can be migrated with 10G APD assisted by DSP technology.

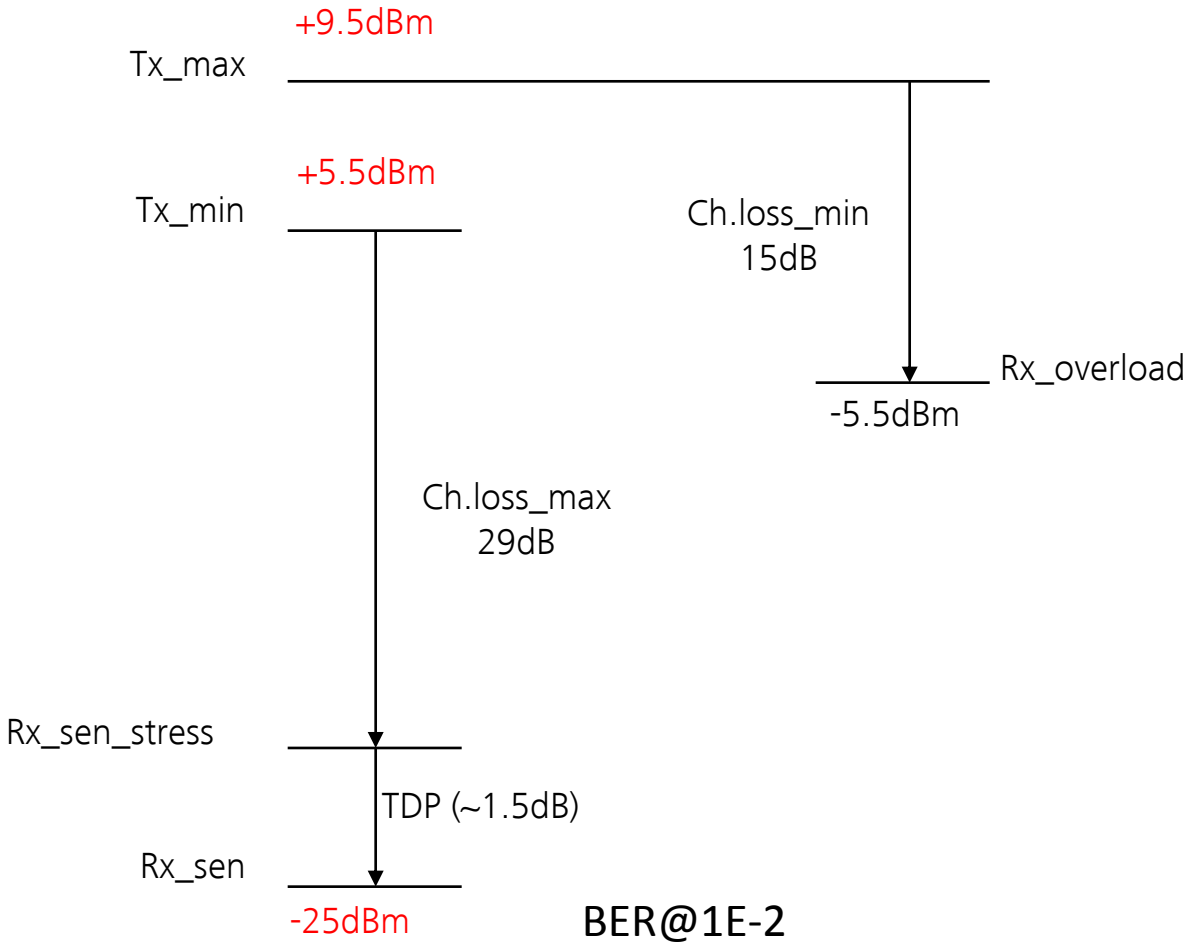
| | Lambda(nm) | Width(nm) |
|---|---|---|
| 100G UP | 1317.5 | +/-1.5 |
| 100G UP | 1311.5 | +/-1.5 |
| 100G UP | 1298.3 | +/-1.5 |
| 25G UP | 1286.5 | +/-1.5 |
| | | |
| 100G DN | 1471.00 | +/-2.5 |
| 100G DN | 1491.00 | +/-2.5 |
| 100G DN | 1511.00 | +/-2.5 |
| 25G DN | 1551.00 | +/-2.5 |

# Downstream power levels (straw man)



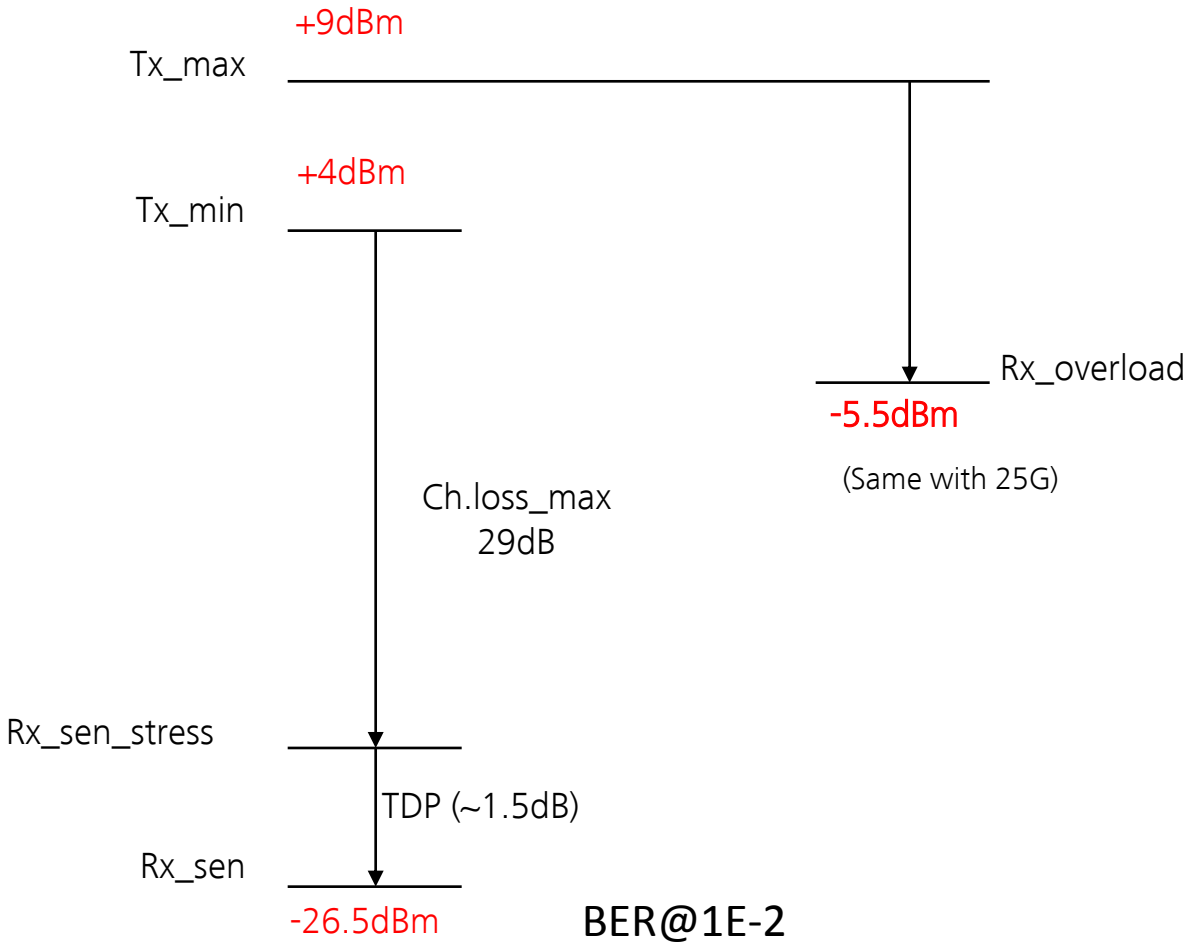

- The 25G Rx sensitivity is assumed with -26dBm@1E-2
- Assume 2.5dB demux loss for 100G ONU, and push 1dB pressure on future sensitivity improvement.
- 25G ONUs will have 1dB sensitivity margin for low cost consideration. (Another choice is 1dB launch power lower for 25G OLT)
- ER is assumed by 8dB

# 25G upstream power levels (straw man)




- The 25G Rx sensitivity is assumed with -26dBm@1E-2
- Assume 1dB burst mode sensitivity penalty compared with continuous mode.
- With some pressure , 25G OLT can be implemented without preamplifier.
- ER is assumed by 6dB

# 100G upstream power levels (straw man)




- Assume cooled DML transmits +6dBm launch power with moderate cost
- 2dB insertion loss for compact WDM design.
- 4dBm launch power is set for 100G ONUs in the reference point.
- Preamplifier are most probably need in OLT.
- ER is assumed by 6dB

# summary

- The feasibility and economy on 25G in C-band assisted with DSP have been analyzed.
- Plan D based on DSP technology can utilize existing 10G optics, wide channel width and sufficient DS/US gap, which will distinctly decrease the cost of optics.
- The DSP technology can fully migrate the transmission dispersion , the insufficient bandwidth of optics and improve the receiver sensitivity.
- The cost of DSP chips have also been analyzed and estimated, it will be cost effective enough when in volume.

# Thank you

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