201. Physical Coding Sublayer and Physical Media Attachment for 100G-EPON

201.1 Overview

This clause describes the Physical Coding Sublayer (PCS) with FEC and Physical Medium Attachment (PMA) used with {NG-EPON type} point-to-multipoint (P2MP) networks. These are passive optical multipoint networks (PONs) that connect multiple DTEs using a single shared fiber. The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 203.

201.1.1 Conventions

The notation used in the state diagrams in this clause follows the conventions in 21.5. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation ++ after a counter indicates it is to be incremented by 1. The notation −− after a counter indicates it is to be decremented by 1. The notation −= after a counter indicates that the counter value is to be decremented by the following value. The notation += after a counter indicates that the counter value is to be incremented by the following value. Code examples given in this clause adhere to the style of the "C" programming language.

201.1.2 Delay constraints

{TBD}

201.2 Physical Coding Sublayer (PCS) for 100G-EPON

201.2.1 Overview

This subclause defines the physical coding sublayers {NG-EPON type} supporting burst mode operation over the point-to-multipoint physical medium. The {NG-EPON type, symmetric} PCS is specified to support {NG-EPON types}, where both the receive and transmit paths operate at multiples of {TBD} Gb/s rate. The {NG-EPON type, asymmetric} PCS supports {NG-EPON types}, in which OLT transmit path and ONU receive path operate at {TBD} Gb/s, while the ONU transmit path and the OLT receive path operate at {TBD} Gb/s rate.

This subclause also specifies a forward error correction (FEC) mechanism to increase the optical link budget or the fiber distance. Figure 201–1 and Figure 201–2 show the relationship between the PCS sublayer and the ISO/IEC OSI reference model.

201.2.1.1 {NG-EPON, asymmetric} PCS

{TBD}

201.2.1.2 {NG-EPON, symmetric} PCS

{TBD}

201.2.2 PCS transmit function

This subclause defines the transmit direction of the physical coding sublayers for {NG-EPON type}. In the OLT, the PCS transmit function operates at a {TBD} Gb/s rate in a continuous mode. In the ONU, the PCS transmit function may operate at a {TBD} Gb/s rate, as specified herein ({NG-EPON type, symmetric}), or

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at a {TBD} Gb/s rate, as specified in {TBD} ({NG-EPON type, asymmetric}). For all {NG-EPON type}, the ONU PCS always operates in a burst mode in the transmit direction. When operating at the {TBD} Gb/s rate, the PCS includes a mandatory FEC encoder. Figure 201–6 illustrates the transmit direction of OLT PCS. Figure 201–7 illustrates the transmit direction of the ONU PCS.

201.2.2.1 Idle control character deletion

{TBD}

201.2.2.2 64B/66B Encode

See 49.2.4. The encoder shall perform the functions specified in the state diagram shown in Figure 49–16.

201.2.2.3 Scrambler

See 49.2.6.

201.2.2.4 FEC encoding

The {NG-EPON type} PCS shall encode the transmitted data stream using {TBD} FEC. Annex {TBD} gives an example of {TBD} FEC Encoding.

{details are TBD}

201.2.2.5 Data Detector

{TBD}

201.2.2.5.1 Burst Mode operation (ONU only)

In addition to inserting the parity data into the data stream, the Data Detector process in the {NG-EPON type U} PCS generates the PMA_SIGNAL.request(tx_enable) primitive to turn the laser on and off at the correct times.

Upon initialization, the laser is turned off. When the first 66-bit block containing data arrives at the buffer, the Data Detector sets the PMA_SIGNAL.request(tx_enable) primitive to the value ON, instructing the PMD sublayer to start the process of turning the laser on.

When the buffer becomes empty (i.e., contains only 66-bit blocks with Idle characters), the Data Detector sends the End of Burst Delimiter and after that sets the PMA_SIGNAL.request(tx_enable) primitive to the value OFF, instructing the PMD sublayer to start the process of turning the laser off. Between packets, Idle blocks arrive at the buffer. If the number of these Idle blocks is insufficient to fill the buffer then the laser is not turned off.

The length of the FIFO_DD buffer at the ONU shall be chosen such that the delay introduced by the buffer together with any delay introduced by the PMA sublayer is long enough to turn the laser on and to allow a laser synchronization pattern, Burst Delimiter pattern, and a predefined number of Idle blocks to be transmitted. The laser synchronization pattern allows the receiving optical detector to adjust its gain ($T_{receiver\_settling}$) and synchronize its receive clock (T_{CDR}). The Burst Delimiter allows the receiver to easily identify the beginning of FEC protected portion of the ONU transmission. The Idle control characters are used to synchronize the descrambler and establish start-of-packet delineation.

Figure {TBD} illustrates the details of the ONU burst transmission. In particular, this figure shows the details of the synchronization time and the FEC protected portions of the burst transmission.

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{Details are TBD}

201.2.2.6 Gearbox

See 49.2.7.

201.2.3 PCS receive Function

This subclause defines the receive direction of physical coding sublayers for {NG-EPON type}. In the ONU, the PCS operates at a {TBD} Gb/s rate in a continuous mode. In the OLT, the PCS may operate at a {TBD} Gb/s rate, as specified herein ({NG-EPON type, symmetric}), or at a {TBD} Gb/s rate, compliant with Clause {TBD} ({NG-EPON type, asymmetric}). For all {NG-EPON types}, the OLT PCS always operates in burst mode. When operating at the {TBD} Gb/s rate or at {TBD} Gb/s rate, the PCS includes a mandatory FEC decoder. The receive direction of ONU PCS is illustrated in Figure 201–6 and receive direction for the OLT PCS is illustrated in Figure 201–7.

201.2.3.1 OLT synchronizer

The OLT codeword synchronization function receives data via the 16-bit PMA_UNITDATA.indication primitive.

The OLT synchronizer forms a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 201–17). It obtains lock to the thirty-one 66-bit blocks in the bit stream by looking for the burst delimiter. Lock is obtained as specified in the codeword lock state diagram shown in Figure 201–17. While in codeword lock, the synchronizer copies the FEC-protected bits from each data block and the parity bits of the codeword into an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword. When in codeword lock, the state diagram looks for the end of the burst. When this is observed, then the state diagram deasserts codeword lock. The state diagram then goes back to searching for the burst delimiter.

{details are TBD}

201.2.3.2 ONU Synchronizer

The codeword synchronization function receives data via the 16-bit PMA_UNITDATA.indication primitive.

The synchronizer forms a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 201–18). It obtains lock to the thirty-one 66-bit blocks in the bit stream using the sync headers and outputs 2040-bit codewords to the FEC decoder function.

The incoming sync header pattern is 27 conventional (Clause 49) sync headers (binary 01 or 10), and then binary 00, 11, 11, and finally binary 00. The ONU synchronizer attempts to match this pattern to the received data stream, and when it finds a perfect match of two full codewords (62 blocks), it then asserts codeword lock.

While in codeword lock, the synchronizer copies the FEC-protected bits from each data block and the parity bits of the codeword into an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword.

When in codeword lock, the state diagram continues to check for sync header validity. If 16 or more sync headers in a codeword pair (62 blocks) are invalid, then the state diagram deasserts codeword lock. In addition, if the persist_dec_fail signal becomes set, then codeword lock is deasserted (this check ensures that certain false-lock cases are not persistent.)

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{details are TBD}

201.2.3.3 FEC decoding process

The {NG-EPON type} PCS shall correct errors in the received data stream using TBD FEC.

{details are TBD}

The synchronizer state diagram accumulates a full codeword in a buffer. If the synchronizer is locked, then the FEC decoding process is triggered. The FEC algorithm then processes the buffer. The algorithm produces two outputs: the decode_success signal and (if successful) the corrected buffer. The data portion of the buffer is then read out to the descrambler logic in 66-bit blocks, as normal. Note that the rate of 66 bit transfers here is reduced due to the removal of the FEC parity blocks. This is corrected in the Idle Insertion step (see Figure 201–22).

If decode_success is false, then a counter is incremented (see 45.2.3.40). If there are three decoding failures in a row, then the Persist_dec_fail signal is asserted. This signal then resets the synchronizer.

The FEC decoding process shall provide a user option to indicate an uncorrectable FEC codeword (due to an excess of symbols containing errors) to higher layers. If this option is set to be true, the FEC decoding process checks for the value of decode_success. If the variable decode_success is set to false, then each sync header of the received payload blocks in the FEC codeword is set to a value of binary 00. However, the data blocks are nevertheless passed to the descrambler to maintain descrambling synchronization. When this option is set to FALSE and decode_success is FALSE then each received payload block is passed unchanged.

{details are TBD}

201.2.3.4 BER monitor

The BER monitor is described in Figure 201–21. This BER monitor function operates on the uncorrected incoming data stream.

{details are TBD}

201.2.3.5 Descrambler

See 49.2.10.

201.2.3.6 64B/66B Decode

See 49.2.11. The decoder shall perform functions specified in the state diagram shown in Figure 49–17.

201.2.3.7 Idle Insertion

The receiving PCS inserts the Idle control characters to compensate for the removed FEC parity octets. The Idle Insertion function (see Figure 201–22) receives 72-bit vectors from the 64B/66B decoder and writes them into the Idle Insertion FIFO (called FIFO_II) and reads 72-bit vectors from the FIFO_II and transfers them to the XGMII.

The Idle Insertion process receives 72-bit vectors at a slower rate than the nominal 25GMII rate due to the fact that the FEC parity blocks are removed by the FEC decoder and not put through the descrambler and 64B/66B decoder. The Idle Insertion process outputs 72-bit vectors at the nominal 25GMII rate. To match the input and output rates, the Idle Insertion process inserts additional 72-bit vectors containing Idle codes.

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The additional blocks are inserted between packets and not necessarily at the same locations where parity blocks have been removed.

The body of this subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the {NG-EPON type} PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5.

{details are TBD}

201.3 {NG-EPON type} PMA

{details are TBD}

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201.4 Protocol implementation conformance statement (PICS) proforma for Clause 201, Physical Coding Sublayer and Physical Media Attachment for 100G-EPON[33]

201.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 201, Physical Coding Sublayer and Physical Media Attachment for 100G-EPON, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

201.4.2 Identification

201.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[33] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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201.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 201, Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point-to-point media, types 25GBASE-PR and 25/10GBASE-PR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	
Date of Statement	

201.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support

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