25-32G Burst-Mode CDR/SerDes 802.3ca Contribution

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Motivation

FMAX has developed:

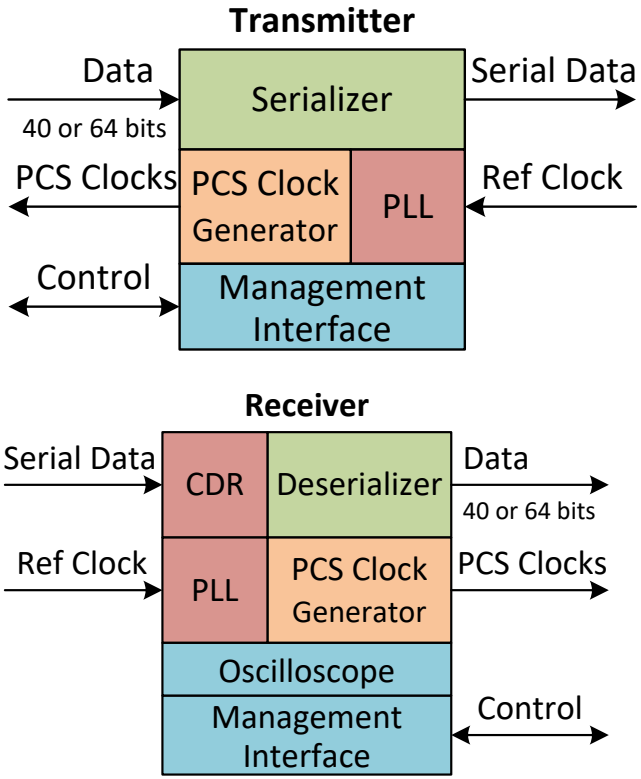
25-32G NRZ Analog Burst-Mode CDR-SerDes IC

This presentation provides information/opinion on:

- 25Gbps NRZ Burst-Mode CDR capability, specs & power
- Scaling to 50/100 Gbps, with <28nm CMOS

Burst CDR-Serdes Description

- Architecture: analog CDR, with digital burst phase-acquisition
- 25.78 to 32 Gbps data rates supported
- Low noise/jitter on-chip LC oscillator; reference-less
- Programmable loop BW and PLL parameters
- Burst mode or continuous mode operation
- 802.3bs EEE deep sleep and fast wake support
- User definable burst lock preamble and sequence
- Programmable Rx CTLE equalization
- Tx 4 tap VML output, 2 post cursor and 1 pre-cursor
- 40 or 64 bit parallel interface
- PCS clock generation available
- On-chip oscilloscope, eye quality monitor
- 250um pitch, fully integrated
- TIA input and laser/modulator output driver options
- Flexibility to support diverse optical transceiver specs
- TSMC 28nm CMOS process
- Deterministic lock-acquisition, no metastability risk



CDR Serdes Specifications

Specification	Value	Units
Data rate	25.78, 32	Gbps
Burst lock time	<3ns	ns
Output jitter	<1	ps rms
Jitter tolerance	0.75	UI
Rx equalization	12 max	dB
Tx equalization	12 max	dB
Rx power	65	mW
Tx power	40	mW
Cell pitch	250	µm

Scaling

- 50Gbaud symbol rate IC appears achievable
  - Work on equalization/dispersion-comp required
- 8x oversampling timing resolution achievable
  - 5ps at 25Gbaud, 2.5ps at 50Gbaud
- Can be implemented with PAM4 phase detector
- Architecture scales favorably to <28nm CMOS

Conclusion

- 25G CDR/SerDes IC with burst phase acquisition provides low power, modest-cost PON solution using mature fabrication technology
- No fundamental barrier to 25G-100G PON burst CDR with NRZ or PAM4 encoding
- No fundamental barrier to <28nm CMOS process
- Need-for and degree-of DSP-based equalization requires further study
- Specifications scale with data rate