More on Folded BCH FEC

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Agenda

- Review from January 2017 meeting
- Simulation results of code candidates
- Folded BCH code construction
- Comparison of Folded BCH with product codes construction
- High level description of decoding algorithms

Review from January 2017 TF meeting

- At the January meeting, we presented FEC selection considerations (laubach_3ca_01_0117.pdf), introduced “Folded BCH”, and held some straw polls
- Dropped one straw poll as informal group opinion appeared to be that the FEC electrical performance should be pushed to better than +1 dB over 10G-EPON
- SP#2: same codeword ds & us: poll results 14/4/9
- SP#3: codeword size between 2KB and 4KB: poll results 2/5/21
  - Majority held by abstains – indicates more study needed
- SP#4: desired total overhead limited to support minimum bidirectional 20Gb/s “unobstructed” (at 25.78125 GBd signaling rate) : poll results 12/1/15
  - Majority held by abstains – indicates more study needed
- Interpreted reaction to the Folded BCH overview as: would like to see more details

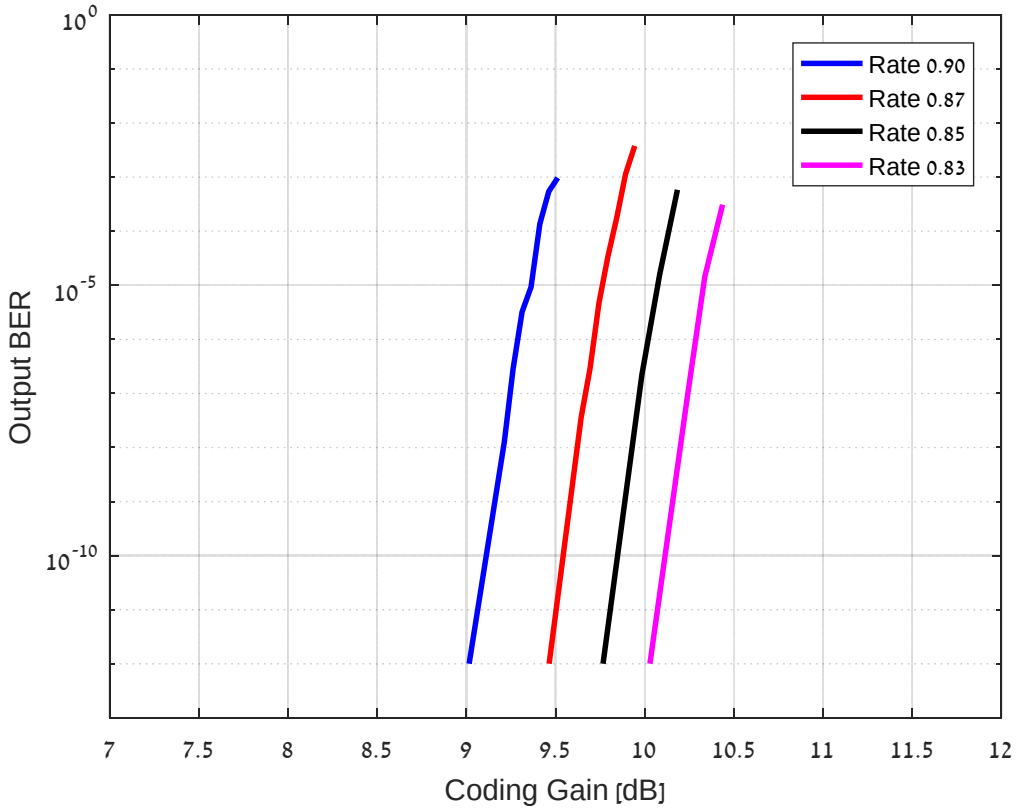
Review from January 2017 TF meeting

- Developed and used as ECC for FLASH memory
  - Provides higher NECG for a given code rate
  - Market is driving BER to be better than 10^{-15} for NAND Flash memory performance
  - Lower power than LDPC
  - Speeds in excess of 3+GB/s (24+Gb/s)
  - No BER floor
  - Based on BCH t<=3 codes

Folded BCH HARD Decoding Capabilities
4KB Codeword Size, Various Rates

- Supported input RBER for output BER $< 10^{-12}$

Code Rate	Length (Bits)	RBER	Coding Gain [dB] @1E-12
0.83	36864	1.2E-2	9.9
0.85	36864	1E-2	9.7
0.87	36864	8E-3	9.4
0.9	36864	5.6E-3	9



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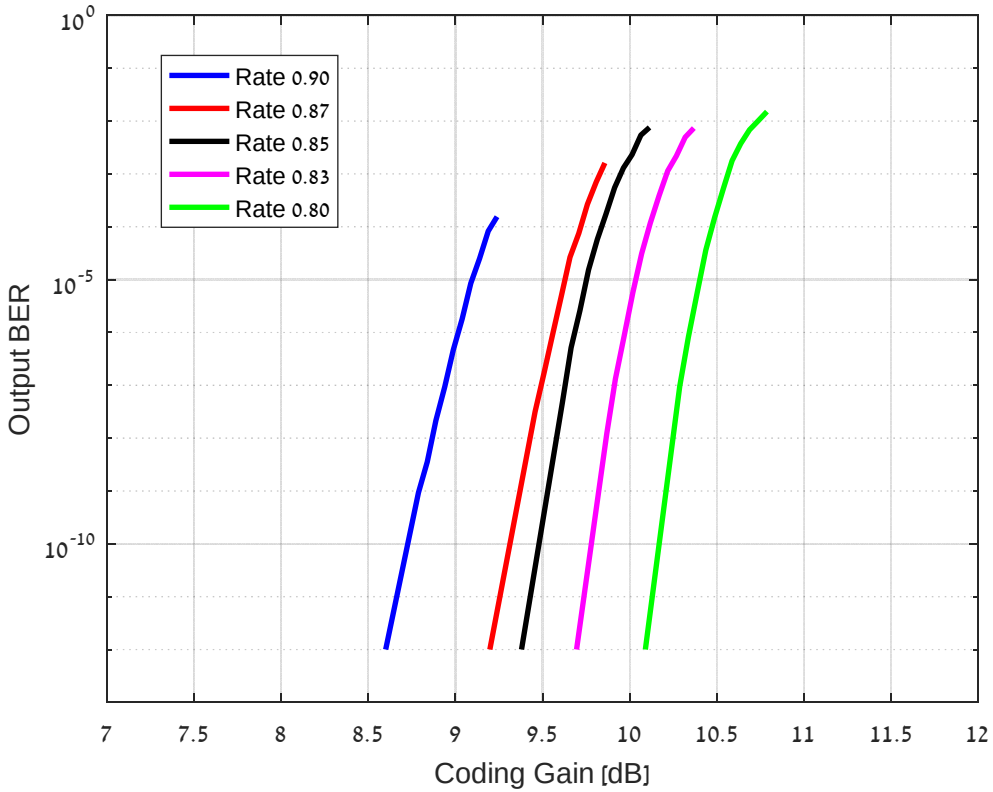
Folded BCH HARD Decoding Capabilities
2KB Codeword Size, Various Rates

- Supported input RBER for output BER $< 10^{-12}$

Code Rate	Length (Bits)	RBER	Coding Gain [dB] @1E-12
0.8	16384	1.25E-2	10.1
0.83	16384	9.5E-3	9.7
0.85	16384	7.5E-3	9.4
0.87	16384	6.5E-3	9.2
0.9	16384	3.9E-3	8.6



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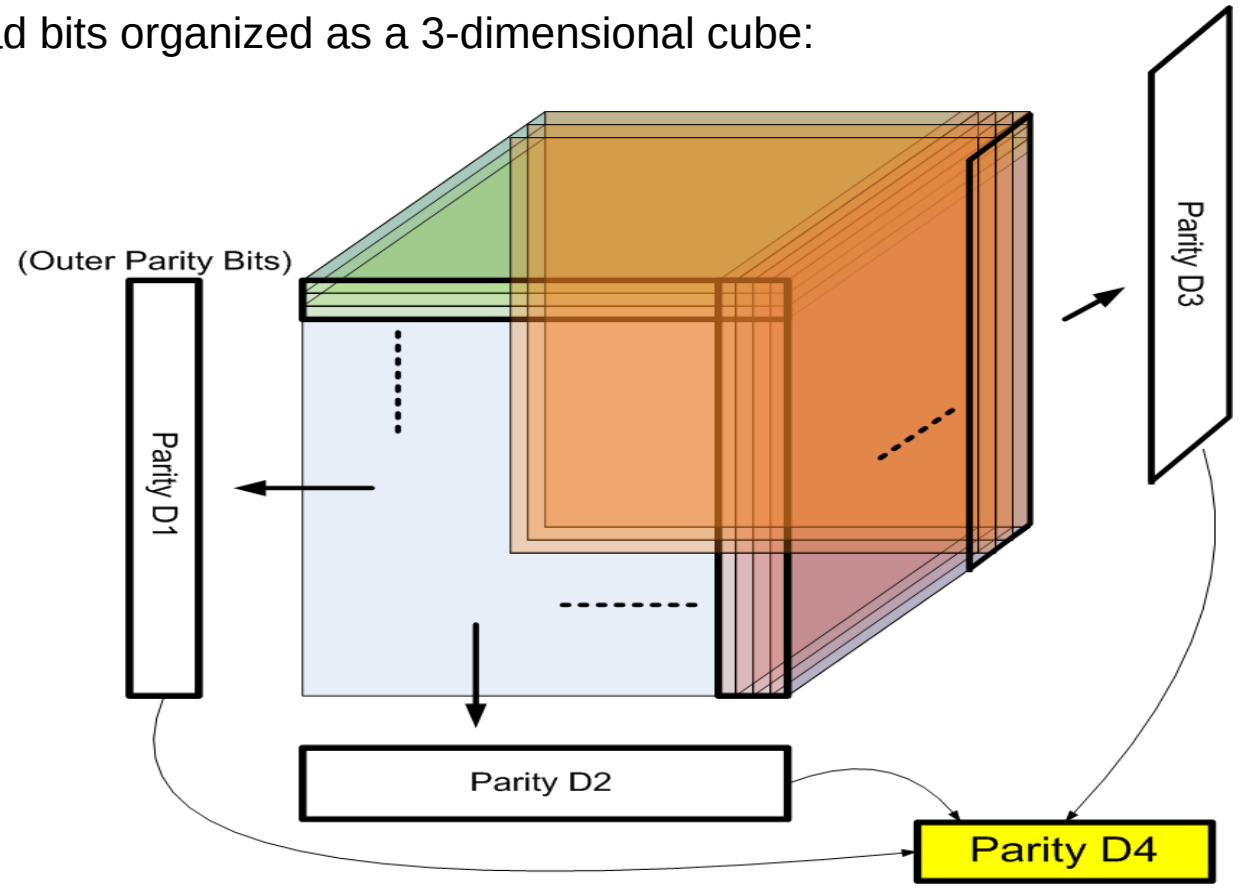
Folded BCH Overview

Encoding Overview

- The systematic encoding includes parallel encoding of the payload bits in multiple dimensions. The payload bits are organized as a cube, where every BCH component encodes together.
- For a given dimension, same BCH component codes are used to encode different set of planes. On different dimensions, the BCH components can be different, by having for example a different length, or decoding capability.
- Main motivation for a multi-dimensional folded code structure is to be able to use relatively strong BCH codes, e.g. which correct $t = 3$ errors, for short codewords and high code rates.

Folded BCH
3D Encoding with Folded-BCH Components

Payload bits organized as a 3-dimensional cube:



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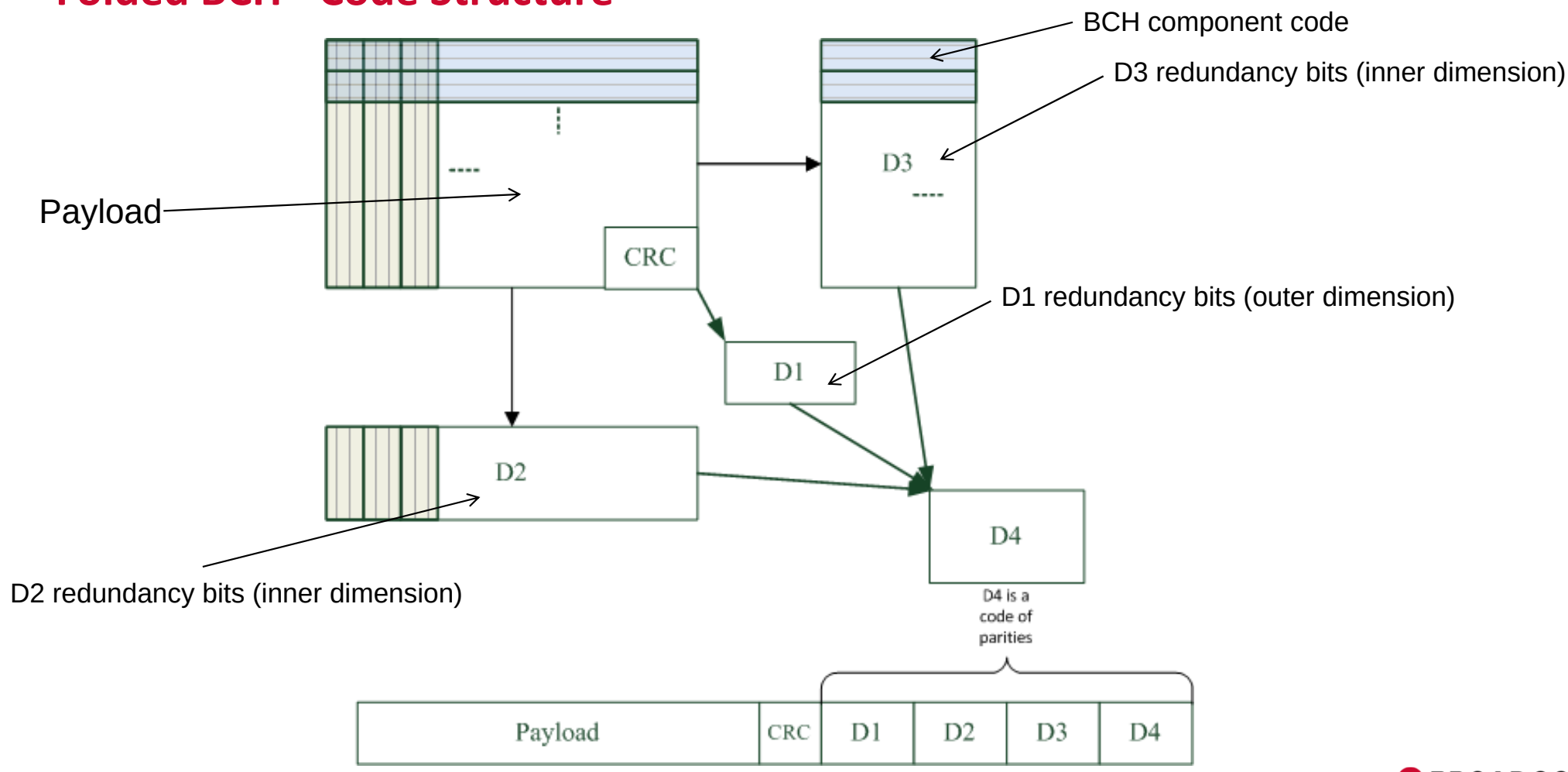
Folded BCH - Code Structure



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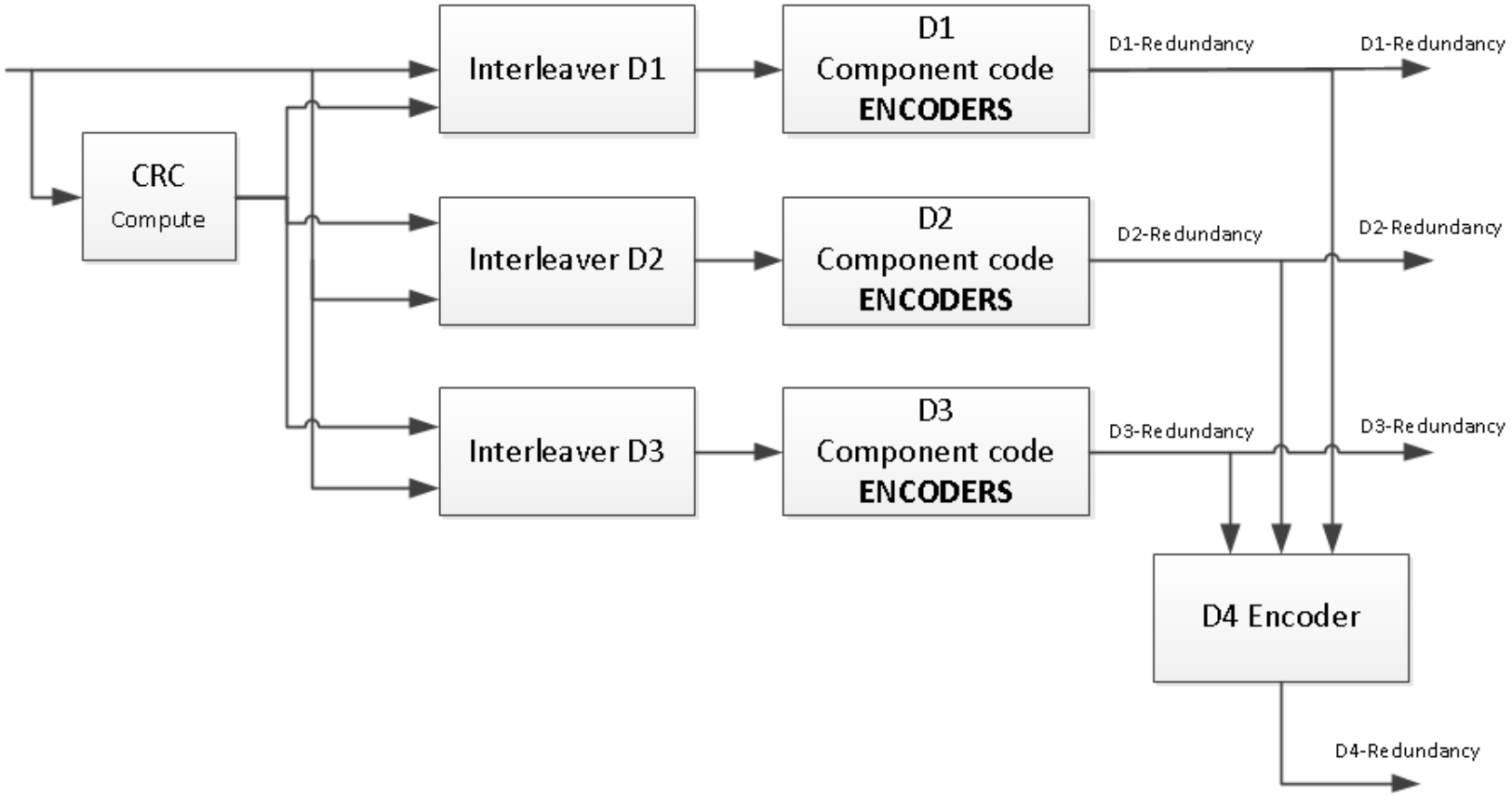
3D Encoding Block Diagram



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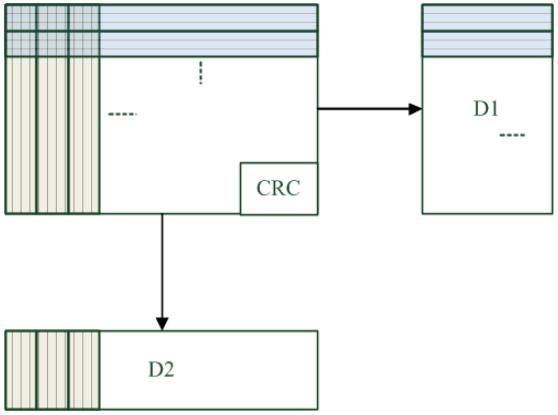
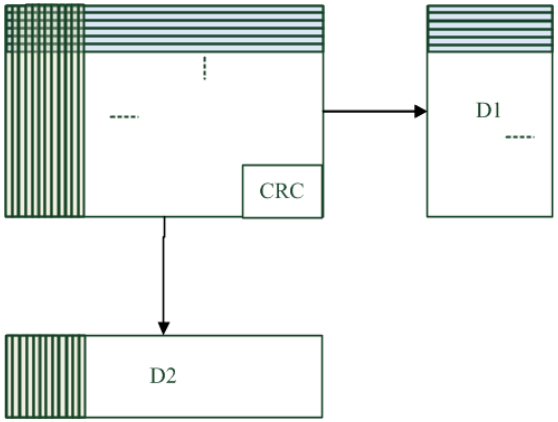
Folded BCH vs. Product Codes

- In Folded BCH every several rows/columns are jointly encoded with a component code
- A standard product code takes a single row/column to encode with a component code
- For obtaining the same code rate this means:
  - **Folded product codes can use fewer component codes, where each code can correct more errors**

Folded BCH Product



Standard product code



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Folded BCH Decoding Schemes

Folded BCH Decoder

- Hard decoder
  - High reliability decoding of up to (*t-1*) errors
  - Fast inner iterative decoding
  - Outer-inner iterations
  - Intersections assisted decoding

Decoding Overview

- Fast decoding is obtained with BCH components of $t \leq 3$ for which the error locating polynomial (ELP) can be directly solved without a Chien-search[1]
- "Intersections decoding" considers unsolved component codes of different dimensions, enumerate over the common bits (intersection bits) for these components, and accept solutions if accepted by both dimensions.
- Hard decision decoding

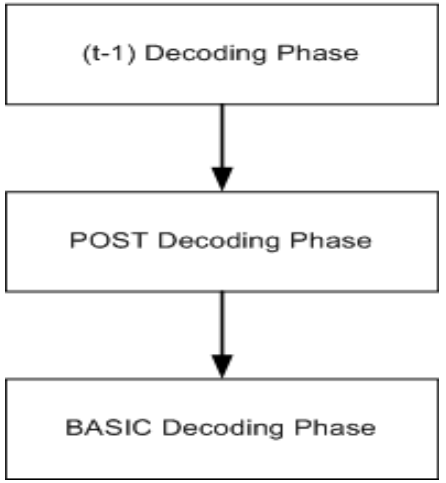
[1] J. van der Horst and T. Berger, "Complete decoding of triple-error correcting binary bch codes," IEEE Transactions on Information Theory, vol. 22, no. 2, pp. 138–147, March 1976.

(*t-1*) Limited Correction Iterations

Goal: Reduce probability of false corrections

- Define *t* to be the highest number of errors that can be corrected by a single BCH component, where *t=(D-1)/2*
- Allow BCH decoder corrections only when
  - Probability of missCorrection close to 0
  - Number of reported errors is **smaller** than *t*
- Such corrected components are marked as **forced**.
- There may be several consecutive iterations with limited corrections.
- **Early termination**: If there is no further decoding progress phase is terminated earlier and next phase is activated

SAFE Decoding Flow:



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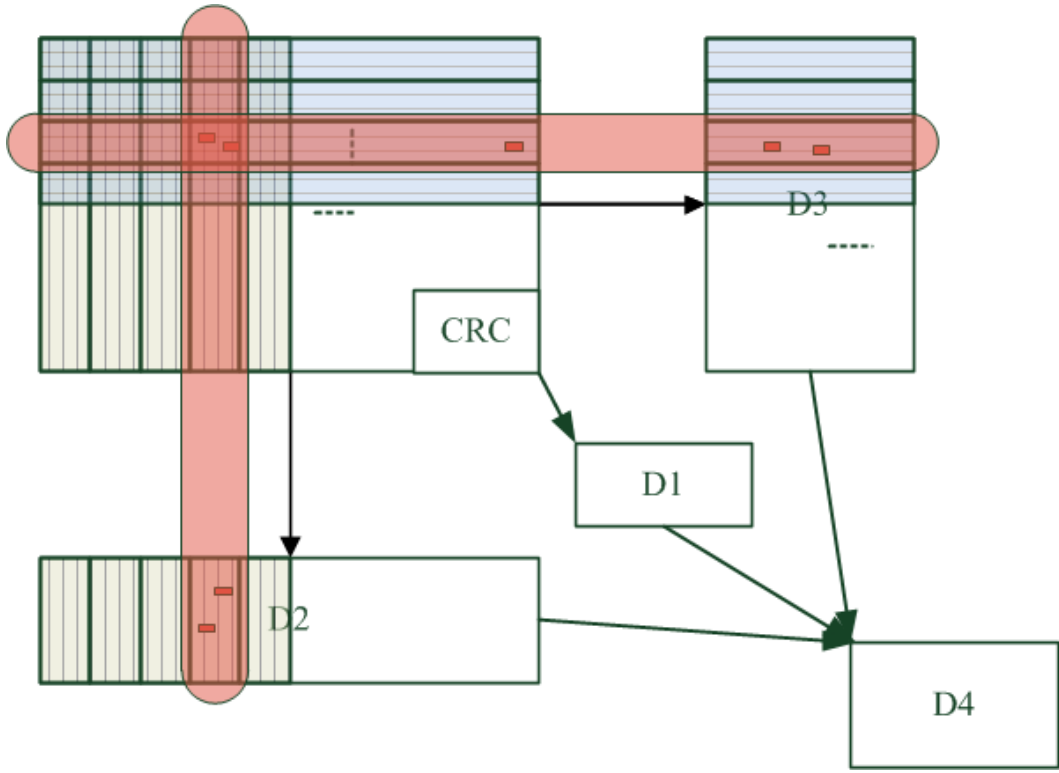
Intersections Decoding

- When some code-components, on different dimensions, have >t errors
- Enumerate hypotheses of bits which are common to unsolved packets of different dimensions
- Conditionally accept solutions
- Example on the right: each component can decode up to t=3 errors. Intersections decoding with 2-bit enumeration successfully decodes both components.



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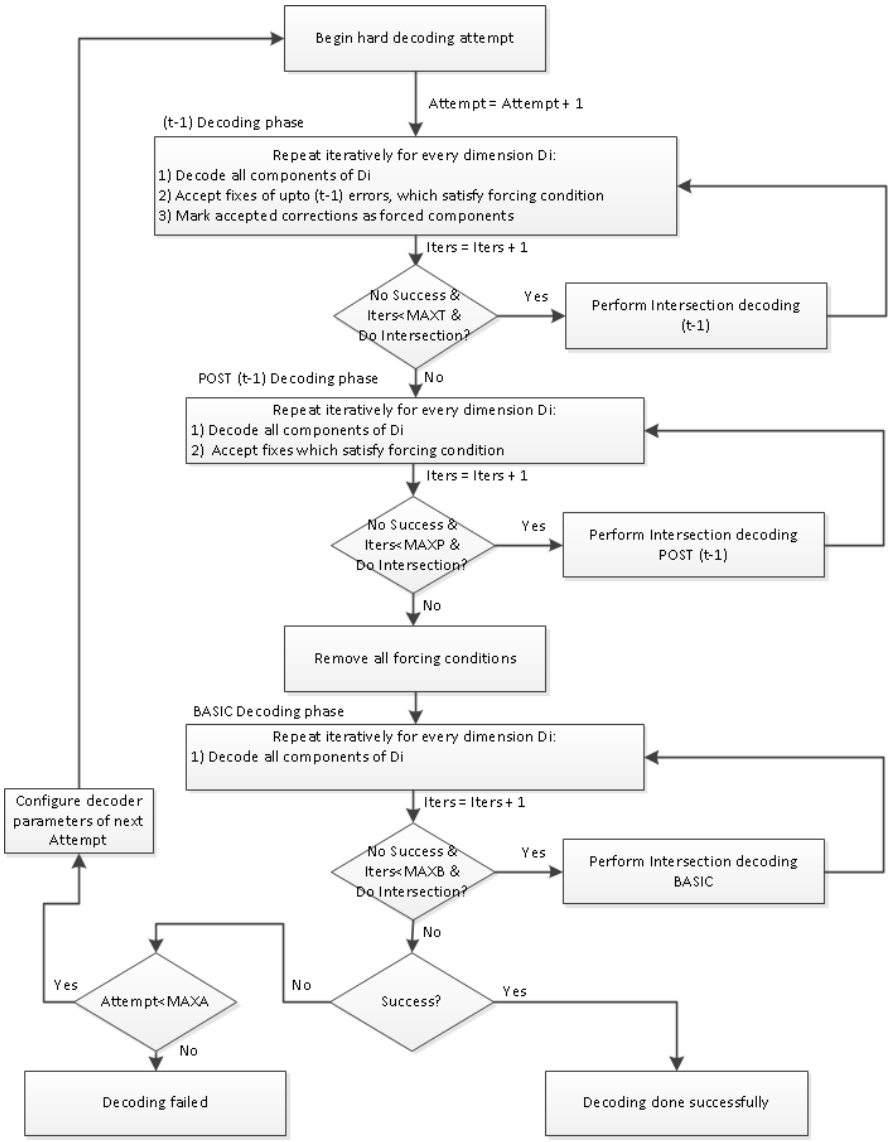
Hard Decoding Flow



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Other

- Hard-decoding meets throughput of 25.78125 Gb/s.

Next Steps

- Examine other code candidates of Folded BCH that meet the 20 Gb/s un-obstructed study results
  - Adjust for rBER of 10^{-2} corrected to 10^{-12}
  - Provide details on simulation set up
- Compare to performance of LDPC and RS with similar block sizes and code rates

Thank You!

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