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High gain FEC and CDR Locking For 25G NRZ

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May, 2017

High gain FEC is proposed for improved power budget

(effenberger_3ca_1_1116, houtsma_3ca_1_0916, laubach_3ca_01_0117)

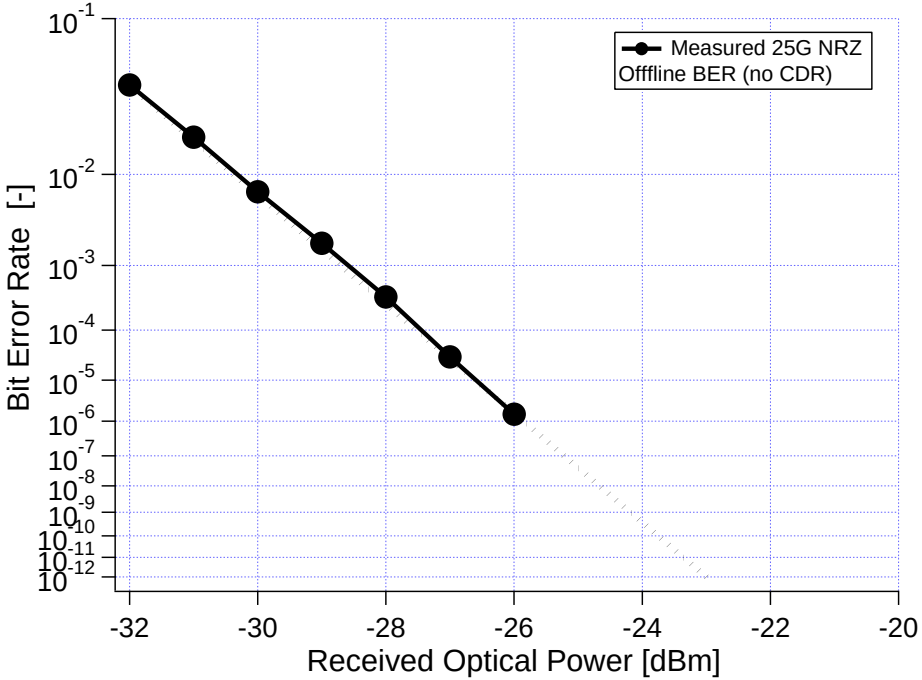
Input BERs before FEC of 10^{-2} are considered

Question can CDR lock to signal and recover data at BER= 10^{-2} ?

How do we know we have recovered data with BER= 10^{-2} to investigate CDR locking ? (since CDR needs to lock to recover the data)

To do this we used offline data for different received powers and calculated the FEC input BER offline without need for CDR to lock

Measured 25G BER curve (with offline data recovery) :



We used this data to investigate clock recovery for different received optical power (and hence different BERs)

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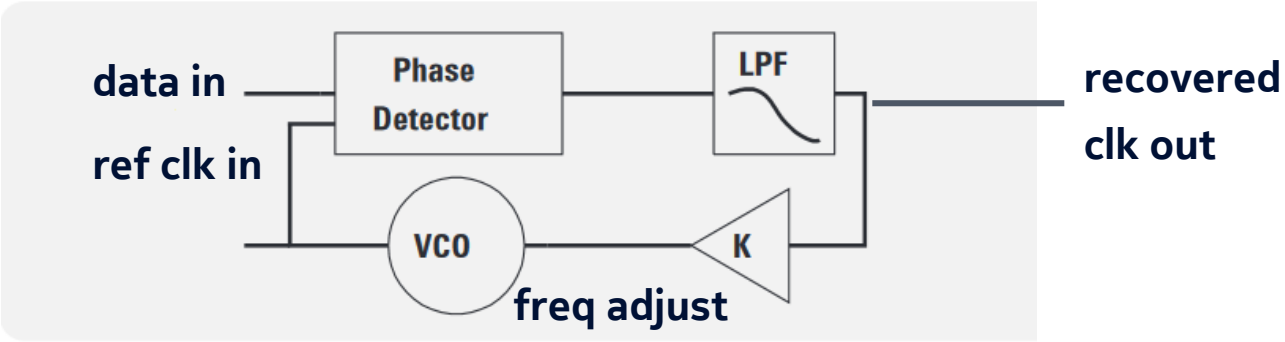
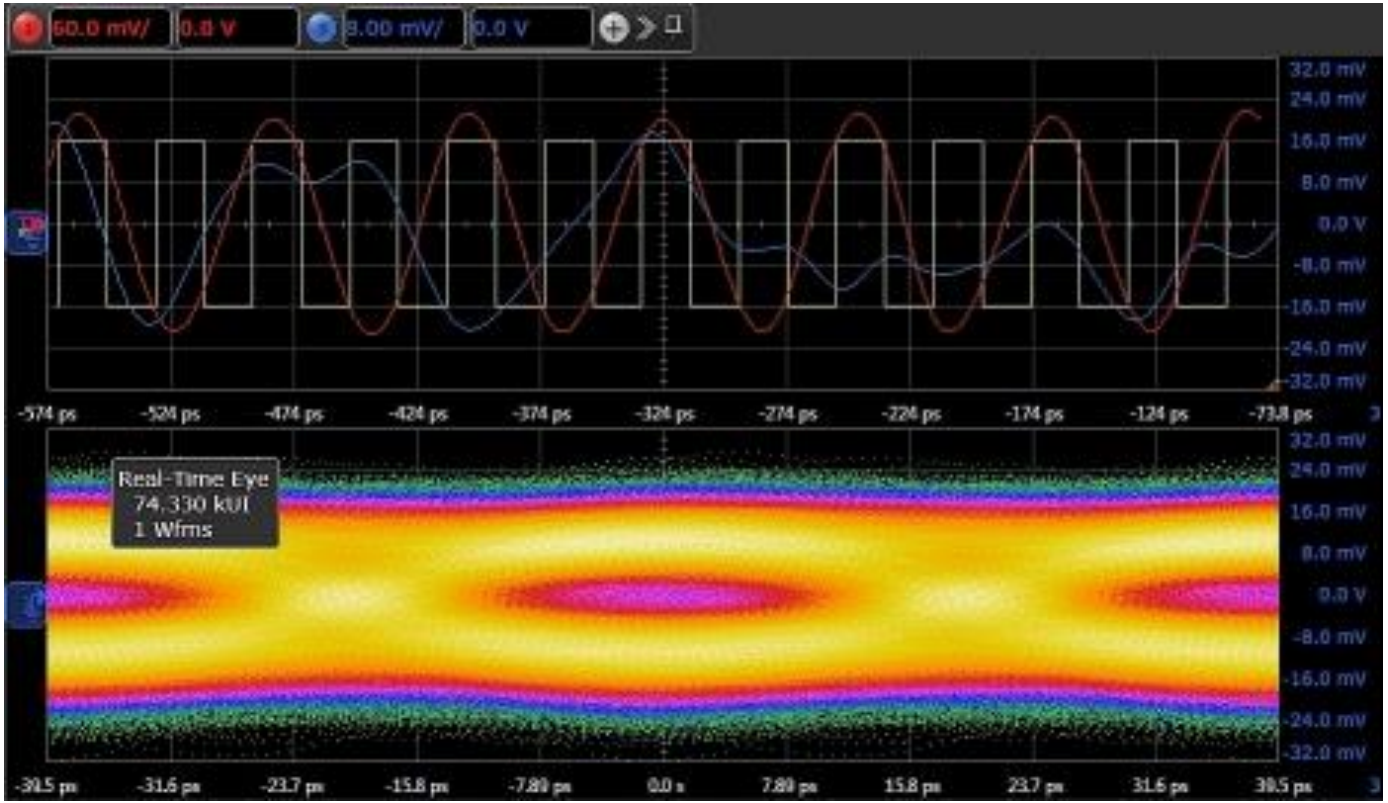
How does CDR lock ?

The receiver generates a clock from an approximate frequency reference, and then phase-aligns the clock to the transitions in the data stream with a phase-locked loop (PLL).



A simple PLL schematic.

Real time measurement using CDR of storage scope at BER~10^{-4}



CDR loop bandwidth =15.2 MHz and damping factor=0.707 (2nd order PLL)

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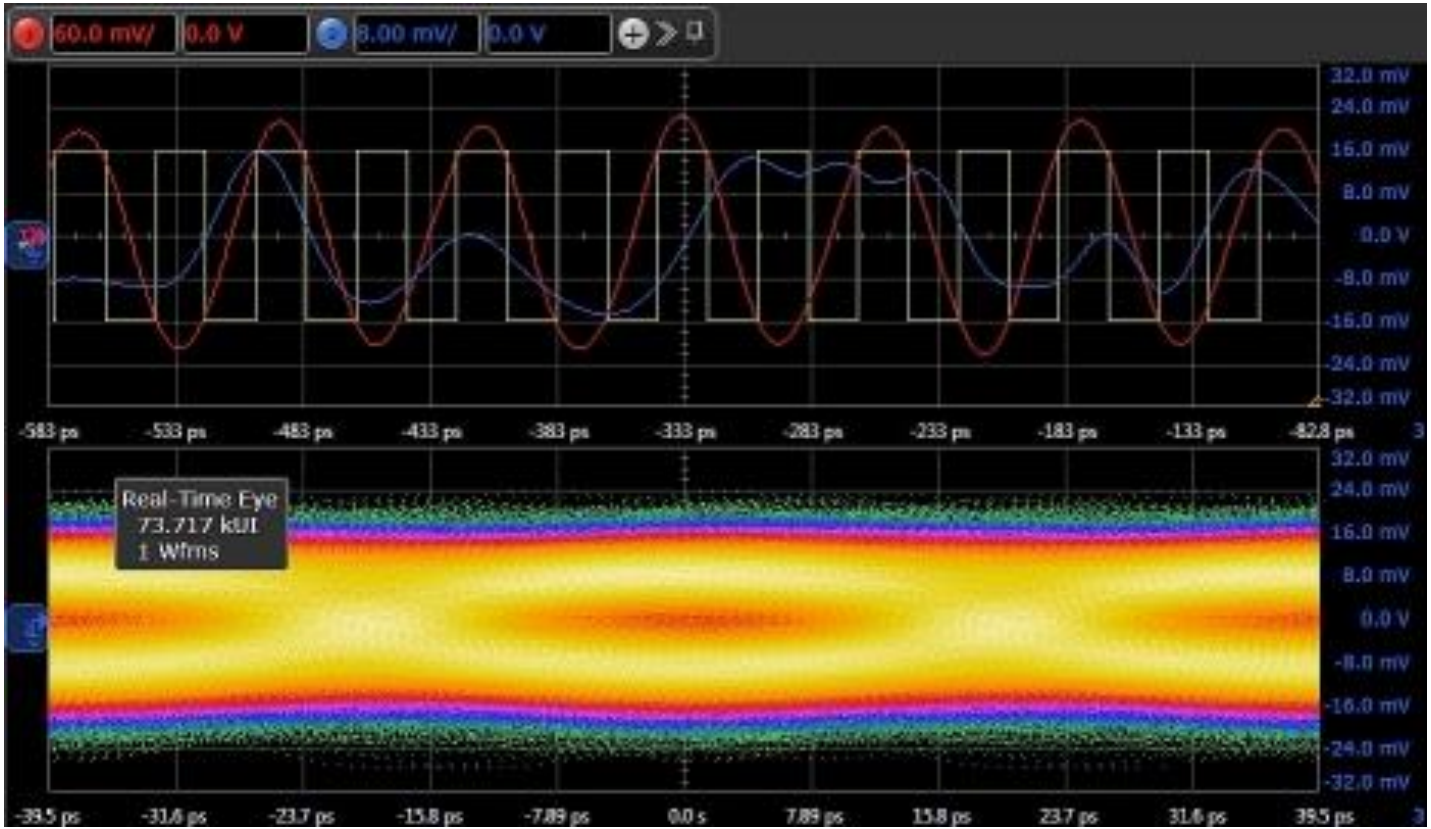
At BER~10^{-3}



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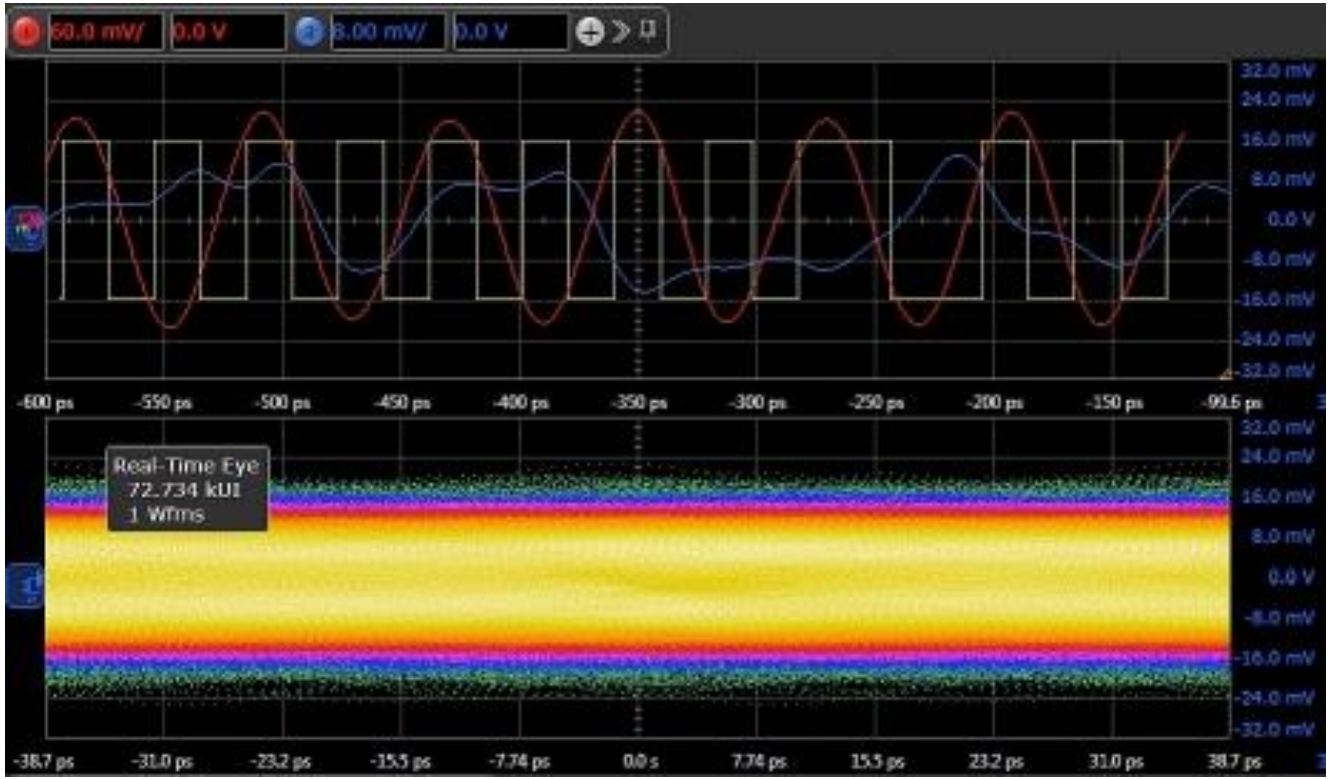
At BER~10^{-2}



Recovered clock starts to deviate from 25G transmitter clock (loss of lock?)

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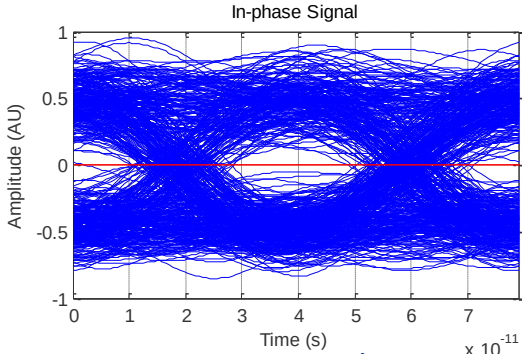
Investigate clock recovery for different optical powers with offline data :

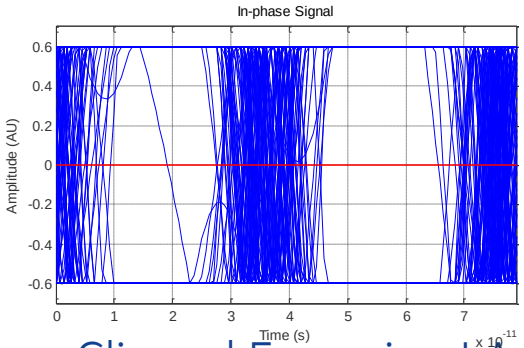
We assume our data is SNR limited at high BER

This means we can’t use any equalization (like FFEs) to improve signal quality before the clock and data is recovered

To ensure CDR sees transitions for locking we implemented an ‘ideal’ limiting amplifier to clip the signals, so CDR is not SNR limited



Measured Eye



Clipped Eye using LA

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CDR locking will depend on how much the recovered clock will deviate from ‘ideal’ 25G clock as function of time

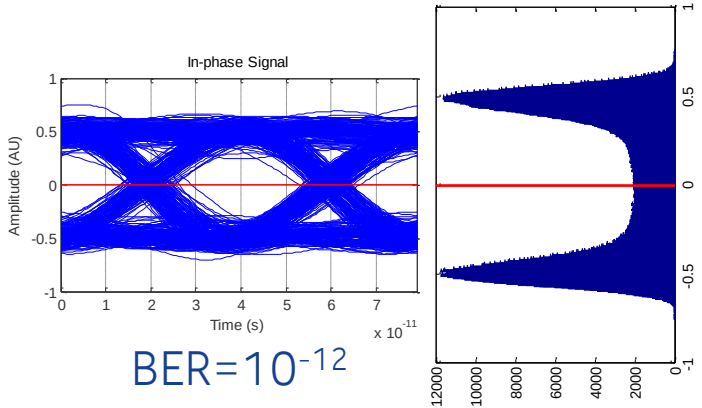
For SNR limited signals the voltage noise will translate into increase of recovered clock jitter which will make it more difficult to recover the ‘ideal’ 25G clock.

Recovered clock jitter is the deviation of the recovered clock from its ideal location in time. Or simply how early or late a transition is with reference to when it should transition.

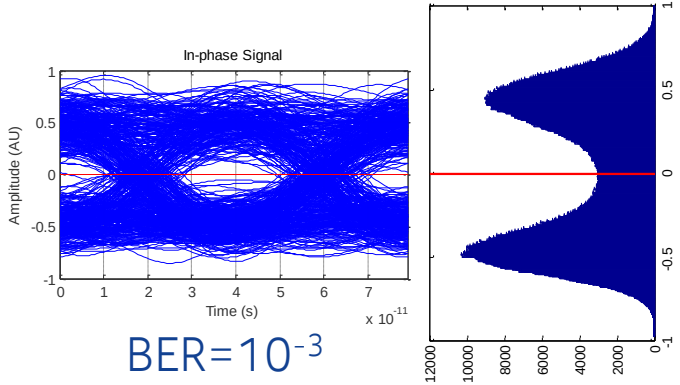
We investigated offline recovered clock with ‘ideal’ 25G clock to investigate if CDR will be able to lock at high BER

Voltage Noise and Recovered clock jitter :

Bit errors at high BERs are caused by voltage noise. If momentary noise voltage exceeds the noise margin, a wrong value can be sampled even if the sampling takes place at the correct moment in time.



BER=10^{-12}



BER=10^{-3}

For high BERs voltage noise will cause increase in jitter due to the fact that bit probability distributions start to overlap

This simply relates to the bit error probability and thus BER

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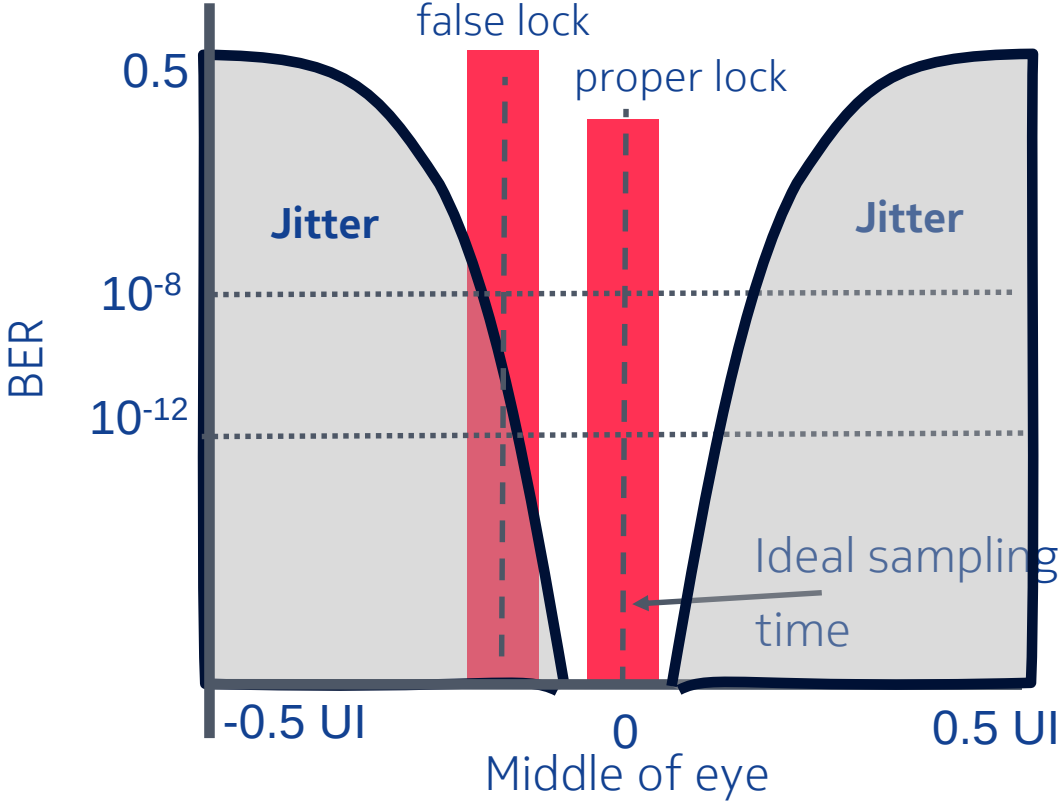
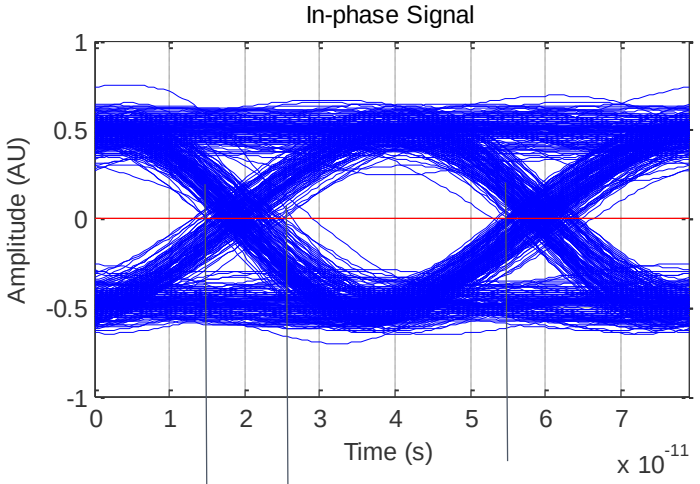
This is different from bathtub curve jitter measurement





Decision window

Jitter

=CDR retiming zone

Plots BER with jitter for good quality eye by changing sampling point

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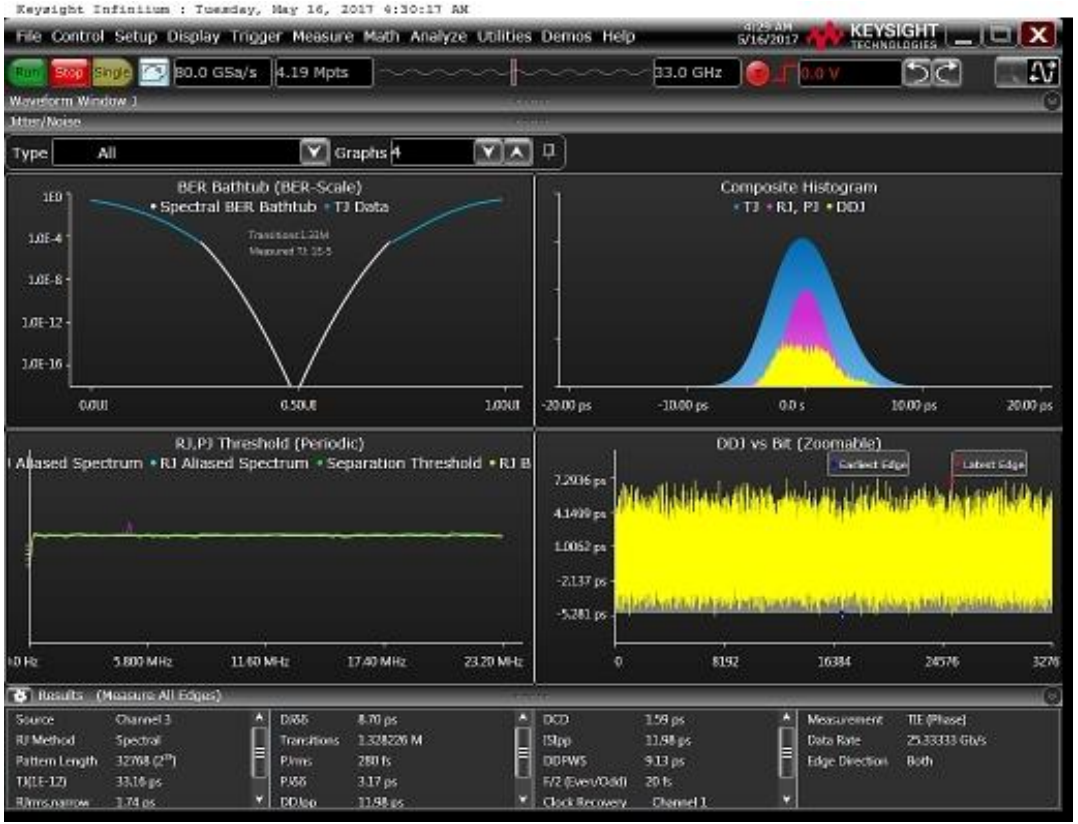
Bathtub measurement at 25G NRZ with 25G APD



For 25G :

1 UI= 40 ps

Tj (10^{-12}) = 33.16 ps

sampling margin < 7 ps

(for 10G: 67 ps, same Tj)

Tj (10^{-3}) = 14.6 ps

sampling margin ~25 ps (0.63 UI)

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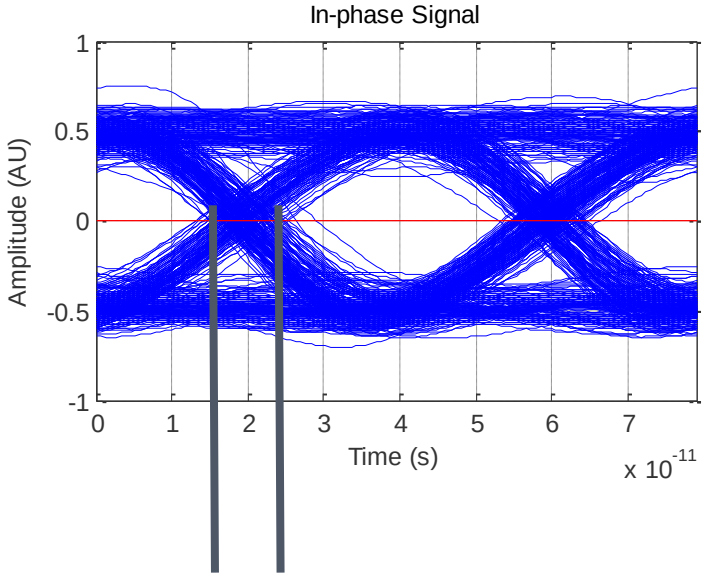
Jitter for BER=10^{-12}

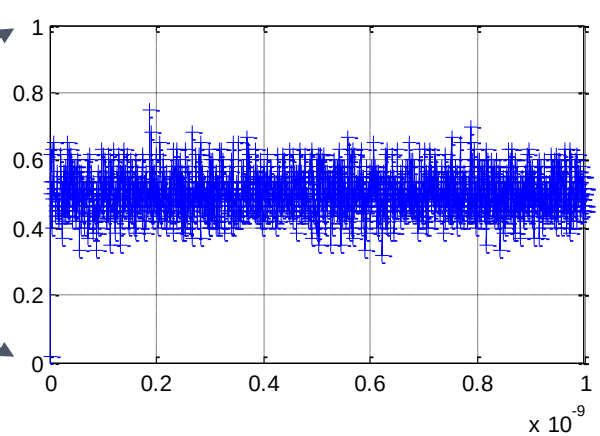
Eye diagram



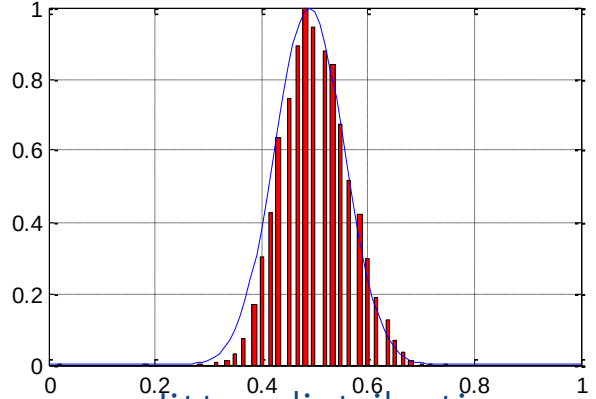
Jitter

Middle of eye

Tbit



Jitter (time domain)



Jitter distribution

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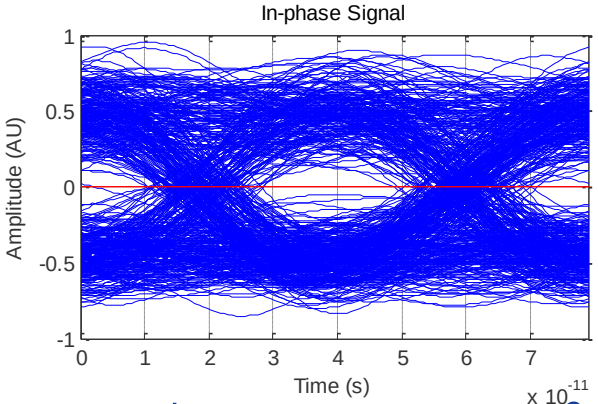
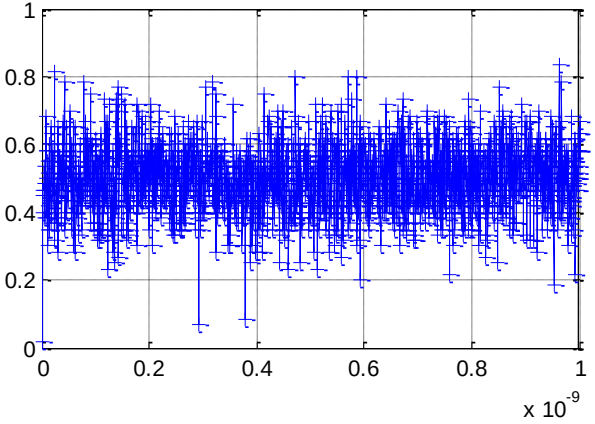
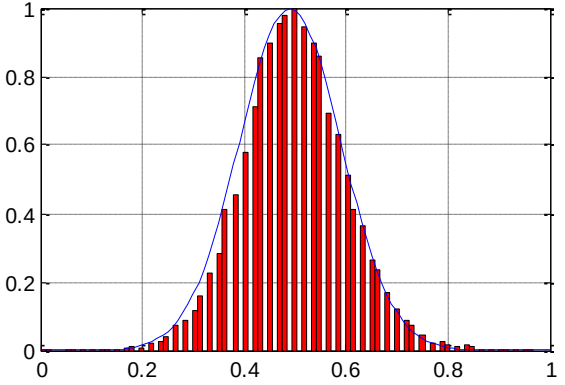
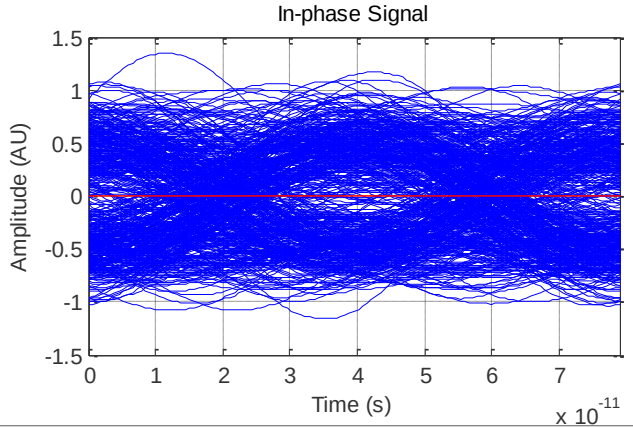
Condition : BER=10^{-3}

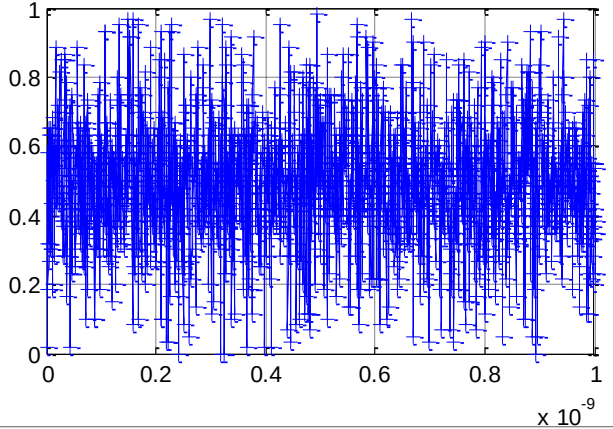


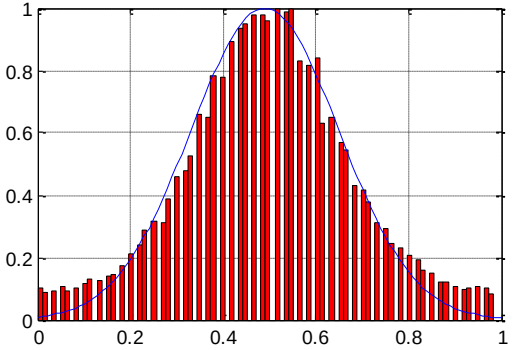




Condition : BER=10^{-2}







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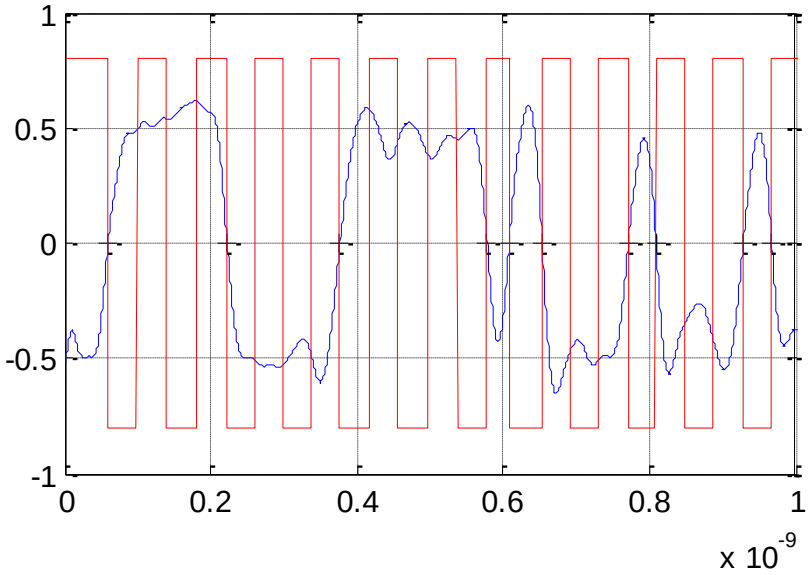
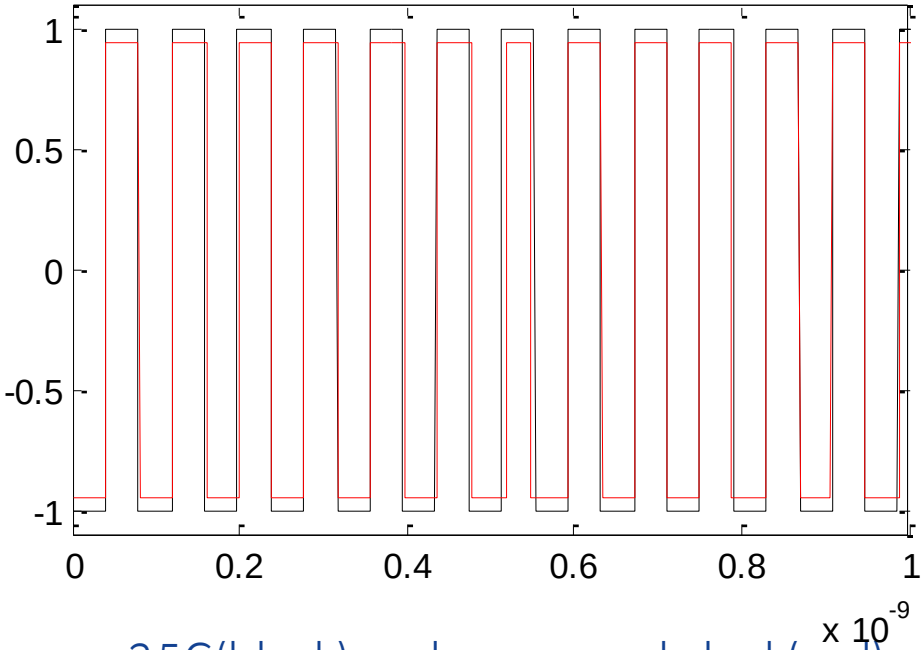
Clock recovery at BER=10^{-12}



Data and recovered clock



25G(black) and recovered clock(red)

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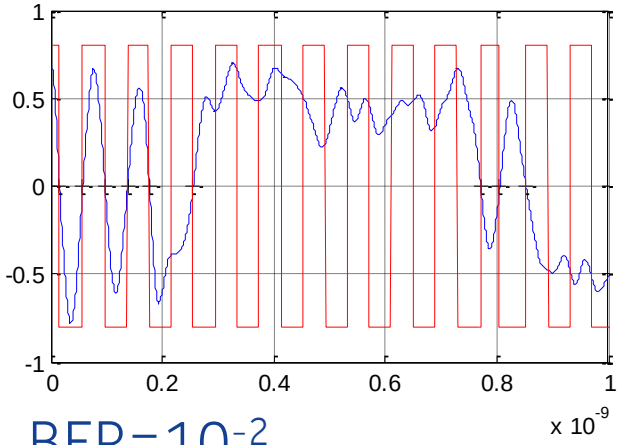
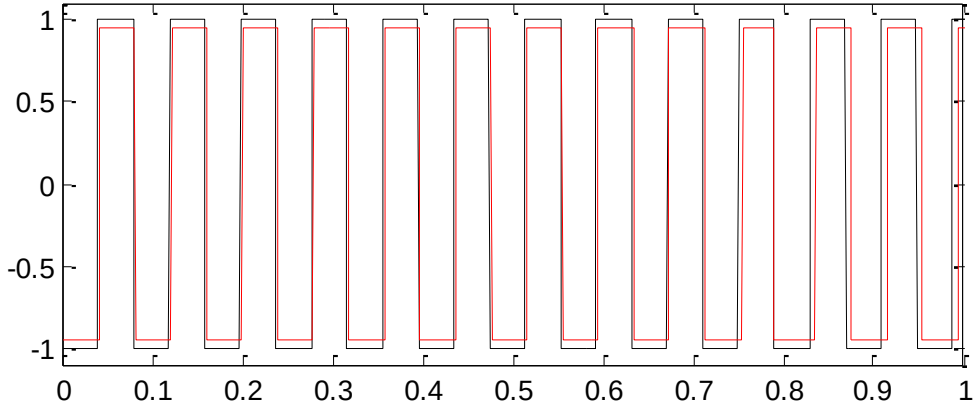
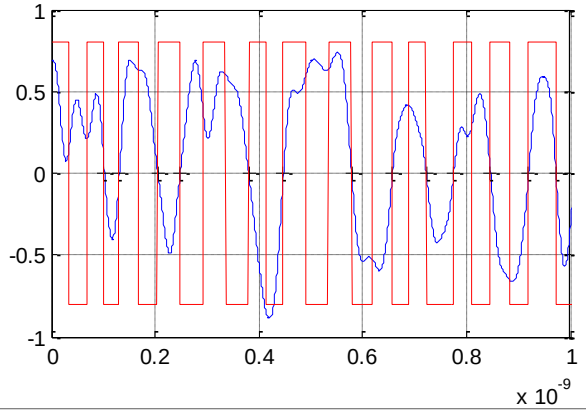
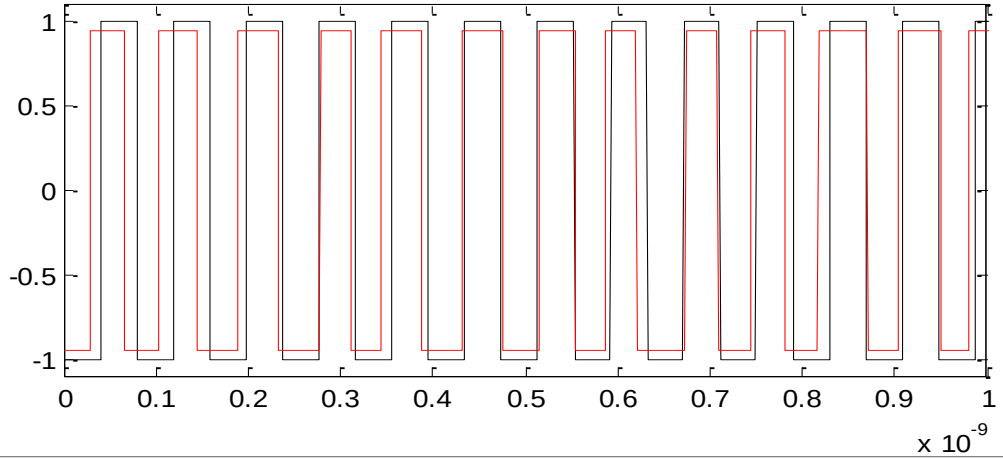
BER=10^{-3}





BER=10^{-2}





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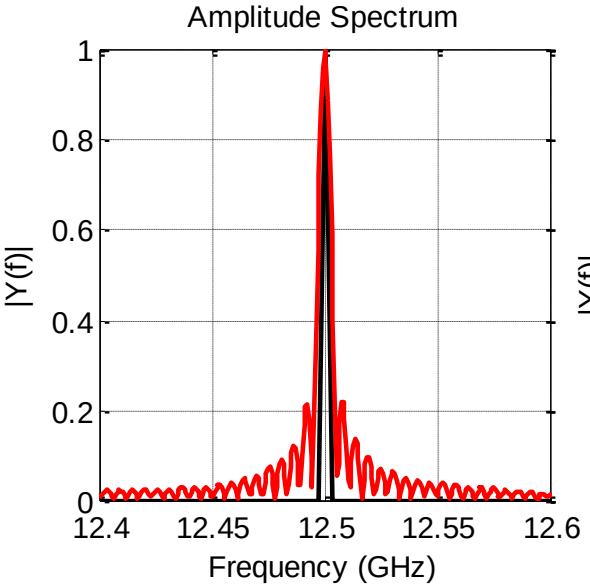
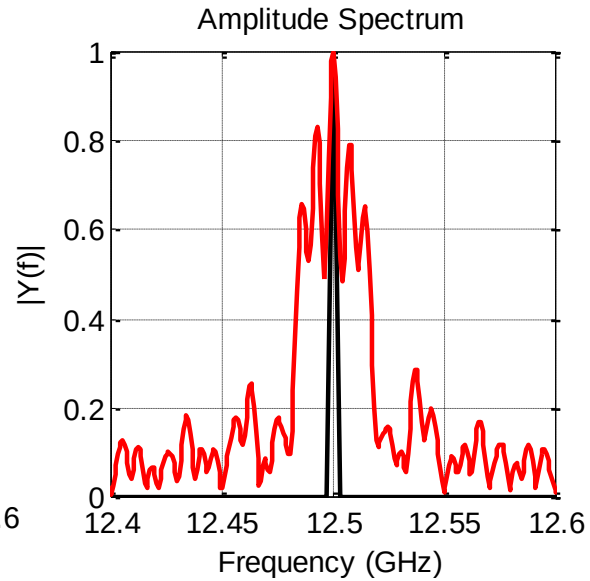
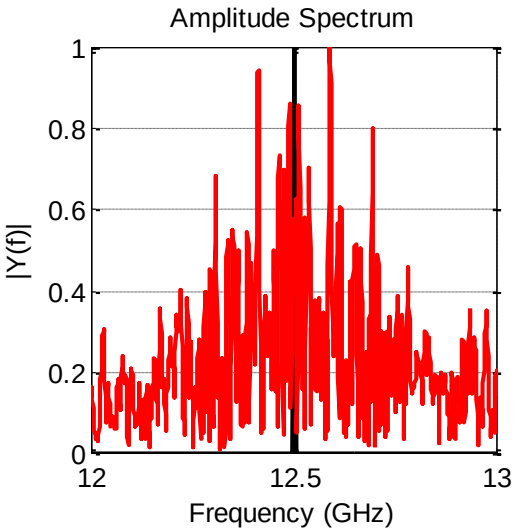
Frequency of recovered clock at different received powers (BERs)



BER=10^{-12}



BER=10^{-3}



BER=10^{-2}

For BER =10^{-2} recovered clock frequency is very dispersive making it hard for CDR to acquire lock

Conclusions :

Up to BER= 10^{-4} recovered clock is ‘very’ similar to 25G clock, so proper locking of CDR is likely possible

For BER= 10^{-3} recovered clock starts to deviate from 25G clock, however CDR locking might still be possible

For BER> 10^{-2} recovered clock starts to deviate significantly from 25G clock and proper CDR locking might not be guaranteed anymore

Conclusions :

Table of other standards with FECs

Physical layer	**Linerate**	**Standard**	**FEC**	**BERin**
100GE Backplane	25G	IEEE 802.3bj	RS(528,514) RS(544,514)	3.92E-05 3.09E-04
100GE Fiber	25G	IEEE 802.3bm	RS(528,514) RS(544,514)	3.92E-05 3.09E-04
10GE PON	10G	802.3av	RS(255,223)	1.1E-03

Up till now **no** other 25G standards proposes FECs with BERin of 10^{-2}

Recommendations :

The abilities of a CDR circuit to deal with noisy signals will be primarily determined by the characteristics of its PLL

Wider bandwidth PLL is needed for noisy signals which will do better job of tracking the data as the recovered clock data will more accurately match each individual bit.

Also locking at 25G is more difficult than at 10G, so increasing loop bandwidth of PLL (~10 MHZ) would be benifitial (10G CDRs ~ 4 MHz)

Unfortunately wider BW PLL leads to degraded output BER of CDR (due to reduced output SNR and higher output phase noise).

CDR locking at 25G for high BER needs more study especially in BM !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