LDPC for 100G EPON

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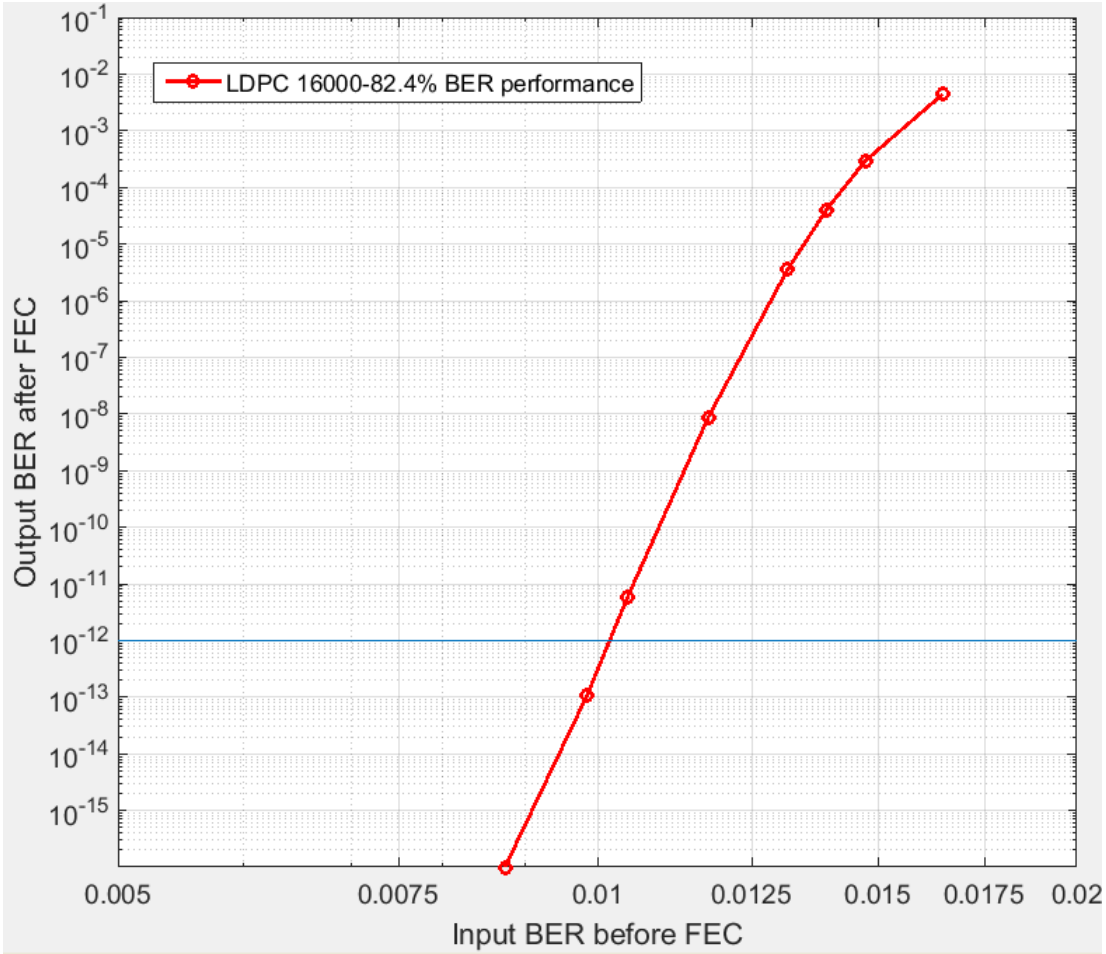
Introduction

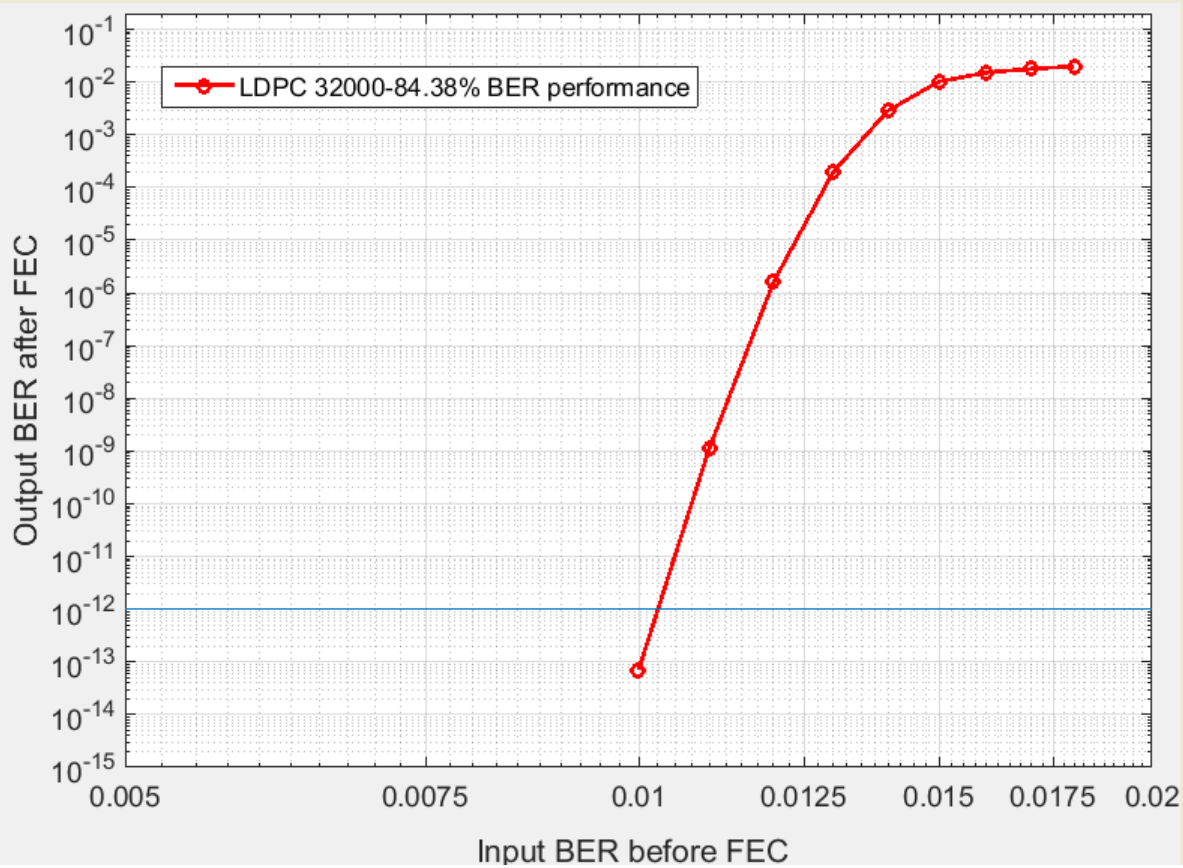
- LDPC has been defined in Docsis 3.1、G.hn，WiMAX、802.3an、802.11n and so on.
- LDPC has the error correction capability of BER_in=1.0e-2@BER_out=1.0e-12 with a code rate larger than 0.8.
- LDPC's encoding and decoding methods have been widely studied and have no IPR issues.
- In this contribution, we will present the LDPC candidate codes applicable in 100G EPON and compare their performance with other enhanced FEC candidate codes.

16K LDPC performance under AWGN channel



- 16K LDPC code in this contribution has a code rate of 0.824
- All simulations are performed based on the logical testbench
- This LDPC code is decoded based on hard decision and will have a 1.5dB electrical coding gain improvement if soft decision is implemented
- It has a correction capability of BER_in=1.0e-2
- No error floor is observed below 1e-14

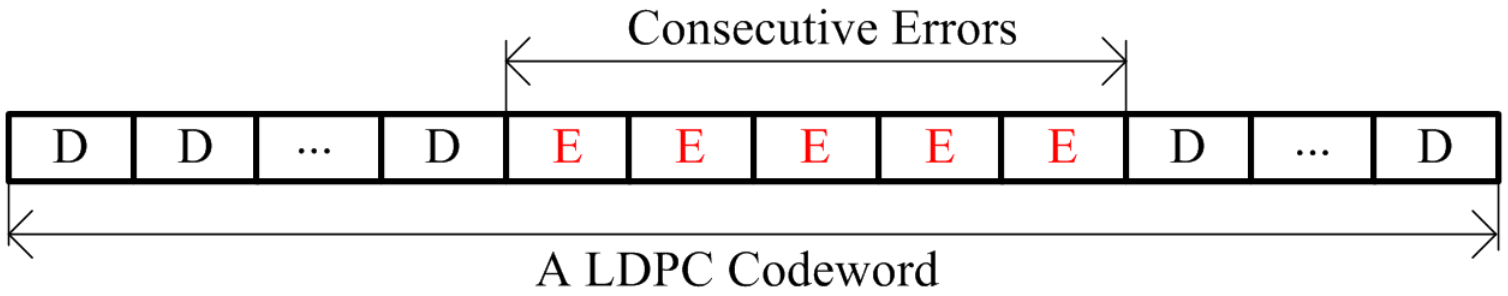
32K LDPC performance under AWGN channel



- 32K LDPC code has the same error correction capability as 16K LDPC, but a larger code rate of 0.844
- This LDPC code is also decoded based on hard decision and will have a 1.5dB electrical coding gain improvement if soft decision is performed
- No error floor is observed below 1e-14

LDPC performance under burst channel

Burst error channel is constructed by generating consecutive errors among an LDPC codeword. The burst error correction ability is defined by the maximum length of consecutive errors the LDPC code is able to correct.



The Burst error correction ability for LDPC codes is listed below:

FEC code	Burst error correction ability (bit)
16K LDPC	208
32K LDPC	335

Comparison of enhanced FEC candidate codes

FEC code	Length(bit)	Code rate	BER_in@ BER_out= 1.0e-12	Optical coding gain relative to RS(255,223) (dBo) (*a)	Burst Error Correction Capability(bit) (*b)	Relative Complexity (*c)	Estimated Decoding Latency (us)
RS(255,223)	2040	0.87	1.1e-3	0	121	1	1.2us
RS(1023,847)[1]	10230	0.83	4.2e-3	0.9~1.2	871	7	4.5us
RS(2047,1739)[1]	22517	0.85	4.5e-3	1~1.3	1684	15	7.6us
Bolded 3DBCH[2]	16K or 37K	0.83 or 0.85	1.0e-2	1.7~2.2	?	?	?
LDPC(16000,13184)	16000	0.82	1.0e-2	1.7~2.2	208	~30	6us
LDPC(32768,27648)	32768	0.84	1.0e-2	1.7~2.2	335	~33	10us

(*a) Assume APD receiver with 1 dBe=(0.7~0.9)dBo
(*b) Assume RS decoder for 25Gbps is 100K gates
(*c) The burst error correction capability for RS codes is calculated by (t-1)*m+1, referring to [3]

Summary

LDPC codes with 16K and 32K bits are introduced for 100G EPON, and are compared with other enhanced FEC codes .

- 16K and 32K LDPC codes are able to provide 2dB optical coding gain improvement with a code rate of 0.82 and 0.84, respectively
- 16K and 32K LDPC have a burst error correction ability of 208 and 335 bits
- The complexity of 16K/32K LDPC codes are around 30 times of RS(255,223). If these codes are implemented in the upstream, this complexity could be left in the OLT side.

References

[1]vanveen_3ca_1a_0317.pdf

[2]laubach_3ca_1_01117.pdf

[3]https://en.wikipedia.org/wiki/Burst_error-correcting_code

Thank you

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