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CDR locking and Error distribution at high BER for 25 Gb/s

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Introduction

- In vanveen_3ca_1b_0317 we concluded that a random noise model might not be usable for determining FEC gain in PON
- jinglei_3ca_1_0717 also found that upstream transmission of XGPON using commercial OLT receivers does not comply with a AWGN model for the errors likely due to residual settling of the burst mode OLT receiver resulting in reduced FEC gain
- Downstream continuous mode is expected to be close to AWGN model for the error distribution

We will investigate the influence of locking at high BER (needed for high gain FEC) on the performance of the 25G PON system

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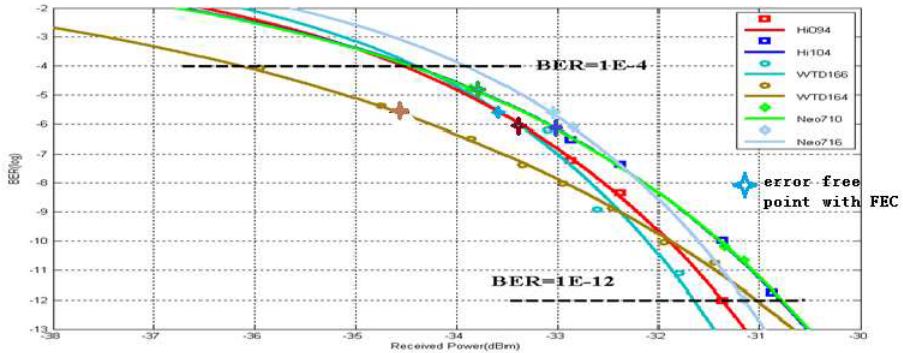
RS(248, 232) FEC gain in upstream PON

BER curve Vs FEC gain (upstream)



Transceiver	measured from BER curve (dB)	FEC gain test in system (dB)
Xcvr A	5.11	3.6
Xcvr B	3.67	3
Xcvr C	3.65	2.9
Xcvr D	3.16	2.1
Xcvr E	2.74	1.8
Xcvr E	2.5	1.7

- The test covers 6 vendors with 6 OLT optical transceivers
- It shows that the smoother BER curve , the larger GEC gain
- The input BER with error free is around 1e-5~le-6 instead of 1e-4

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- FEC gain of RS(248,232) is lower than expected for AWGN model for burst mode transmission with commercial XG-PON1 transceivers

From : jinglei_3ca_1_0717

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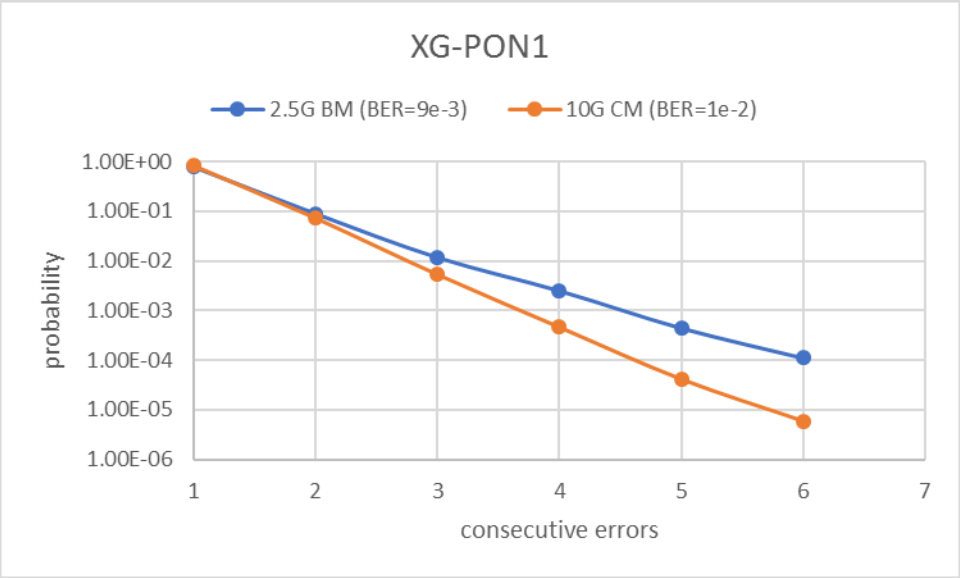
Experimental data XG-PON1
Probability burst errors

Data from: jinglei_3ca_1_0717



- Probability of burst errors is higher for burst mode transmission

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BM settling induced errors
Depends on preamble length

From: N. Brandonisio et al., "Forward error correction analysis for 10Gb/s burst-mode transmission in TDM-DWDM PONs," 2017 Optical Fiber Communications Conference and Exhibition (OFC), Los Angeles, CA, 2017

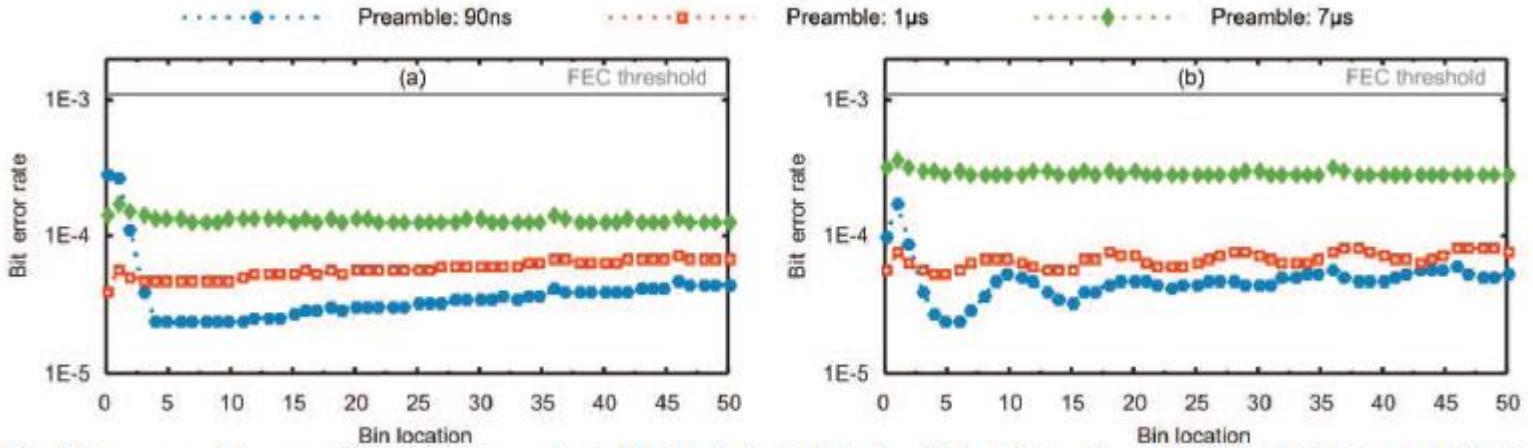

Fig. 5 Histograms of the error distribution along a single FEC block for ONU2 using 24.8ns bin duration with DR of ~0dB (a) and ~17dB (b).

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25G continuous mode experiment
Real time error statistics collection using FPGA

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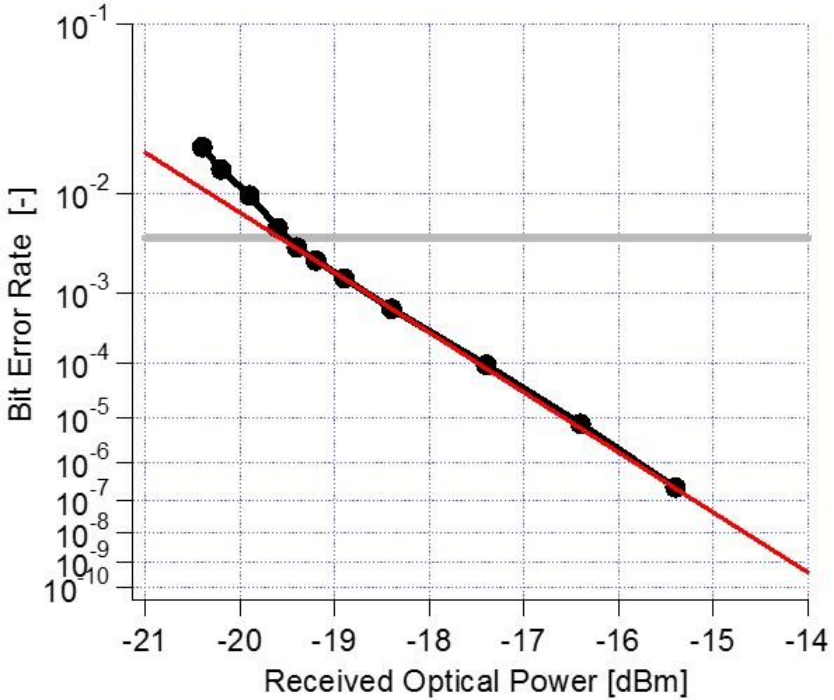
Measured BER curve

- CDR introduced penalty of ~0.4dBo:

Potential FEC gain (BER=1e-3->1e-2) of 1.64 dBo reduces to 1.24 dBo in this PIN-based experiment (APD has more shallow BER curve, so effect might be even larger)



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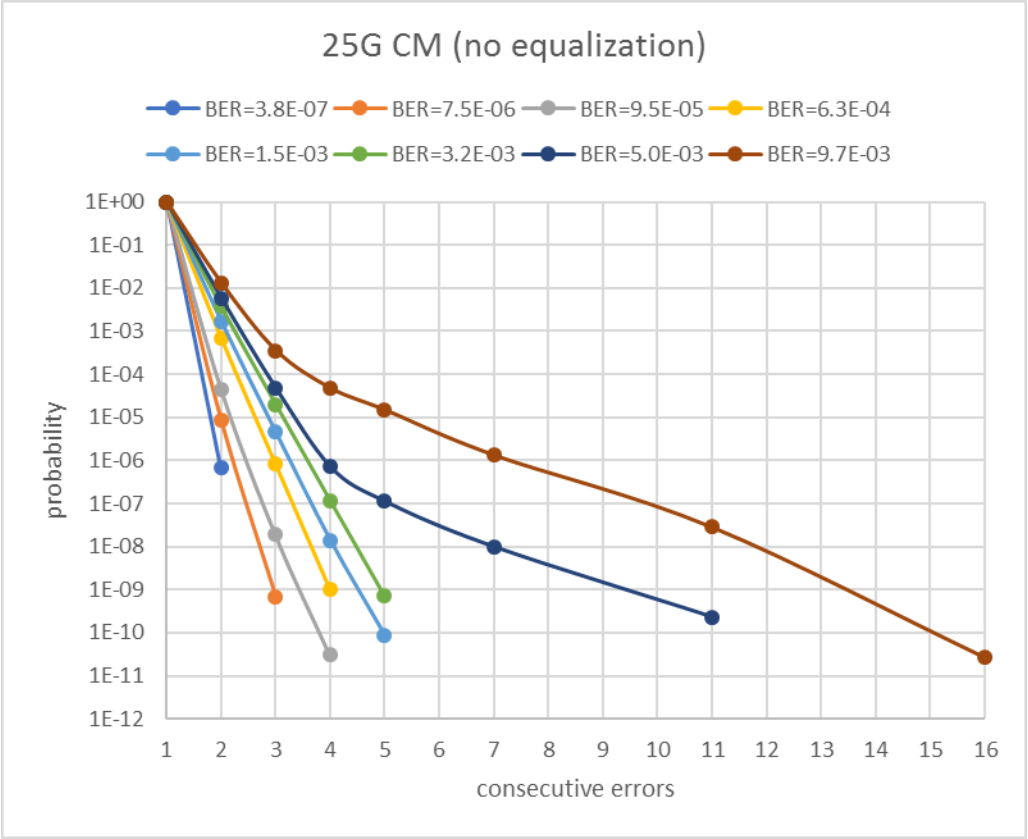
Experimental data CM 25G
Analyzing error statistics

- Probability of burst errors is higher for higher BER
- Additional reduction of FEC gain is expected due to burst errors at BERs especially beyond BER ~3e-3 with the 25G CDR we used



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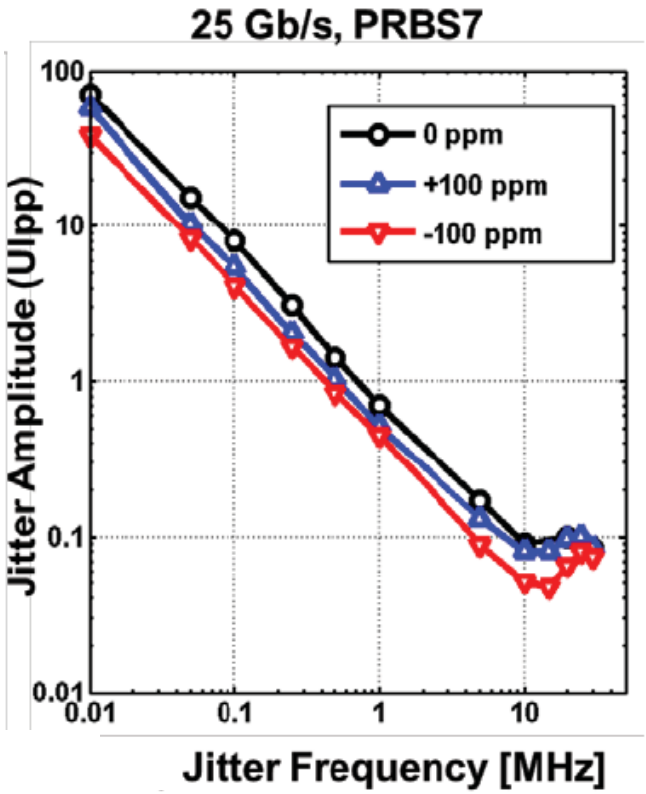
25G BM CDR in recent research
Jitter tolerance at 25 Gb/s

- At BER~1e-2 the jitter frequency is in the GHz because it is noise induced => jitter tolerance very low, CDR can not follow the jitter variations.

- Jitter tolerance is usually measured by adding MHz range noise instead of GHz noise bandwidths

The CDR jitter tolerance curve measured at BER ~ 4×10^{-12})



From: A. Rylyakov et al., "A 25 Gb/s Burst-Mode Receiver for Low Latency Photonic Switch Networks," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 3120-3132, Dec. 2015.

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Conclusions

- We showed that at high BER the CDR introduced a penalty and also introduces burst errors => the actual optical FEC gain (relative to AWGN model based FEC gain) of high gain FECs depends a lot on the performance of the CDR

- Error distribution becomes more bursty at higher BER with current available 25G CDR (FPGA transceiver)
- CDR we studied introduced a penalty of ~0.4 dBo at BER=1e-2 (PIN-based receiver)
- High gain FEC needs to be evaluated with a bursty error model to take CDR locking effects into account

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References

- Private discussion with Xin Yin of IMEC – Ghent University
- A. Rylyakov et al., "A 25 Gb/s Burst-Mode Receiver for Low Latency Photonic Switch Networks," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 3120-3132, Dec. 2015.
- N. Brandonisio *et al.*, "Forward error correction analysis for 10Gb/s burst-mode transmission in TDM-DWDM PONs," *2017 Optical Fiber Communications Conference and Exhibition (OFC)*, Los Angeles, CA, 2017


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