FEC Selection for 25G/50G/100G EPON

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Current FEC Code Proposals

A number of LDPC and RS FEC codes have been proposed and analyzed the past several meetings

From [1]

Comparison of recent FEC proposals

FEC code	OH (%)	FEC Gain (dBe) @ BERout = 1e-12	BERin for BERout = 1e-12	Optical Gain Δrel to RS(255,223)	Length (bits/usec)	Burst errors capable (bits)	Huawei		Broadcom		Nokia	
							Complexity (rel. to RS(255,223))	Latency (us)	Complexity (rel. to RS(255,223))	Latency (us)	Complexity (rel. to RS(255,223))	Latency (us)
RS(255,223) [10G EPON, XGS-PON]	12.5	7.1	1.1e-3	0	2040/0.08	121	1	1.2	1	?	1	0.3
RS(1023,847)	17	8.5	4.2e-3	1-1.3 1.3* 1.4#	10230/0.40	871	7	4.5	6.9 1.1M	E+D: 0.77	Note 1	Note 1
RS(2047,1739)	15	8.5	4.1e-3	1-1.3 1.8*	22517/0.90	1684	15	7.6	- 3.3M	E+D: 1.54	Note 1	Note 1
LDPC(16000,13184) [Huawei]	18	?	1.0e-2	1.7-2.2	16000/0.64	208	~30	6	-	-	-	-
LDPC(18493,15677) [Broadcom]	15		1e-2	2.5* 1.8# 2.5* 1.9#	18493/0.74	?	-	-	7.7 E: <0.3M D: 1.5M	E: 2.77 D: 2.92	64	14
LDPC(19200,16000) [Broadcom]	17	9.6	1e-2	2.8*/2.1#	19200/0.77	?	-	-	9.1	?	-	-
LDPC(32768,16000) [Huawei]	16.7	?	1e-2	1.7-2.2	32768/1.31	335	~33	10	-	-	-	-

zhao_3ca_1_0517 | laubach_3ca_4_0517 | laubach_3ca_1a_0917 | Nokia FPGA estimates

- Optical FEC gain, latency, complexity, and burst error capability are all important

Note 1 - estimation in progress
* - AWGN noise model
\# - Gilbert Elliot noise model

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Comparison of Proposed RS and LDPC Codes

Performance

- Proposed LDPC codes have a higher theoretical optical gain when compared with RS codes of similar code lengths (~0.5-1 dBo), [1]

Issues

- Need to operate in a high input-BER region (4E-3 to 1E-2) to achieve this extra gain
- Upstream burst mode performance in this BER region is largely unknown or shows error propagation issues [2] and degraded performance from theoretical
- LDPC codeword length can be shortened for smaller upstream bursts, but this limits the use of an interleaver, and has a significant impact on the code rate for short codes [3], or producing error floors if puncturing [4]
  (e.g., for a 100-byte payload, the code length is 3618, i.e., a rate of 0.22)
- Other similar P2MP standards (EPoC, DOCSIS 3.1) handled shortened US bursts with three different LDPC codes of different length and rate (added complexity)
- Complexity and encoding/decoding & latency for LDPC is higher than for RS codes of similar length

Upstream Risks

- LDPC codes bring a lot of risks for speculative performance
- LDPC may not perform as well as RS codes for high input-BER & short US burst lengths

Shortening calculations

FEC block code sizes proposed:

- LDPC - 16,000 to 32,768 bits
- RS - 10,230 bits (RS(1023,847)) to 22,517 bits (RS(2047,1739))

Calculation of code rates with shortening
(fixed the input BER and set the output BER to 1E-12)

- **RS(255,223)** - Max input BER-1.05E-3, shortened both information & parity symbols keeping input & output BER constant; Lowest info length 64 bytes, Code rate = 0.744

- Similarly, but now with higher input BER
  - **RS(1023, 847)** - p_BER_in = 4.22E-3, R_min = 0.575, R_max = 0.829
  - **RS(2047,1739)** - p_BER_in = 4.08E-3, R_min = 0.569, R_max = 0.850
  - **LDPC(18493,15677)** - p_BER_in = 1E-2, R_min = 0.1538

Observations

To minimize risks, perhaps RS codes are the best choice for upstream burst mode operation, whereas an LDPC code for downstream continuous mode might give better performance

Past Working Assumptions

- It is desirable to use the same FEC for DS and US (BCM request for ASIC testing/verification purposes)

Proposals

Proposal. Use an LDPC code in the downstream and an RS code in the upstream

This could be the optimal solution, where

- The performance gain for full-length LDPC codes are exploited for the continuous-mode downstream
- The reconfigurability and burst error capabilities of RS codes are exploited for the burst-mode upstream.

Alternative proposal. Use a RS code for both upstream and downstream.

This proposal

- Satisfies the request to use the same FEC codes in both directions for ASIC testing and verification purposes
- Provides extra robustness against burst errors

References

[1] B. Powell et al., Latency and Complexity for Various 25/50/100G FEC Code Proposals, powell_3ca_2a_0917, Charlotte, NC, Sep. 2017

[2] D. van Veen, et. al., CDR Locking and Error distribution at High BER for 25 Gb/s, houtsma_3ca_2_1117, Orlando, FL, Nov. 2017

[3] M. Laubach et al., FEC Proposal for NGEPON - update, laubach_3ca_1_1117, Orlando, FL, Nov. 2017

[4] R. Bonk et al., LDPC Code Length Reduction, bonk_3ca_1_1117, Orlando, FL, Nov. 2017