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143. Multi-Point Reconciliation Sublayer (MPRS) for 100G-EPON

143.1 Overview

per Draft 0.5

Figure 143–1—100G-EPON Layering diagram

143.2 Summary of major concepts

143.2.1 Concept of a logical link and LLID

143.2.1.1 Physical Layer ID

143.2.1.2 Management Link ID

143.2.1.3 User Link ID

143.2.1.4 Group Link ID

143.2.2 25 Gb/s, 50 Gb/s, and 100 Gb/s operation over P2MP media

143.2.2.1 MPRS channels

143.2.2.2 Binding of multiple MACs to multiple PCS instances

143.2.3 Transmission and reception over multiple MPRS channels

143.2.3.1 Transmission Unit

per ms word submission

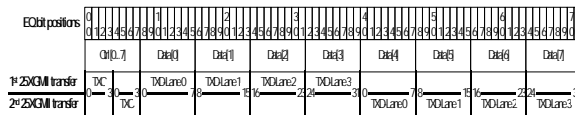


Figure 143-2—Envelope Quantum (EQ) format

143.2.3.2 Transmission Envelopes

per ms word submission

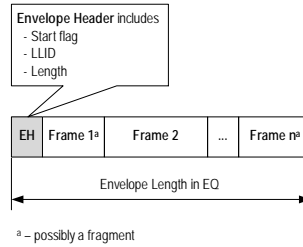


Figure 143-3—Transmission envelope structure

143.2.3.3 Envelope Headers

per ms word submission

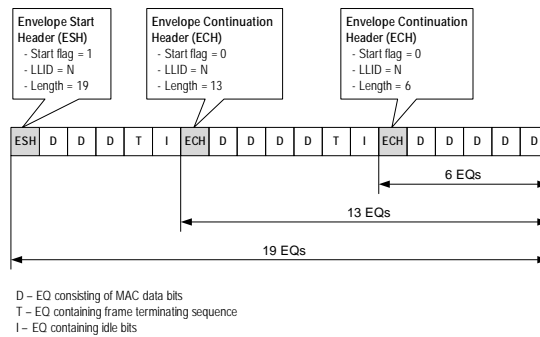
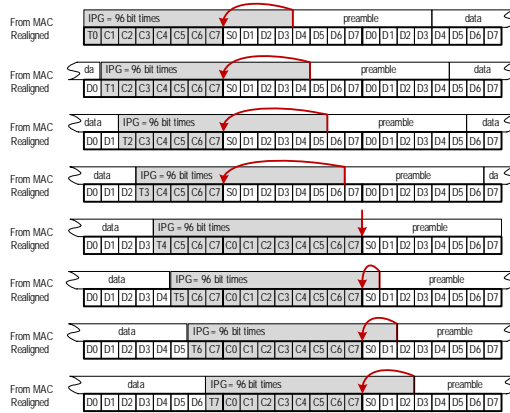


Figure 143-4—An illustration of a transmission sequence consisting of three frames

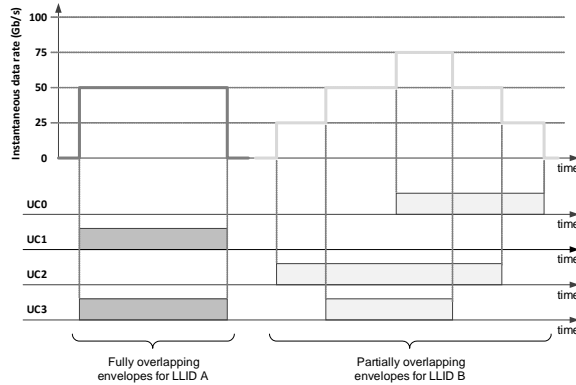
143.2.3.4 Interpacket gap adjustment



per ms word submission

Figure 143-5—An illustration of a Start control character alignment to octet 0

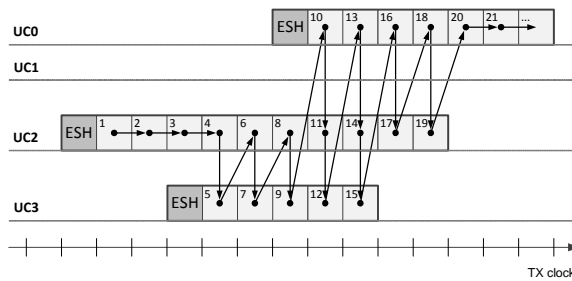
143.2.4 Dynamic channel bonding



per ms word submission

Figure 143-6—Full or partial envelope

143.2.4.1 LLID transmission over multiple MPRS channels



per ms word submission

Figure 143-7—Fill order of overlapping envelopes

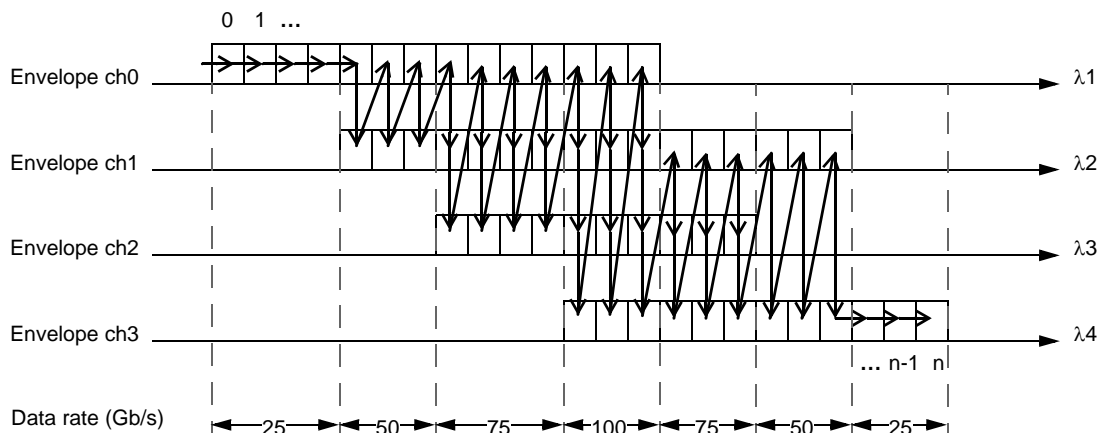


Figure 143-8—Overlapping transmission envelopes

143.2.4.2 Channel skew remediation mechanism

143.2.4.3 ENV_TX and ENV_RX buffers

143.2.4.4 Envelope Position Alignment Marker

143.3 100G-EPON MPRS Requirements

143.3.1 MPRS and MPCP clock synchronization

143.3.2 Delay variability constraints

143.4 MPRS Functional Specifications

143.4.1 MPRS Interfaces

Fig 143-1 draft 0.5

Figure 143-9—100G-EPON MPRS inputs and outputs

143.4.1.1 PLS service primitives

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Table 143–1—Mapping of PLS_DATA.request primitives

MAC operating speed	Transmit interface	Signals
25G-EPON	25GMII[0]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK ^a
50G-EPON	25GMII[0] 25GMII[1]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK ^a TXD[1]<31:0>, TXC[1]<3:0>
100G-EPON	25GMII[0] 25GMII[1] 25GMII[2] 25GMII[3]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK ^a TXD[1]<31:0>, TXC[1]<3:0> TXD[2]<31:0>, TXC[2]<3:0> TXD[3]<31:0>, TXC[3]<3:0>

^a All transmit 25GMII interfaces share a common clock.

Table 143–2—Mapping of PLS_DATA.indication primitives

MAC operating speed	Receive interface	Signals
25G-EPON	25GMII[0]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0]
50G-EPON	25GMII[0] 25GMII[1]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1]
100G-EPON	25GMII[0] 25GMII[1] 25GMII[2] 25GMII[3]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1] RXD[2]<31:0>, RXC[2]<3:0> and RX_CLK[2] RXD[3]<31:0>, RXC[3]<3:0> and RX_CLK[3]

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143.4.1.1.1 Mapping of PLS_DATA[<i>ch</i>].request primitive	1
143.4.1.1.2 Mapping of PLS_SIGNAL[<i>ch</i>].indication primitive	2
143.4.1.1.3 Mapping of PLS_DATA[<i>ch</i>].indication primitive	3
143.4.1.1.4 Mapping of PLS_DATA_VALID[<i>ch</i>].indication primitive	4
143.4.1.1.5 Mapping of PLS_CARRIER[<i>ch</i>]. indication primitive	5
143.4.1.2 MPRS Control Primitives	6
143.4.1.2.1 MPRS_CTRL[<i>ch</i>].request(<i>link_id</i> , <i>epam</i> , <i>env_length</i>) primitive	7
143.4.1.2.2 MPRS_CTRL[<i>ch</i>].indication(<i>cw_left</i>) primitive	8
143.4.1.3 25GMI interfaces	9
143.4.2 Envelope Header format	10

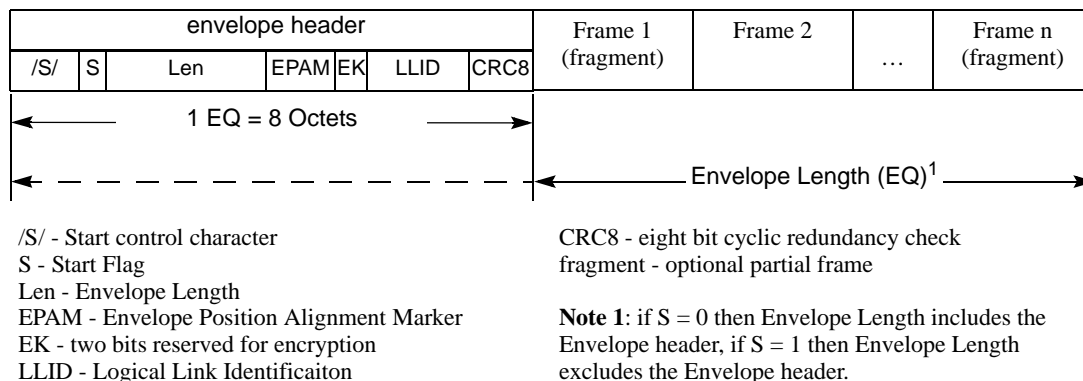


Figure 143–10—Transmission envelope structure

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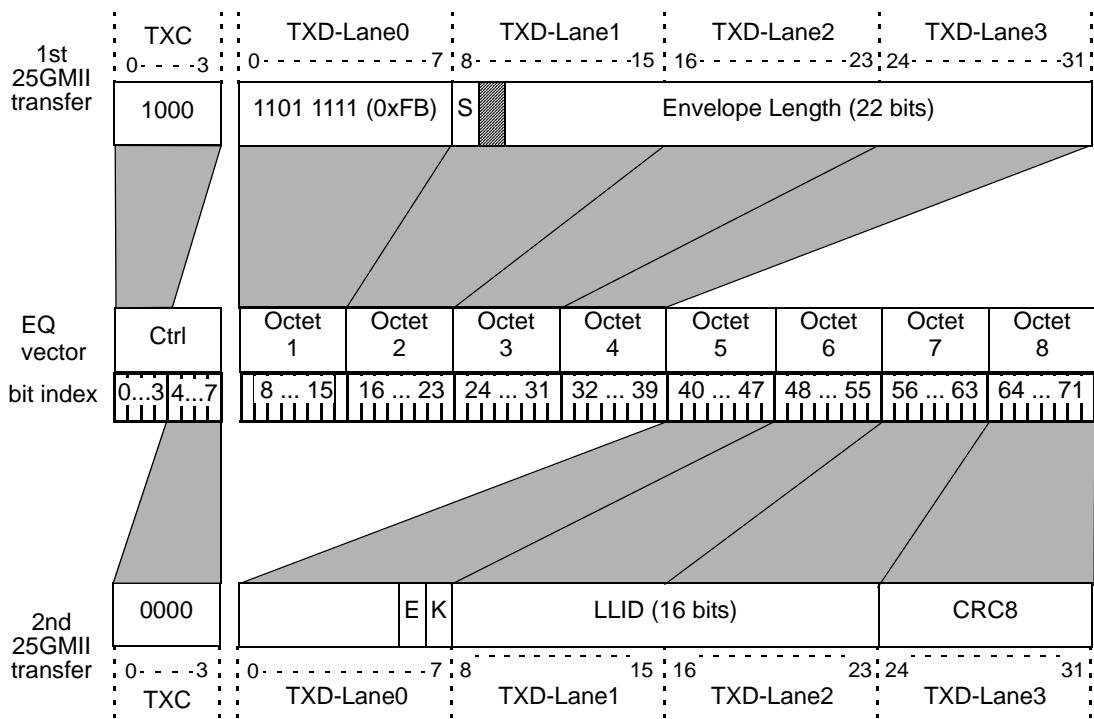


Figure adapted from kramer_3ca_1a_0917.pdf slide 13 “Envelope Header (EQ Format)”

Key
 S - Start of Envelope (1 = yes, 0 = no) K- Encryption Key Index (0, 1)
 E - Encryption (1 = enabled, 0 = disabled) ▨ - reserved (value = 0 for CRC8 calculation)

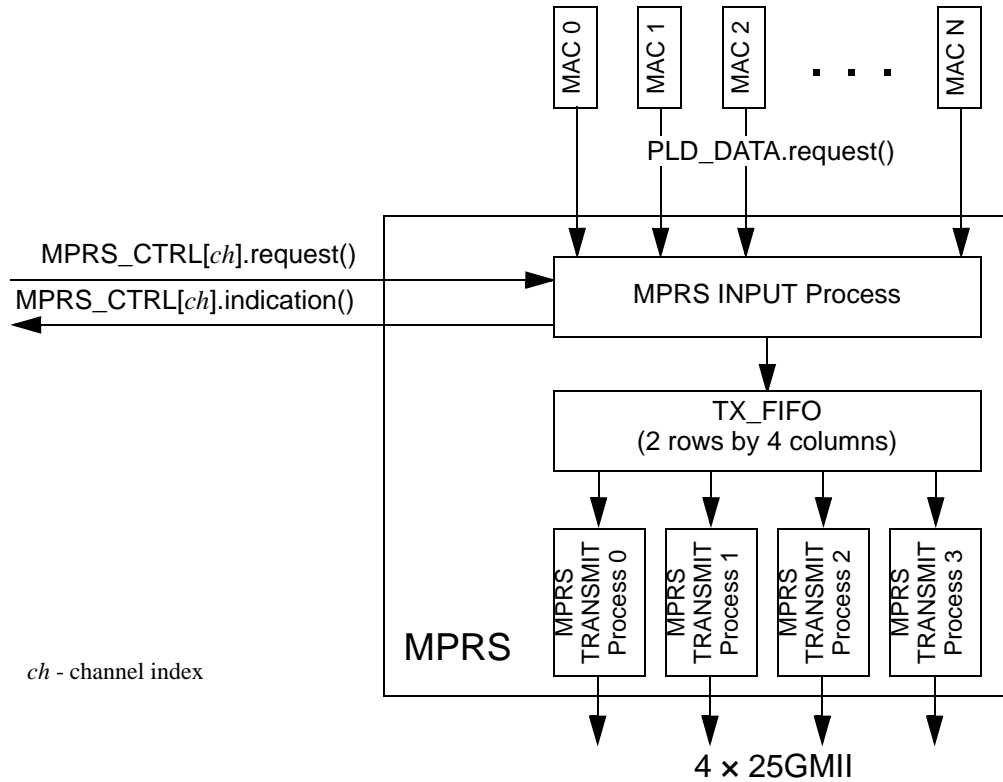
Figure 143–11—Transmission envelope header format

Table 143–3—Envelope Header EQ

EQ Bits	Value	Description
0-7	0x80	Control bits corresponding to TXC<3:0> in two successive MII transfers
8-15	0xFB	Start Control Code
16	0 for ECH 1 for ESH	Start Flag
17	0	reserved
18-39	varies	Length of envelope (in EQ)
40-45	varies	Envelope Position Alignment Marker (Number of bits matches the size of wRow)
46-47	0x0	reserved
48-63	varies	LLID
64-71	varies	CRC8

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1 **143.4.3 Transmit functional specifications**
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29 **Figure 143–12—100G-EPON MPRS transmit functional block diagram**

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 31
 32 **143.4.3.1 Conventions**

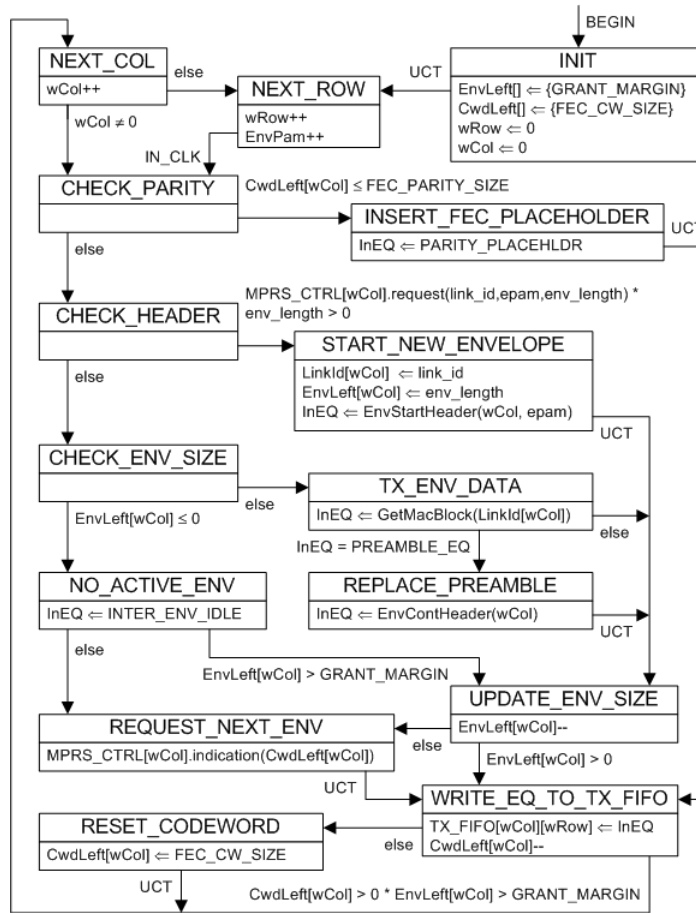
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 34 **143.4.3.2 Constants**

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 36 **143.4.3.3 Variables**

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 38 **143.4.3.4 Functions**

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 40 **143.4.3.5 State Diagrams**
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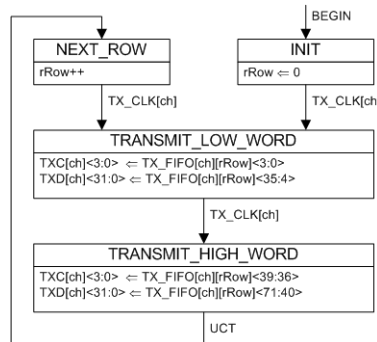
143.4.3.5.1 Input Process



per kramer_3-ca_1a_0917.pdf slide 15 or similar (CHR Motion #5)
 “TxEQ = REAMBLE_EQ” replaced with “TxEQ = PREAMBLE_EQ” on exit from TX_ENV_DATA
 “TxEQ” replaced with “InEQ”

Figure 143-13—MPRS Input Process state diagram

143.4.3.5.2 Transmit Process



kramer_3ca_1a_1116.pdf slide 13 or similar (SA Motion #4)

Figure 143-14—MPRS Transmit Process state diagram

143.4.4 Receive functional specifications

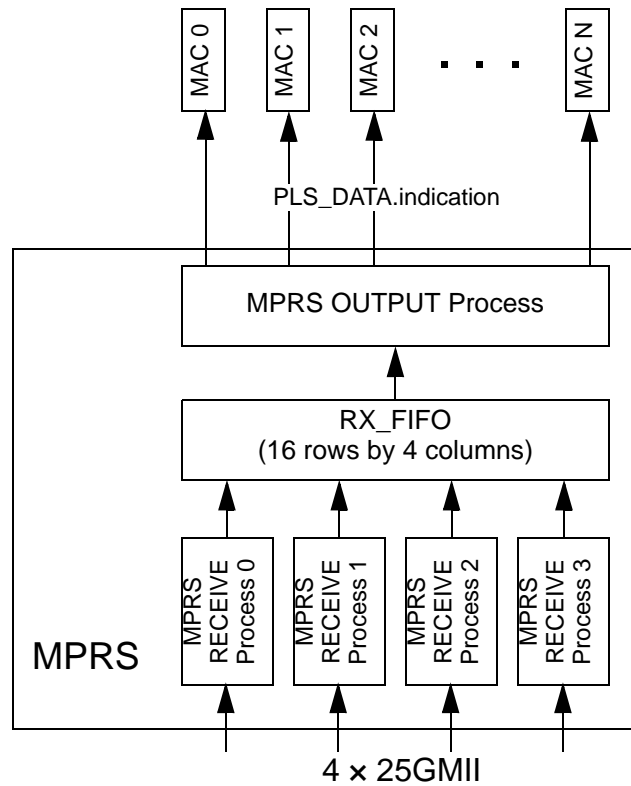


Figure 143–15—100G-EPON MPRS receive functional block diagram

143.4.4.1 Conventions

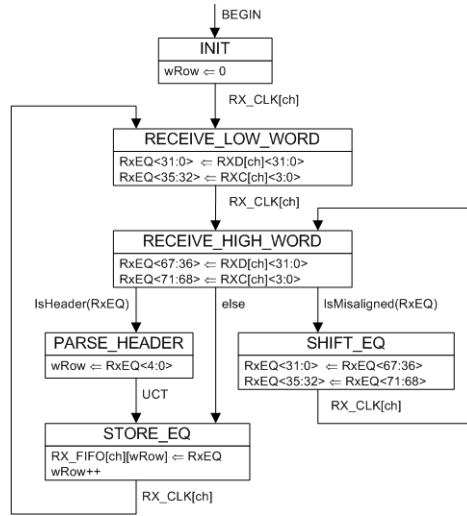
143.4.4.2 Constants

143.4.4.3 Variables

143.4.4.4 Functions

143.4.4.5 State Diagrams

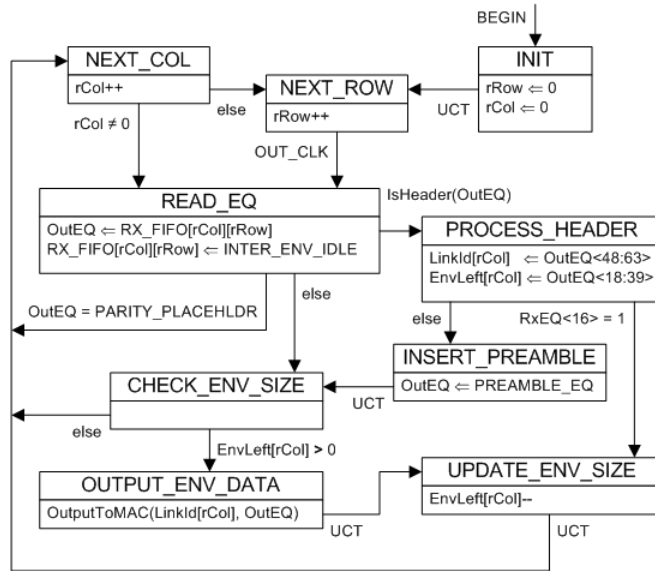
143.4.4.5.1 Receive Process



kramer_3-

Figure 143-16—MPRS Receive Process state diagram

143.4.4.5.2 Output Process



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er_1a_0917.pdf slide 20 or similar (CHR Motion #5)

Figure 143-17—MPRS Output Process state diagram

143.5 Channels with asymmetric rates

143.5.1 Mapping of 25GMII and XGMII primitives at the OLT

143.5.2 Mapping of 25GMII and XGMII primitives at the ONU

1 **143.5.3 MPRS channel operation at 10 Gb/s**

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3 **143.5.3.1 Changes to Input Process**

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5 **143.5.3.2 Changes to Transmit Process**

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7 **143.5.3.3 Changes to Receive Process**

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9 **143.5.3.4 Changes to Output Process**

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