Latency Consideration for LDPC FEC Code

IEEE 802.3ca Meeting, Orlando, Florida

November 2017

Zheng Liu, Junwen Zhang, and Jun Shan Wey

Introduction

- In the IEEE802.3ca meeting in September 2017, an action item was assigned to further investigate latency requirements for LDPC FEC code
- This contribution reports the results of our investigation on latency as well as complexity

Comparison of recent FEC proposals

powell_3ca_1a_0917

FEC code	OH (%)	FEC Gain (dBe) @ BERout = 1e-12	BERin for BERout = 1e-12	Optical Gain Δ rel to RS(255,223)	Length (bits/ usec)	Burst errors capable (bits)	Huawei		Broadcom		Nokia	
							Complexity (rel. to RS(255,223))	Latency (us)	Complexity (rel. to RS(255,223))	Latency (us)	Complexity (rel. to RS(255,223))	Latency (us)
RS(255,223) [10G EPON, XGS-PON]	12.5	7.1	1.1e-3	0	2040/ 0.08	121	1	1.2	1	?	1	0.3
RS(1023,847)	17	8.5	4.2e-3	1-1.3 1.3* 1.4#	10230 /0.40	871	7	4.5	6.9 1.1M	E+D: 0.77	Note 1	Note 1
RS(2047,1739)	15	8.5	4.1e-3	1-1.3 1.8*	22517 /0.90	1684	15	7.6	- 3.3M	E+D: 1.54	Note 1	Note 1
LDPC(16000,13184) [Huawei]	18	?	1.0e-2	1.7-2.2	16000 /0.64	208	~30	6	-	-	-	-
LDPC(18493,15677) [Broadcom]	15		1e-2	2.5* 1.8# 2.5* 1.9#	18493 /0.74	?	-	-	7.7 E: <0.3M D: 1.5M	E: 2.77 D: 2.92	64	14
LDPC(19200,16000) [Broadcom]	17	9.6	1e-2	2.8*/2.1#	19200 /0.77	?	-	-	9.1	?	-	-
LDPC(32768,16000) [Huawei]	16.7	?	1e-2	1.7-2.2	32768 /1.31	335	~33	10	-	-	-	-

zhao_3ca_1_0517 laubach_3ca_4_0517 Nokia FPGA estimates

laubach_3ca_1a_0917

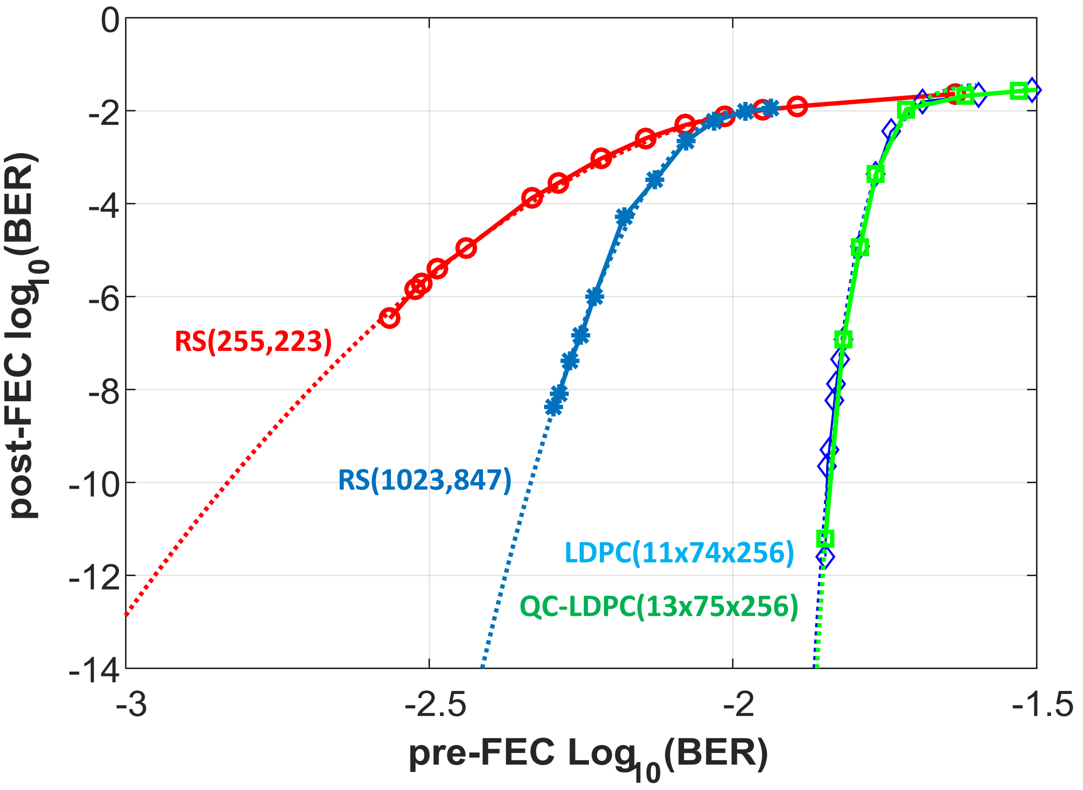
- Optical FEC gain, latency, complexity, and burst error capability are all important

Note 1 - estimation in progress
* - AWGN noise model
\# - Gilbert Elliot noise model

NOKIA

Simulation results of RS and LDPC code performance

- Channel model: AWGN
- Simulation results for LDPC code is based on soft decision input
- RS code is always based on hard decision input



Latency requirements for big video and 5G fronthaul

Latency is an major design factor and must be considered in NG-EPON standards

Potential latency sensitive services:

- Big video applications and 5G mobile fronthaul transport (wey_3ca_1_0117, wey_3ca_1_0317, powell_3ca_1_0917)

Expectation for **big video applications**:

- Max tolerable delay for 4K VR video (28 Mb/s bandwidth with compression) is ~20 ms
- Experimentally verified in a G-PON test bed. Latency should not be a concern for video applications

Expectation for max one-way latency in the **wireless fronthaul transport** link

- 3GPP: 250 μs [1]
- eCPRI and IEEE P1914: 100 μs [2,3]

Factors contributing to latency

- For 5G wireless fronthaul transport over PON, main contributing factors of latency include fiber propagation delay, DBA, processing time of other functions in OLT/ONU. In this contribution, we discuss the latency due to FEC.
- Factors contributing to FEC computation latency:
  - Decoding delay is the main contributor. It is typically 5-10 times of coding delay
  - Number of iterations in decoding process
  - Interleaving to mitigate burst errors is generally small
- Exact value of latency depends on specific code design and implementation
  - No theoretical prediction available
  - Estimate the latency by comparing RS and LDPC decoding delay with different decoding iterations (see next page)

Estimate decoding latency for LDPC(18944,16128)

- Decoding latency for LDPC code depends on the number of iterations needed to correct the errors
- Initial condition: BER=1e-2
- All values are an average over 1000 simulation results

	RS(255,223)	LDPC(18944,16128)
Baseline	2 μs	
15 iterations		6 μs
30 iterations		13 μs
50 iterations		21 μs

- With 50 iterations, LDPC decoding latency is ~ 10x of RS decoding latency
- Simulation results only give a ballpark estimate of the ratio. Actual latency values need to be verified in hardware (FPGA)

Encoding latency

- Latency due to encoding is typically much less than decoding latency
- However, when the code matrix is not in a typical lower triangular matrix format, it could have higher complexity comparing to regular LDPC code.
  - In laubach_3ca_1a_0917 with 18k code word size: 2.77 μs for encoding; 2.92 μs for decoding
- Careful selection of a code matrix is a must
- Encoding process needs to be shared with 802.3ca members in the code selection process. Example coding process: Clause 7.1.3.2.1.1 of G.9960 https://www.itu.int/rec/T-REC-G.9960/en

Complexity discussion

- In several 802.3ca contributions, complexity of LDPC code relative to RS(255,223) ranges from 7-30 for different code word lengths (powell_3ca_1a_0917)
- Complexity of LDPC code depends on specific chipset design, e.g., clock frequency, parallelism, fixed-point bit width, bit loading, and channel bandwidth
- Here are a few independent examples of single decoder complexity based on adaptive logic module (ALM) gate count
  - RS(255,223): ~ 4.5k-5k, for 25/50 GbE [4]
  - LDPC(16200,14400) ~20k-88k [5, for DOCSIS3.1]: complexity is 4-20x of RS code
  - LDPC(8176, 7156) ~42K-96K [5, for NASA GSFC]: complexity is 10-24x of RS code
- Complexity at higher rate needs to consider, additionally, the degree of parallelism and the amount of modules could be reused

Summary

- 5G fronthaul transport has stringent latency requirement: max one-way end-to-end latency ~100 μs according to eCPRI and IEEE1914
- LDPC decoding latency is about ~6-21 μs for 15-50 iterations. This is ~3-10 times of RS decoding latency. RS code may be needed to support 5G wireless fronthaul transport
- Encoding latency is typically much lower than decoding latency. However, it could be comparable to decoding latency depending on specific design
- Encoding process needs to be shared with 802.3ca members to select the most suitable code

References

1. 3GPP Release 14, TR 38.801 V14.0.0 (2017-03)
2. eCPRI Transport Network D0.1 (2017-08-30)
3. IEEE P1914.1/D0.1 Draft Standard for Packet-based Fronthaul Transport Networks
4. Intel, “High-speed Reed-Solomon IP Core User Guide,” UG-01166, 2016-11-02
5. Altera, “LDPC IP Core User Guide,” UG-01156, 2016-05-01

Thank You!