Data Rate to Line Rate Conversion (Further Optimization)

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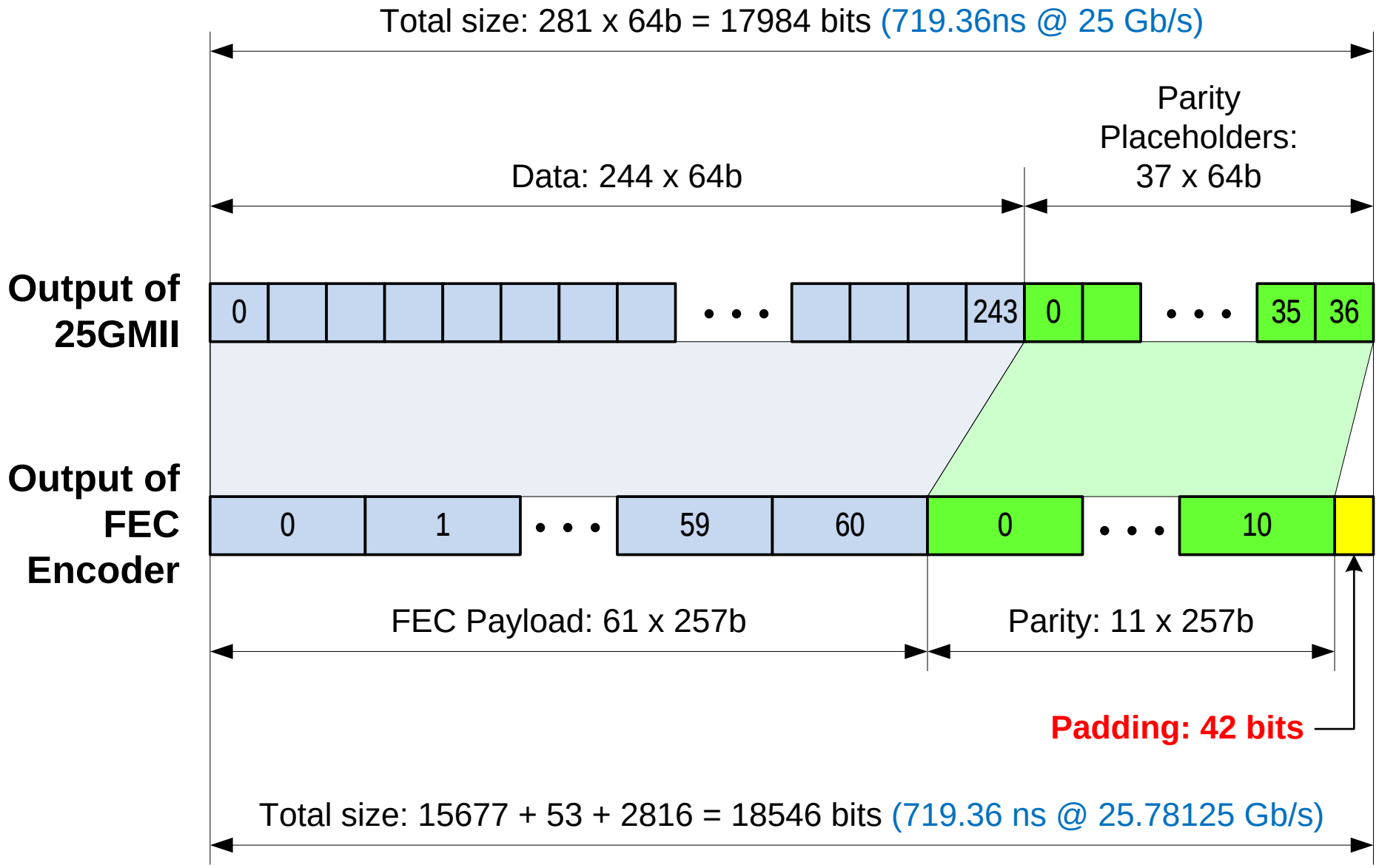
History

- The 256b/257b encoding is more efficient compared to 64b/66b and this increases the available link capacity
  - But there is a question on how to get enough data from MAC to fill the increased available link capacity.
- At the Geneva meeting, we agreed to use “approach #2” (see kramer_3ca_4a_0118.pdf)
  - Keep MAC/MPRS/25GMII data rate as is and inflate the data below 25GMII to fill the extra capacity
    - This method is outlined in gao_3ca_1_0118.pdf
    - MPRS generates fewer parity placeholders than needed for the FEC encoding.
    - PCS/FEC encoder adds the actual parity. This inflates the data to fill the extra capacity

Illustration of 2nd approach



The problem

- All state diagrams (functions) in PCS are defined to output fixed-size units at fixed rates

- It is hard to define a state diagram that needs to output, for example, 257-bit blocks most of the time, but occasionally a 42-bit padding.

Solution

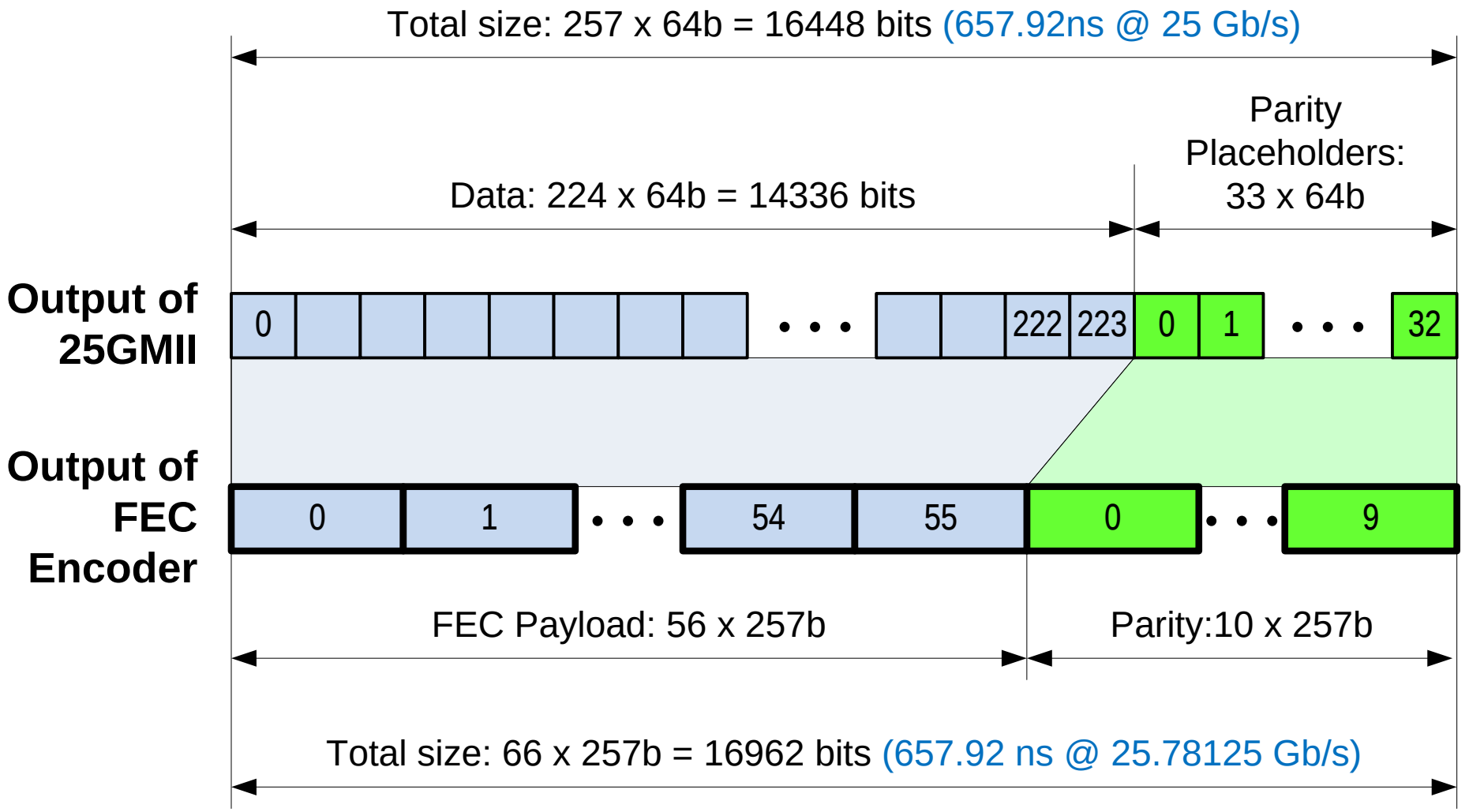
- If we reduce FEC codeword from **72** 257-bit blocks to **66** 257-bit blocks (~8.5% reduction), the MAC rate and line rate will align perfectly:

- **257 64-bit blocks @ 25 Gb/s = 66 257-bit blocks @ 25.78125 Gb/s**

- Now, all PCS processes can operate on a fixed block size (vector) and no padding is necessary.

- FEC codeword size in units of 257-bit blocks (payload + parity)
  - Old: 61 + 11 = 72 (+42 bit padding)
  - New: 56 + 10 = 66

Improved Alignment



Efficiency

- The new mapping is more efficient

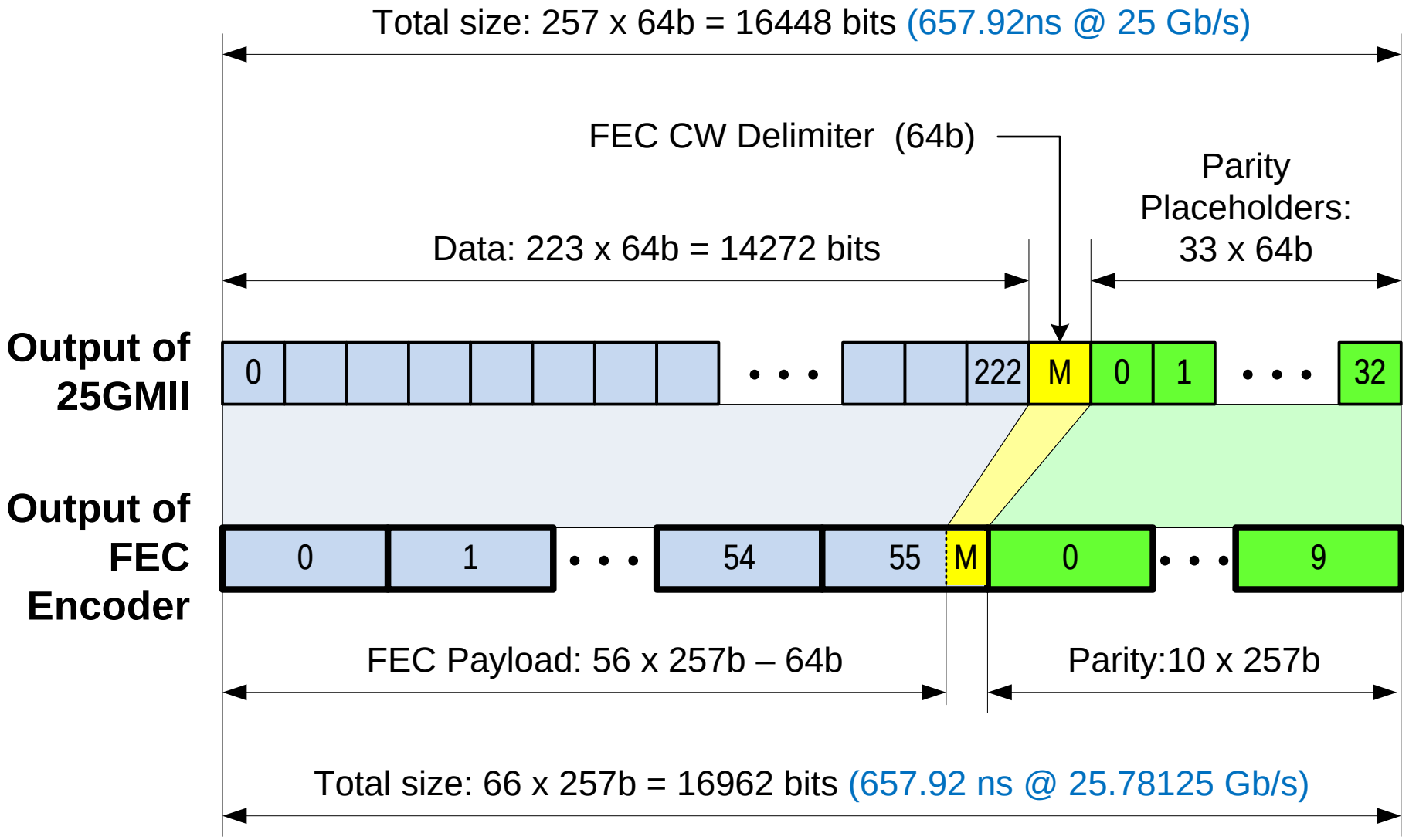
	Old	New
Code information rate	84.77%	84.90%
FEC + Line coding efficiency	84.20%	84.52%

- But, the new FEC framing leaves only 10 bits to do FEC codeword alignment.
  - ONU may take longer time to align upon power up.

- It is better to trade off extra efficiency for improved robustness
  - FEC codeword shall include an explicit alignment marker.
  - With a 64-bit marker, we get very fast alignment and good efficiency:

	Old	New+
Code information rate	84.77%	84.84%
FEC + Line coding efficiency	84.20%	84.14%

Improved Alignment with Marker



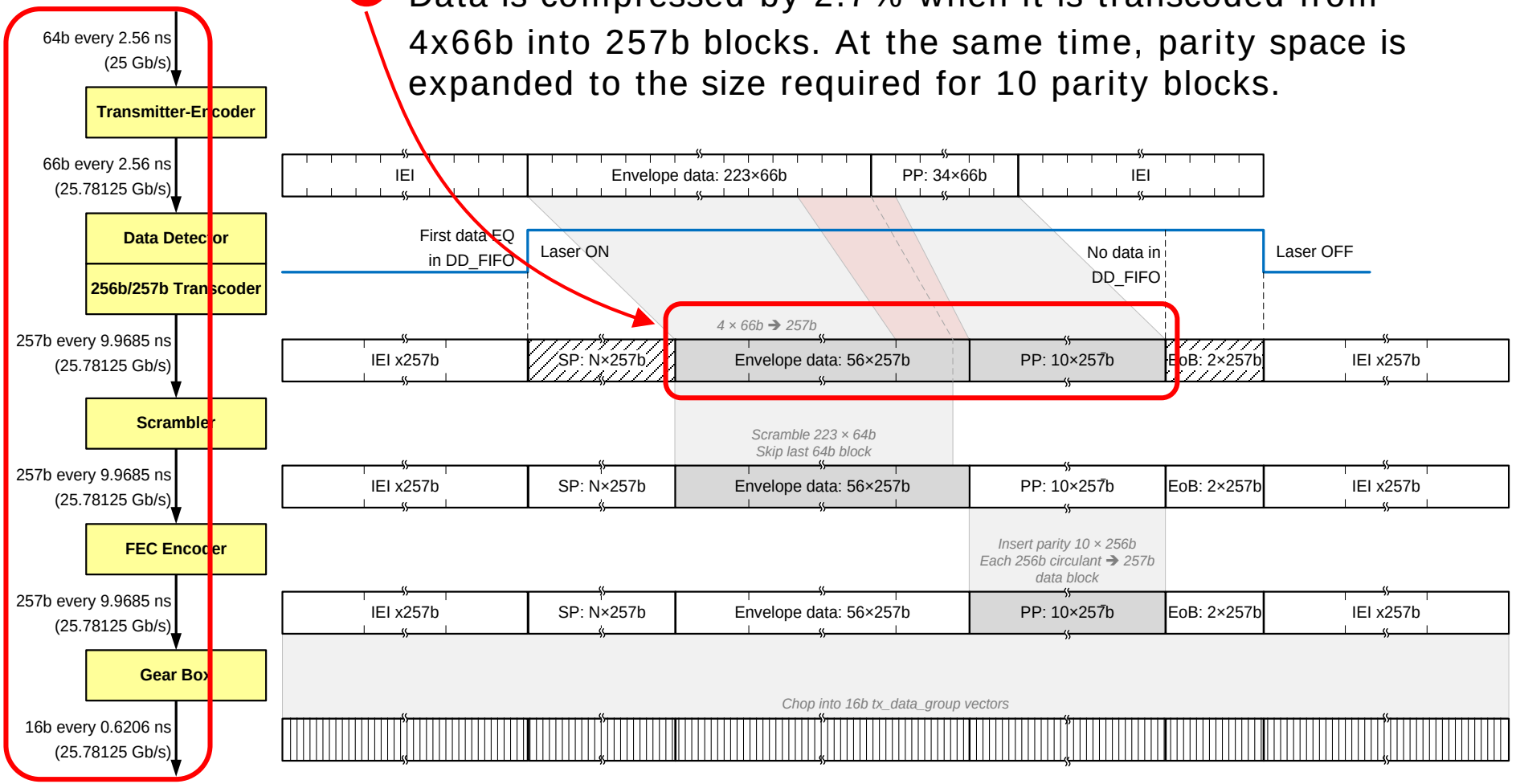
FEC code options

The FEC codeword length reduction can be achieved by increasing the number of shortened/punctured bits, or we can come up with a new parity-check matrix

	D0.7: LDPC(18493,15677)	More shortening/ puncturing	New Code LDPC(16888,14328)
Parity check matrix and circulant size	13×75×256	13×75×256	12×69×256
User bit length before shortening Transmitted: Shortened:	62×256 = 15,872 15,677 195	62×256 = 15,872 14,328 1,544	57×256 = 14,592 14,328 264
Parity bit length before puncturing Transmitted: Punctured:	13×256 = 3,328 2,816 512	13×256 = 3,328 2,560 768	12×256 = 3,072 2,560 512
Codeword length before any shortening and puncturing	19,200	19,200	17,664
Codeword length after shortening and puncturing	18,493	16,888	16,888
Code rate after shortening and puncturing	0.8477	0.8484	0.8484
Estimated NEOG delta vs. D0.7	-	-0.08 dB	-0.03 dB

Data Transformation within PCS

1. Every block accepts and outputs constant block sizes (vectors) at constant time period
2. Data is compressed by 2.7% when it is transcoded from 4x66b into 257b blocks. At the same time, parity space is expanded to the size required for 10 parity blocks.



Alignment robustness

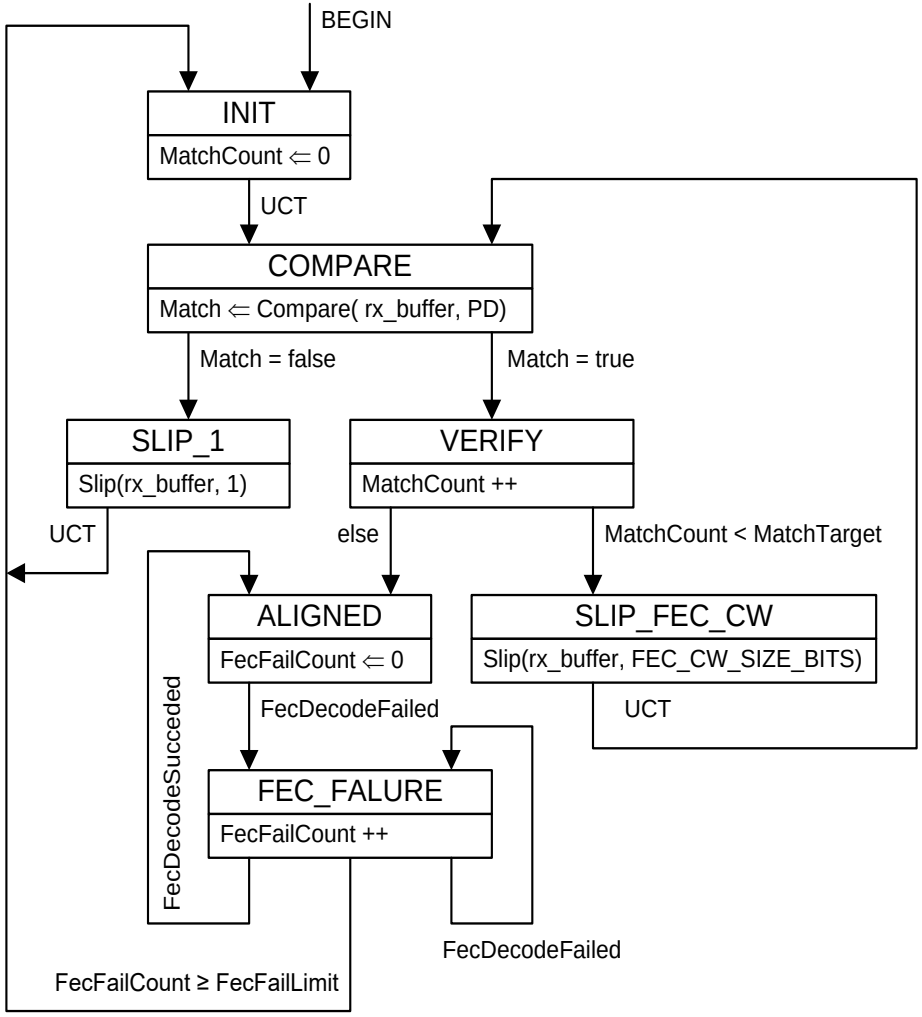
- Let's assume that from the 64-bit marker, we only use 32 bits for fixed FEC delimiter and we reserve the remaining 32 bits for possible PHY signaling.

- *Simulation analysis is coming*

FEC Alignment SD

Same alignment method as discussed in Geneva *(kramer_3ca_1_0118.pdf)*:

1. Hunt for PD (32-bits) in the received bit stream
   a) If PD is not matched, MatchCount = 0, slip incoming stream by 1 bit, go to 1.
   b) If PD is matched, MatchCount ++, slip incoming stream by 16962 bits (1 FEC CW), go to 1
2. When MatchCount reaches a threshold (5?), declare the alignment
3. If FEC decoder consistently indicates decoding failure (for 3 consecutive FEC CWs?), set MatchCount = 0, go to 1 to realign.



Conclusion

- PCS state diagrams have input and output in fixed units (vectors) at constant rate. No padding to fill fractional units.
- Signal on the wire is always formatted into 257-bit blocks.
- Fast and reliable FEC alignment with 32-bit FEC delimiter
- Slightly smaller encoder/decoder latency and buffering requirement