

# LDPC Decoder

Figure x1 illustrates the receiver LDPC decoder with shortening/puncturing, interleaver/de-interleaver data path.

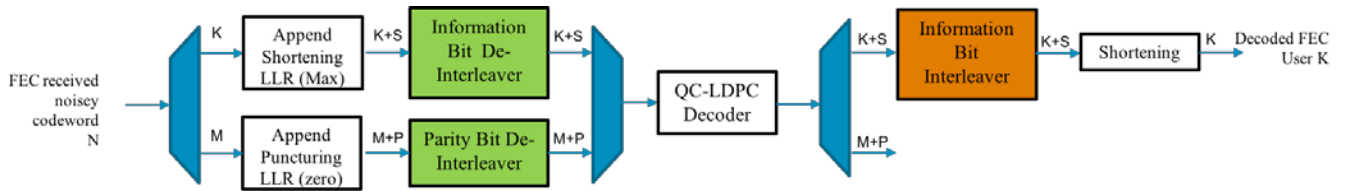


Figure x1 – FEC decoder

## Interleaver and De-Interleaver

For the purposes here: *interleaver* refers to the mapping from transmitted sequence to encoding/decoding sequence (including user and parity) and *de-interleaver* refers to the mapping from encoding/decoding sequence to transmitted sequence.

The information bit de-interleaver consists of 57 local de-interleavers of size 256-by-256. The control bit of each 257-bit block is not included in encoding and interleaving. As illustrated in Figure x2 these local interleavers are realized by 57 independent reverse-omega networks. The information bits after zero padding are divided into 57 data chunks, and each data chunk has 256 bits, which is sent to one of the 256-by-256 omega networks.

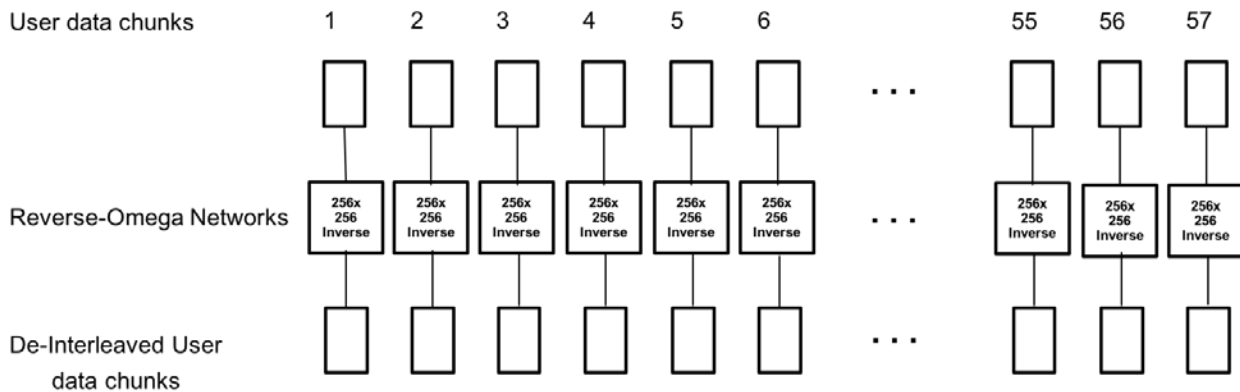
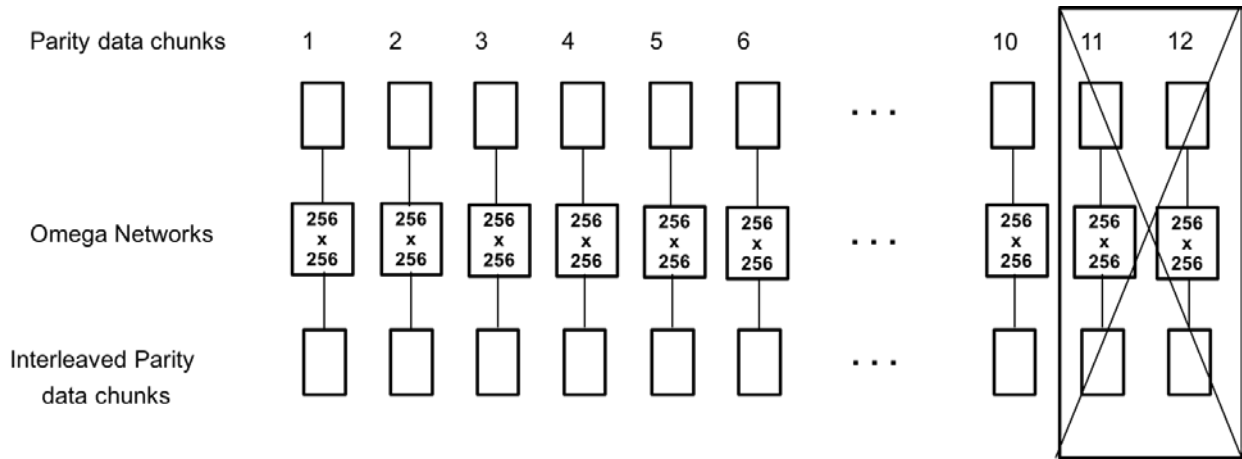


Figure x2 – Information Bit De-Interleaver

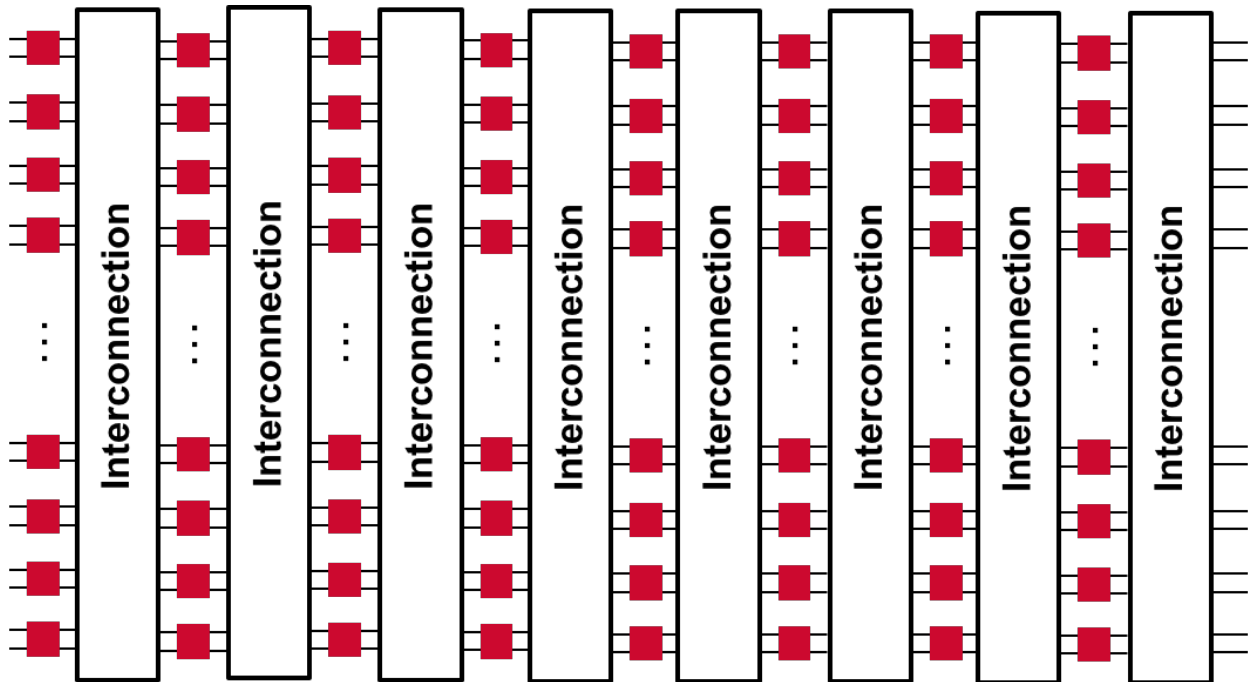
The parity bit interleaver consists of 12 local interleavers of size 256-by-256. These local interleavers are realized by 12 independent omega networks. Because puncturing length is fixed (512) and 512 bits make up of two whole data chunks, the last two parity omega networks are by-passed. In implementation, the parity bit interleaver consists of 10 omega networks.



**Figure x3 – Parity Bit Interleaver**

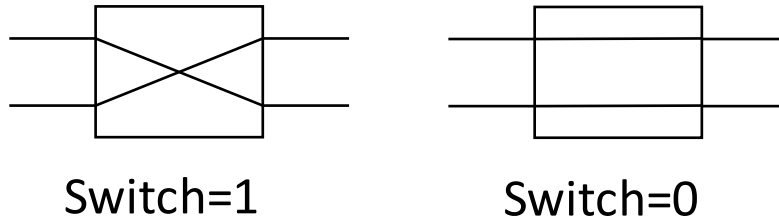
Note that the interleaver and de-interleaver are just reverse permutations of each other; the omega network and reverse-omega network are just reverse permutations of each other. With the omega network architecture, data is input from the left side and output from the right; while the reverse-omega network are obtained just by feeding the data to the right side and output from the left side.

Each omega network is made of an interconnection network with 8 stages of switches, each stage has 128 switches, and each switch has two inputs and two outputs as shown in Figure x4.



**Figure x4 – Omega Network 256 Interconnection Network**

Each switch is individually programmed. If the switch is programmed to be 1, then this switch performs a swap of the input bits, otherwise, the input will be pass-through as shown in Figure x5.

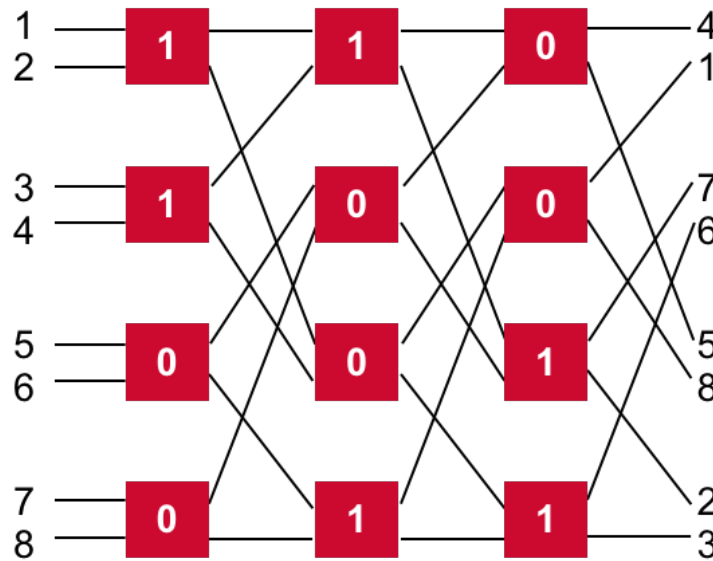


**Figure x5 – Switch programming**

The interconnection between each stage of switches is deterministic and is described as follows. Denote the two output ports of switch  $i$  in stage  $k$  as  $S^k_{i,0}$  and  $S^k_{i,1}$ ,  $k = 0, \dots, 7$  and  $i = 0, \dots, 7$ :

- Switch output port at stage  $k$ ,  $S^k_{i,0}$ , is connected to switch input port at stage  $k + 1$ ,  $S^{k+1}_{\lfloor \frac{i}{2} \rfloor, \text{mod}(i,2)}$
- Switch output port at stage  $k$ ,  $S^k_{i,1}$ , is connected to switch input port at stage  $k + 1$ ,  $S^{k+1}_{\lfloor \frac{i}{2} \rfloor + 64, \text{mod}(i,2)}$

As an example, Figure x6 illustrates an 8-by-8 omega network with interconnections of 3 stages of 4 switches; and for a given switch programming, how the inputs are mapped to the output.



**Figure x6 – Example 8x8 Omega Network with a given switch programming**

*Editor’s Note (to be removed prior to publication): Before entering WG ballot, content of Table 142-x1 and Table 142-x2 will be published under <http://standards.ieee.org/downloads/802.3/> in a machine readable format*

In implementation one 256-by-256 omega network of 8x128 switches is programmed based on a 128-bit control seed (see Table x2 and Table x3). The 128-bit switch programming sequence is derived by a circular bit shift of the control seed by  $x$  positions where  $x$  is given in Table x1 for each of the 8 stages:

**Table x1 Control seed circular bit shift for stage 1 through 8**

Stage	Circular shift $x$ (bits)
1	17
2	34
3	51
4	68
5	85
6	102
7	119
8	8

The control seeds for the 57 independent user interleavers are shown in Table x2 where each row is a 128-bit seed sequence.

**Table x2 – User interleaver control seed values**

User Interleaver	128-bit control seed sequence (represented by a 32 character hex value)
1	0xE388B09A74F4948E5DC0CC8A189AB9B2
2	0xC30AB4F49208FFEA24FF175D94967072
3	0x8831C546D3EC8B9FFF48449FA94E8F20
4	0x924332870C2237A3E1066A9FF8F2CC1E
5	0x90F6C130A03E70CF608179536C353F7E
6	0x0377AA718AACD36D1B30CA20D15631A9
7	0x9728EB4EAE3B936C32EA079DF81847EF
8	0xC1E5233AD21A9200B78B346590E1BD40
9	0x8FDCFCE6E3B0EADF96427F9398CE3F0C
10	0x3FC42923C901DEE00BBDD1940B413DA
11	0x42950A45CFABF16E868D96F05EF18F7B
12	0x873632E95D0D99BB1F57465C555EE9D2
13	0x0511387FA6EB93A2439196F19CEE673A
14	0x4CEF11A01DFBA05EC0019E8078C1B588
15	0x407CC39FD5DE6C9AC2C01E3B45FBEEB2
16	0xAEFC166F9D15EDE08C7F2B1474853614
17	0x8E6DB33BC7C89AF908AD1DC363379B43
18	0xE7E0B98690297B7C68D86B0E52798F4F
19	0xA1F178714BB7D36B134190A4681C888A
20	0x51BD15ABA9885BF811C0975CFC1B65E1
21	0xDA5C9A8EA2F89353D9F068A5F87F2D8E
22	0x3169A59D01B3CDB1270C8CB5E8F7A2D2
23	0x04E236BE89467E08D563DA4167A2DCA5
24	0x4EBB16BFE619C8E34498AFC4881853B0
25	0xEFBB12286647EC22C71DF6496FBEA03A
26	0x630F7E0FAF3C47152DA720E0D2EC6961
27	0x7C3D14A5BE9EE4A47164BF1B71C53ED6
28	0xA4660BF827EB63A4C12969EC81D4C089
29	0xF6309591A5F5EDB03339B67275CCB193
30	0x1393BD21441685C35FA1A3DE89A75BA2

31	0xE2327BD23111CB0ED154CC59E0A4554B
32	0x54AC4C7E587432DFCE54F6AE65F754F8
33	0x7ED1D3B87D3A1DEFDF1370FB6DAF7949
34	0x27CCFF46F2C94A45A93580D24469A4CE
35	0x992752B8963FC090989F6DA07CFCD3B3
36	0x13D39E3C5AB4AD76CF8B825FE902A5EA
37	0xB3AD1CD1EDF5174BAF4B0754F6305E81
38	0x22766236B9924F83AB04E737B64CD27D
39	0x5F3CDEA105AE029924CCA2898D57C3E7
40	0xAFE47DA0B9F6CC512DB8C9FDB68AE9B2
41	0x94E758DF617BDABFC0C47215C776995C
42	0x34640A892E466346C0A826FD4660F3C7
43	0x8954488350C6B47235F4C8476C2BD250
44	0xFB68B29BCAE6F1504BEDAAC99FDC7766
45	0x0834F8F35F4AB4E54985F1C791BFA76A
46	0x9DC737D5C6917CD060CC663AFA6A791
47	0x01896B6C8C6E35B512B4BBBC41AADFEC
48	0xF073F802029B8B381B78F27051962A5C
49	0x67AE64C51BB3B0CEE689B16FB3578C80
50	0x84C3F1408582DE32FB43EF1CA00215D4
51	0x6E733D348562EFE1F18FC6096D19B95A
52	0x578978DB42D919C5112A79B477F7E428
53	0x870383E6F6C6A0F3D56584638307424A
54	0x4FB769FC300E5A5B0EE8D8976843F074
55	0xCF92E6AABFCE5CB3F22E0302F1C8EC
56	0x4329FB56A657019F913FBA7AB0A57FB3
57	0x1C6192BEC8C3FAE3B58BB8D07A9BB1D7

The control seeds for the 10 independent parity interleavers are in Table x3 where each row is a 128-bit seed sequence.

**Table x3 – Parity interleaver control seed values**

Parity Interleaver	128-bit control seed sequence (represented by a 32 character hex value)
1	0x11C7DC599A6176D9E344BF752EAA34AF
2	0x5F5CF0209AE9B44BCDF952C8228DF089
3	0x89349C4BF190130BF8BE476B29BB963C
4	0xA26D3B8DCCB1D9C45EFC119FAE07A6C6
5	0xAC4529CCE52CC7D06047ED32764F847B
6	0x923ADC975B23629AFB81BE93ECAB25BF
7	0x2C4D7301D301D8B89A734A3F0AE4B6F5
8	0xEFCAA92F1018344246D4BD8348596ABE
9	0x7218537016E0844B8ED796F807AAA58D
10	0x4DF05D35759E07C9566EB14F2B224390

## Example initial control seed sequence

For example, from Table x2 the control seed sequence for the first user interleaver is:

0xE388B09A74F4948E5DC0CC8A189AB9B2

Which represents the binary sequence:

```
111000111000100010110000100110100111010011110100100101001
000111001011101110000001100110010001010000110001001101010
11100110110010
```

From Table x1, the switch programming sequence for the first stage of the user interleaver is a circular shift of the above control seed by 17 positions:

```
010111001101100101110001110001000101100001001101001110100
111101001001010010001110010111011100000011001100100010100
00110001001101
```

From Table x1, the switch programming sequence for the second stage of the user interleaver is a circular shifts of the above control seed by 34 positions:

```
100001100010011010101110011011001011100011100010001011000
010011010011101001111010010010100100011100101110111000000
11001100100010
```